DOKUZ EYLÜL UNIVERSITY
GRADUATE SCHOOL OF NATURAL AND APPLIED SCIENCES

NEW POSSIBILITIES IN THE DESIGN OF ANALOG INTEGRATED CIRCUIT WITH MOS-C REALIZATION

by
Ahmet GÖKÇEN

June, 2010
İZMİR

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A Thesis Submitted to the
Graduate School of Natural and Applied Sciences of Dokuz Eylül University
In Partial Fulfillment of the Requirements for the Degree of Doctor of Philosophy in Electrical and Electronics Engineering,
Electrical and Electronics Program

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Ph.D. THESIS EXAMINATION RESULT FORM

We have read the thesis entitled "**NEW POSSIBILITIES IN THE DESIGN OF ANALOG INTEGRATED CIRCUIT WITH MOS-C REALIZATION**" completed by **AHMET GÖKÇEN** under supervision of **PROF.DR. UĞUR ÇAM** and we certify that in our opinion it is fully adequate, in scope and in quality, as a thesis for the degree of Doctor of Philosophy.

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ACKNOWLEDGMENTS

First and foremost, I express my deepest gratitude to my advisor Prof. Dr. Uğur ÇAM for his guidance, support, and advices at every stage of this dissertation. It has been a great honor and privilege for me to work with Prof. Dr. ÇAM. His valuable insights, experiences, and encouragement will guide me in all aspects of my academic life in the future.

I would like to thank the member of my Thesis Progress Committee Dr. Haldun KARACA¸ for useful comments, trust and support.

I would like to thank the member of my Thesis Progress Committee Dr. Erol UYAR for his useful comments and suggestions.

I would like to thank Dr. Selçuk KILINÇ for his useful comments and suggestions.

I am also thankful to my kind friends Yakup KUTLU, Umut DENİZ, Şebnem SEÇKİN, Tarık SERİNDAĞ, Güven İPEKOĞLU, and my other dear friends who I could not write here for their helps, supports and warmest friendships throughout PhD studies.

I am also grateful to my love, Sevil SAHİLLİOĞLU because without her encouragement, suggestions, contributions and patience this study would not be possible.

Finally, with great pride, I would like to express my deep appreciation and gratitude to my family who gave me both material and spiritual support throughout my university education without expecting anything in return except for my success and health. They have been really understanding and patient. I love them all.

Ahmet GÖKÇEN

NEW POSSIBILITIES IN THE DESIGN OF ANALOG INTEGRATED CIRCUIT WITH MOS-C REALIZATION

ABSTRACT

In this thesis, MOS-C realization approach in analog integrated circuits is investigated. According to this approach, resistors in a circuit are implemented by MOS transistors. For this purpose, firstly the nonlinearity cancellation techniques in the MOS transistor currents are examined and the relevant equations are presented. Appropriate active elements, namely operational amplifier, operational transresistance amplifier, first generation current conveyor, second generation current conveyor, third generation current conveyor, inverting second generation curret conveyor, differential voltage current conveyor, differential difference current conveyor, for the nonlinearity cancellation techniques are given, also the element representations and the terminal equations are shown. Using the nonlinearity cancellation techniques and above mentioned active elements, two new first order allpass filters are presented. Kerwin-Huelsman-Newcomb, Fleischer-Tow and Tow-Thomas biquads are improved for fully integrable and electronically tunable property. A novel single amplifier biquad is obtained and an oscillator circuit is modified for tunable oscillation frequency. As an application example, fifth order elliptic video filter is given. In all of the above mentioned circuits, the resistors are implemented via MOS transistors and this feature gives them fully integrable property. By changing the gate voltage of the MOS transistor, the circuit parameters have electronically tunable feature. The natural frequency, the quality factor and the gain of the circuits can be changed electronically. The workability of the presented circuits has been verified by PSPICE simulation results.

Keywords: Analog Integrated Circuits, MOS-C Realization, Nonlinearity Cancellation in MOS Transistor Current

MOS-C GERÇEKLEMESİ İLE ANALOG TÜM DEVRE TASARIMINDA YENİ OLANAKLAR

ÖZ

Bu tezde, analog tümdevrelerdeki MOS-C gerçeklemesi yaklaşımı incelenmiştir. Bu yaklaşıma göre, devrelerdeki dirençler MOS tranzistörler ile gerçeklenir. Bu amaç için, ilk olarak MOS tranzistör akımındaki doğrusal olmayan terimlerin yok edilme teknikleri incelenmiş ve bu tekniklere ait denklemler verilmiştir. Bahsedilen bu tekniklerin kullanılabileceği uygun aktif eleman yapıları işlemsel kuvvetlendirici, işlemsel geçiş-direnç kuvvetlendiricisi, birinci nesil akım taşıyıcı, ikinci nesil akım taşıyıcı, üçüncü nesil akım taşıyıcı, ikinci nesil tersleyen akım taşıyıcı, diferansiyel gerilim akım taşıyıcı, diferansiyel fark akım taşıyıcı sunulmuş, terminal bağlantıları ve eleman simgeleri gösterilmiştir. Bahsedilen doğrusal olmayan terimleri yok etme tekniklerini ve bunlara uygun aktif elemanları kullanarak iki adet yeni birinci dereceden tüm geçiren süzgeç devresi tasarlanmıştır. Kerwin-Huelsman-Newcomb Fleischer-Tow ve Tow-Thomas filtre devreleri tümüyle tümleşik edilebilir ve elektronik olarak ayarlanabilir özellikte yeniden geliştirilmiştir, Yeni bir tek aktif elemanlı filtre devresi tasarlanmış ve daha önce sunulmuş olan bir osilatör devresi geliştirilerek elektronik ayarlı frekansa sahip hale getirilmiştir. Ayrıca bir uygulama devresi olarak da beşinci dereceden eliptik video filtre uygulaması sunulmuştur. Sunulan bütün devrelerdeki dirençler MOS tranzistörler ile gerçeklenmiş ve bu özellik sayesinde devreler tümdevre edilebilir hale gelmişlerdir. MOS tranzistörlerin kapı gerilimlerini değiştirerek, sunulan devrelerin açısal frekansları, kalite faktörleri ve kazançları elektronik olarak ayarlanabilir özelliğe sahip olmaktadır. Sunulan devrelerin çalışabilirliği PSPICE benzetim sonuçlarıyla gösterilmiştir.

Anahtar Kelimeler: Analog Tümdevreler, MOS-C Gerçeklemesi, MOS Tranzistör Akımındaki Doğrusal Olmayan Terimlerin Yok Edilmesi

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CHAPTER ONE
INTRODUCTION

1.1 Introductory Remarks

Metal-oxide-semiconductor (MOS) technology was originally developed for digital large-scale integration (LSI) design. The small size and self-isolating nature of the enhancement-mode MOS transistors allows a much higher functional density to be achieved on an integrated circuit (IC) chip than is possible with bipolar technology. Traditionally, MOS technology has been used extensively in the design of wholly digital system blocks, such as microprocessors and memories. On the other hand, analog circuit functions, such as amplifiers, digital to analog converters, and active filters, have been designed primarily with bipolar technology (Grebene, 1983).

Technological progress over years has rapidly increased the feasible level of integration for complete systems containing both digital and analog functions. Thus, the dividing line between analog and digital LSI technologies has become less distinct. Therefore, it has become necessary to extend the capabilities of MOS technology into analog IC design so that a higher level of system integration can be made economically feasible (Grebene, 1983).

The use of MOS transistors to perform analog functions presents many design challenges and requires a number of design compromises. In most cases, the resulting MOS analog blocks, such as operational amplifiers (op-amps), comparators, or voltage references, may not be able to meet the performance specifications of their bipolar equivalents, but still perform satisfactorily as a subsystem within the monolithic chip. The high density of MOS transistors makes it possible to integrate analog functions on a much smaller chip area. For example, a MOS op-amp requires only 30-50% of the chip area that is needed for an equivalent bipolar amplifier. The usage of MOS makes it possible to increase greatly the density of analog functions on the chip (Gray, Hurst, Lewis & Meyer, 2000).

Automatic electronic tuning is crucial for fully integrated filters to compensate the drifts of element values and filter performances due to component tolerance, device non-ideality, parasitic effects, temperature, environment and aging.

In conventional active RC filters in ICs, the resistor is the problem; it has a very limited range of values (normally $R \leq 40k\Omega$ without use of special processing techniques and resistances beyond the limit will be physically too large) and is not electronically tunable.

On the other hand, a MOSFET can be used as a voltage-controlled resistor biased in the ohmic region, with the resistance being adjustable by the bias gate voltage. It is therefore obvious that using the MOSFET to replace the resistor in active RC filters can meet the two requirements, which are electronic tunability and occupying less area, and the resulting filters are called the MOSFET-C filters (Deliyannis, Sun & Fidler, 1999).

MOS transistors, when used in filter applications with the aim of implementing linear resistors, suffer from non-idealities causing signal distortion: body effect, mobility variation, device mismatch. These effects cause nonlinear terms in transistor current. The main object is to eliminate these nonlinear terms. In the literature, several techniques are presented to cancel these nonlinear terms. Balanced two-transistor configurations have first been introduced to cancel out even order nonlinearities (Banu & Tsividis, 1983). It was later demonstrated using a strong-inversion MOS model that a four-transistor structure fully suppresses the body effect-related odd-order terms as well (Song, 1986, Czarnul, 1986). Another technique, which uses two depletion type MOS transistors, is introduced by Babanezhad & Temes, (1984). Tsividis, Banu & Khoury, (1986) gives eight nonlinearity cancellation techniques which include above mentioned techniques. Another technique for cancelling even and odd order nonlinearities in two-MOS transistor is introduced by Ismail & Fiez (1994) and Salama & Soliman (1999a).

In the literature, a great deal of filters, oscillators, integrators and other circuits exist using these nonlinearity cancellation techniques. MOSFET-C filters are proposed by Ismail, Smith & Beale (1988), Tsividis & Shi (1985), Salama & Soliman (1999a), Salama (2002), Liu, Tsao & Wu (1990), Ibrahim & Kuntman (2004), Hwang, Chen & Lee (2005), Mahmoud & Soliman (1999), Salama, Elwan & Soliman (2001), Schmid & Moschytz (1997), Chen, Tsao & Liu (2001), Hwang, Wu, Chen, Shih & Chou (2007), Fangxiong, Min, Heping, Hailong, Yin & Forster (2009), Hwang, Wu, Chen, Shih & Chou (2009). Salama & Soliman (1999a) is proposed filter and oscillator topologies. The resistors are implemented via two NMOS transistors. Also, Salama (2002) proposed a universal filter topology using resistor implementing technique with two NMOS transistor. The filter parameters can be controlled via NMOS gate voltages. Liu, Tsao & Wu (1990) and Hwang, Chen & Lee (2005) are proposed electronically controllable filter topologies. The resistors are implemented via four NMOS transistors. Oscillators, integrators, frequency depended negative resistor and equalizer circuits are proposed by Lee (2003), Osa & Carlosena (2000), Salama & Soliman (1999c), Jia & Chen (1995), Babanezhad & Temes (1984), Chiu, Tsay, Liu, Tsao & Chen (1995), Karaca, Metin & Kuntman (2010), Sakurai, Ismail, Michel, Sinenco & Brannen (1992). Osa & Carlosena (2000) and Lee (2003) proposed electronically tunable oscillation frequency oscillator. Four NMOS are used for implementing resistors. Babanezhad & Temes (1984) proposed integrated amplifier using op-amp and grounded resistor implementing technique via depletion type two NMOS transistors.

1.2 Overview of the Thesis

The main purpose of this thesis is to gain the knowledge of MOS-C realization approach in analog integrated circuit and to present new MOS-C based circuits.

This thesis is organized as follows. In Chapter 2, the implementation of resistors using MOS transistors and nonlinearity cancellation techniques are presented. For each technique, the linear and nonlinear terms are calculated and the resistor values are given.

In Chapter 3, suitable active components namely op-amp, operational transresistance amplifier (OTRA), first generation current conveyor (CCI), second generation current conveyor (CCII), third generation current conveyor (CCIII), inverting second generation curret conveyor (ICCII), differential voltage current conveyor (DVCC), differential difference current conveyor (DDCC) in IC technology for nonlinearity cancellation techniques are presented. The historical background, block diagram and terminal port relations of the components are given.

In Chapter 4, the performance comparison of four nonlinearity cancellation techniques is done by appling them on the integrator circuit. Frequency, transient and Total Harmonic Distortion (THD) analyses are presented in this chapter.

The MOS-C based allpass filter, biquadratic filter and oscillator circuit examples, and PSPICE simulation results are given in Chapter 5. All of the above mentioned circuits have electronically tunable feature and this property allows controllable center frequency, quality factor, and gain. And a fifth order video band elliptic filter topology, as the application example, is presented.

Finally, in Chapter 6, the conclusions are drawn and possible future works are given.

CHAPTER TWO
MOSFET BASED RESISTOR REALIZATION TECHNIQUES

IC design becomes more popular with the advances in analog VLSI technology. Resistors are one of the components in ICs, which can be designed and fabricated using semiconductor manufacturing process. Resistors fabricated in IC's physically occupy large chip areas. They have large parasitic capacitance, and that limits their applications for high frequency circuits. Resistor synthesis by using MOS transistors can result large resistance values, and they use smaller fraction of chip areas. It is important to reduce the area of the integrated circuits. In this respect, it could be attractive to implement the resistors using transistors which would reduce the size considerably. Also transistors consume less power than resistors and resistors suffer from heat effect. However, implementing resistors via MOS transistors yields linear and nonlinear terms in transistor current. The main problem is cancelling these nonlinear terms in the transistor current. In this chapter, the implementation of resistors using MOS transistors and ten nonlinearity cancellation techniques are presented. The linear and the nonlinear terms of the transistor currents are presented. The required equations are given. Also the comparisons of the techniques are given in a table.

2.1 The MOSFET as a Voltage Controlled Resistor

An n-channel MOSFET is shown in Figure 2.1. The device's gate is connected to a dc control voltage V_C and the substrate is connected to a fixed dc bias V_B (Tsividis, Banu & Khoury, 1986).

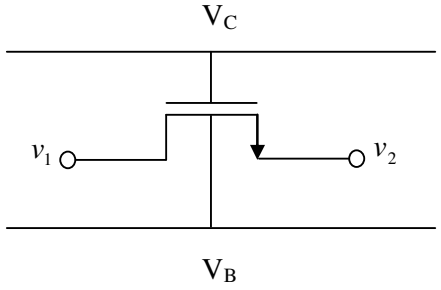

Figure 2.1 An n-channel MOSFET

To allow operation in the "non-saturation" region, the terminal voltages v_1 and v_2 are assumed to remain below V_C by at least an amount V_K as shown in Figure 2.2. Also, v_1 and v_2 are assumed to remain above V_B by a non-critical quantity V_Q (Tsividis, Banu & Khoury, 1986).

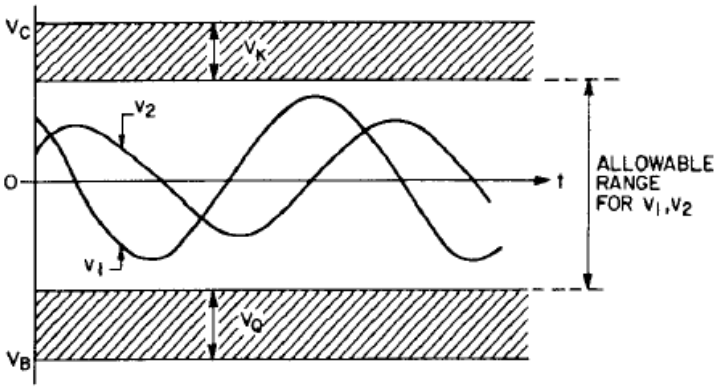

Figure 2.2 Terminal voltages for the transistor (Tsividis, Banu & Khoury, 1986)

A model for the MOS transistor is shown in Figure 2.3.

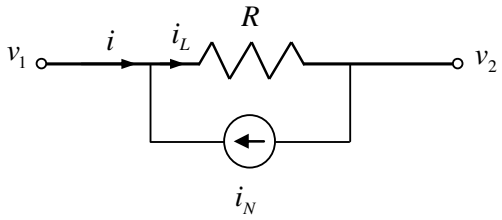

Figure 2.3 Low frequency large signal model for the MOS transistor

The transistor current i can be written in the following form;

$$i = i_L - i_N , \tag{2.1}$$

where, i_N and i_L represent nonlinear and linear terms, respectively.

The linear term of the transistor current can be defined as follows;

$$i_L = G(v_1 - v_2)\,. \tag{2.2}$$

In Equation (2.2), the conductance parameter G is given by;

$$G = \left(\frac{W}{L}\right)\mu C_{ox}\left(V_C - V_T\right). \tag{2.3}$$

where W and L are the channel width and length, respectively, μ is the effective mobility, C_{ox} is the oxide capacitance per unit area, V_T is the threshold voltage of the transistor. Clearly, if one cancels the effect of the i_N, the transistor behaves like a linear resistor with a conductance G. The resistance $R = 1/G$ can be written in the following form;

$$R = \left(\frac{L}{W}\right)R_S\,, \tag{2.4}$$

where L/W is aspect ratio of the transistor, which is a design parameter, and R_S is given by;

$$R_S = \frac{1}{\mu C_{ox}(V_C - V_T)}. \tag{2.5}$$

The above material holds also for p-channel devices, with appropriate changes in the signs of voltages and currents.

The nonlinear term in Equation (2.1) can be written in the following form;

$$i_N = g(v_1) - g(v_2)\,, \tag{2.6}$$

where the function $g(v)$ is independent of V_C and it can be written as;

$$g(v) = g_e(v) + g_o(v), \tag{2.7}$$

where $g_e(v)$ and $g_o(v)$ are even and odd functions, respectively, and can be expressed by ;

$$g_e(v) = \left(\frac{W}{L}\right)\mu C_{ox}\left\{\frac{1}{2}v^2 + \frac{1}{3}\gamma\left[(V_R + v)^{3/2} + (V_R - v)^{3/2}\right]\right\}, \tag{2.8}$$

$$g_o(v) = \left(\frac{W}{L}\right)\mu C_{ox}\left\{\gamma\left[\frac{1}{3}(V_R + v)^{3/2} - \frac{1}{3}(V_R - v)^{3/2} - V_R^{1/2}v\right]\right\}, \tag{2.9}$$

where γ is body effect coefficient and $V_R = \phi_B - V_B$.

The nonlinear term of the current i can be written using Equation (2.6) and (2.7) in the following form;

$$i_N = g_e(v_1) + g_o(v_1) - g_e(v_2) - g_o(v_2), \tag{2.10}$$

$$i_N = [g_e(v_1) - g_e(v_2)] + [g_o(v_1) - g_o(v_2)]. \tag{2.11}$$

The nonlinear term is;

$$i_N = \left[\begin{array}{l}\left[\left(\frac{W}{L}\right)\mu C_{ox}\left\{\begin{array}{l}\frac{1}{2}v_1^{\,2} + \frac{1}{3}\gamma(V_R + v_1)^{3/2} + \frac{1}{3}\gamma(V_R - v_1)^{3/2}\\ -\left\{\frac{1}{2}v_2^{\,2} + \frac{1}{3}\gamma(V_R + v_2)^{3/2} + \frac{1}{3}\gamma(V_R - v_2)^{3/2}\right\}\end{array}\right\}\right]\\ +\left[\left(\frac{W}{L}\right)\mu C_{ox}\left\{\begin{array}{l}\frac{1}{3}\gamma(V_R + v_1)^{3/2} - \frac{1}{3}\gamma(V_R - v_1)^{3/2} - \gamma V_R^{1/2}v_1\\ -\left\{\frac{1}{3}\gamma(V_R + v_2)^{3/2} - \frac{1}{3}\gamma(V_R - v_2)^{3/2} - \gamma V_R^{1/2}v_2\right\}\end{array}\right\}\right]\end{array}\right]. \tag{2.12}$$

After the simplification of the Equation (2.12), i_N is;

$$i_N = \left(\frac{W}{L}\right)\mu C_{ox}\left[\frac{1}{2}\left(v_1{}^2 - v_2{}^2\right) + \frac{2}{3}\gamma\left(V_R + v_1\right)^{3/2} - \frac{2}{3}\gamma\left(V_R + v_2\right)^{3/2} - \gamma V_R{}^{1/2}\left(v_1 - v_2\right)\right]. \tag{2.13}$$

The nonlinear current of transistor includes even $\left[g_e(v_1) - g_e(v_2)\right]$ and odd $\left[g_o(v_1) - g_o(v_2)\right]$ components of expression. The term $\left[g_e(v_1) - g_e(v_2)\right]$ is very small compared to the linear term i_L. The term $\left[g_o(v_1) - g_o(v_2)\right]$ depending on v_1 and v_2, can be large and its effect must be eliminated. Also, by connecting substrate to source, the body effect coefficient is zero, so the odd nonlinearities have been eliminated.

2.2 Nonlinearity Cancellation of Transistor Current

Many different techniques have been proposed for eliminating the effect of nonlinearities. Some cancel the nonlinearities in the current of one device; others cancel the nonlinearities in the difference or sum of the currents in two or more devices. In all cases except for the seventh nonlinearity cancellation technique given in the following, the substrate is assumed to be connected V_B. In the seventh nonlinearity cancellation technique, p-channel device is used and the p-channel device's substrate is connected to the opposite V_B (Tsividis, Banu & Khoury, 1986).

2.2.1 First Technique for Nonlinearity Cancellation

This technique uses an NMOS transistor, which operates in non-saturation region. Drain and source of the NMOS transistor is connected to equal but opposite voltages as shown in Figure 2.4. The substrate is assumed to be connected to the source, so the body effect is neglected.

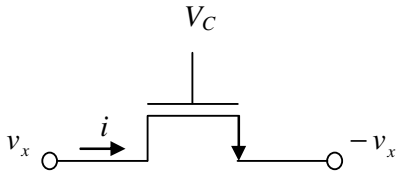

Figure 2.4 The first nonlinearity cancellation technique

The transistor current i can be written as; $i = i_L - i_N$. i_L and i_N had been calculated previously in Equations (2.2) and (2.13). For the first nonlinearity cancellation technique, i_N and i_L are defined as;

$$i_N = \left(\frac{W}{L}\right)\mu C_{ox}\left[\frac{2}{3}\gamma(V_R + v_x)^{3/2} - \frac{2}{3}\gamma(V_R - v_x)^{3/2} - \gamma V_R^{1/2} 2v_x\right], \tag{2.14}$$

$$i_L = \left(\frac{W}{L}\right)\mu C_{ox}(V_C - V_T)2v_x, \tag{2.15}$$

V_T is the threshold voltage of the transistor defined as ;

$$V_T = V_{FB} + \phi_B + \gamma V_R^{1/2}, \tag{2.16}$$

where V_{FB} is flat-band voltage and ϕ_B is the surface inversion potential. The transistor current i can be written as;

$$i = \left(\frac{W}{L}\right)\mu C_{ox}\left\{\{(V_C - V_{FB} - \phi_B)(2v_x)\} - \frac{2}{3}\gamma\left[(V_R + v_x)^{3/2} - (V_R - v_x)^{3/2} - V_R^{1/2} 2v_x\right]\right\}, \tag{2.17}$$

by neglecting nonlinear terms, Equation (2.18) is obtained.

$$i = \left(\frac{W}{L}\right)\mu C_{ox}(V_C - V_{FB} - \phi_B)(2v_x). \tag{2.18}$$

The resistance value of the transistor can be calculated as the following form;

$$R = \frac{2v_x}{i} = \frac{1}{\left(\frac{W}{L}\right)\mu C_{ox}\left(V_C - V_{FB} - \phi_B\right)}, \tag{2.19}$$

$$R = \frac{1}{\left(\frac{W}{L}\right)\mu C_{ox}\left(V_C - V_T\right)}. \tag{2.20}$$

By using this scheme, the even nonlinearities are eliminated. For zero body effect coefficient, the remaining odd nonlinearities are eliminated completely.

2.2.2 Second Technique for Nonlinearity Cancellation

In this technique, two NMOS transistors are used, each drain and source terminals of which is connected to equal but opposite voltages, as shown in Figure 2.5.

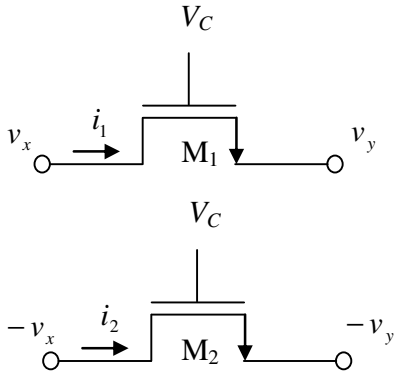

Figure 2.5 The second nonlinearity cancellation technique

The currents of the transistors are;

$$i_1 - i_2 = \left[i_{L1} - i_{L2}\right] - \left[i_{N1} - i_{N2}\right]. \tag{2.21}$$

Both nonlinear and linear terms can be written in the following form;

$$i_{N1} = \left(\frac{W}{L}\right)\mu C_{ox}\left[\frac{1}{2}\left(v_x{}^2 - v_y{}^2\right) + \frac{2}{3}\gamma\left(V_R + v_x\right)^{3/2} - \frac{2}{3}\gamma\left(V_R + v_y\right)^{3/2} - \gamma V_R{}^{1/2}\left(v_x - v_y\right)\right]. \tag{2.22}$$

$$i_{N2} = \left(\frac{W}{L}\right)\mu C_{ox}\left[\begin{array}{l}\frac{1}{2}\left(\left(-v_x\right)^2 - \left(-v_y\right)^2\right) + \frac{2}{3}\gamma\left(V_R - v_x\right)^{3/2} \\ -\frac{2}{3}\gamma\left(V_R - v_y\right)^{3/2} - \gamma V_R{}^{1/2}\left(-v_x + v_y\right)\end{array}\right]. \tag{2.23}$$

$$i_{L1} = \left(\frac{W}{L}\right)\mu C_{ox}\left(V_C - V_T\right)\left(v_x - v_y\right). \tag{2.24}$$

$$i_{L2} = \left(\frac{W}{L}\right)\mu C_{ox}\left(V_C - V_T\right)\left(\left(-v_x\right) - \left(-v_y\right)\right). \tag{2.25}$$

Nonlinear term of the current $i_1 - i_2$ can be written in the following form;

$$i_{N1} - i_{N2} = \left(\frac{W}{L}\right)\mu C_{ox}\left[\begin{array}{l}\frac{2}{3}\gamma\left(V_R + v_x\right)^{3/2} - \frac{2}{3}\gamma\left(V_R + v_y\right)^{3/2} - \frac{2}{3}\gamma\left(V_R - v_x\right)^{3/2} \\ +\frac{2}{3}\gamma\left(V_R - v_y\right)^{3/2} - 2\gamma V_R{}^{1/2}\left(v_x - v_y\right)\end{array}\right]. \tag{2.26}$$

At the same time, linear term of the current $i_1 - i_2$ can be written in the following form;

$$i_{L1} - i_{L2} = \left(\frac{W}{L}\right)\mu C_{ox}\left(V_C - V_T\right)2\left(v_x - v_y\right). \tag{2.27}$$

Thus, current $i_1 - i_2$ is obtained as;

$$i_1 - i_2 = \left[\begin{array}{l}\left(\frac{W}{L}\right)\mu C_{ox}\left(V_C - V_T\right)2\left(v_x - v_y\right) - \left(\frac{W}{L}\right)\mu C_{ox}\left[\begin{array}{l}\frac{2}{3}\gamma\left(V_R + v_x\right)^{3/2} - \frac{2}{3}\gamma\left(V_R + v_y\right)^{3/2} \\ -\frac{2}{3}\gamma\left(V_R - v_x\right)^{3/2} + \frac{2}{3}\gamma\left(V_R - v_y\right)^{3/2} \\ -2\gamma V_R{}^{1/2}\left(v_x - v_y\right)\end{array}\right]\end{array}\right] \tag{2.28}$$

Because the body effect coefficient is zero, the nonlinear terms can be neglected, then the transistor current becomes as;

$$i = \left(\frac{W}{L}\right)\mu C_{ox}(V_C - V_T)2(v_x - v_y). \tag{2.29}$$

Thus, the resistance value of the NMOS transistors is obtained as;

$$R = \frac{2(v_x - v_y)}{i} = \frac{1}{\left(\frac{W}{L}\right)\mu C_{ox}(V_C - V_{FB} - \phi_B)} = \frac{1}{\left(\frac{W}{L}\right)\mu C_{ox}(V_C - V_T)}. \tag{2.30}$$

Similarly, as mentioned in the first nonlinearity cancellation technique, using this scheme, the even nonlinearities and the remaining odd nonlinearities are eliminated completely.

2.2.3 Third Technique for Nonlinearity Cancellation

This technique is similar to the second nonlinearity cancellation technique. Only difference is, the source terminals of both NMOS transistors are connected to the same voltage as depicted in Figure 2.6.

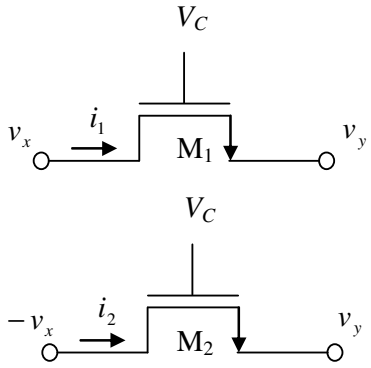

Figure 2.6 The third nonlinearity cancellation technique

Nonlinear and linear terms can be defined as the following form;

$$i_{N1} = \left(\frac{W}{L}\right)\mu C_{ox}\left[\frac{1}{2}\left(v_x{}^2 - v_y{}^2\right) + \frac{2}{3}\gamma\left(V_R + v_x\right)^{3/2} - \frac{2}{3}\gamma\left(V_R + v_y\right)^{3/2} - \gamma V_R{}^{1/2}\left(v_x - v_y\right)\right]. \tag{2.31}$$

$$i_{N2} = \left(\frac{W}{L}\right)\mu C_{ox}\left[\begin{array}{l}\frac{1}{2}\left(\left(-v_x\right)^2 - \left(v_y\right)^2\right) + \frac{2}{3}\gamma\left(V_R - v_x\right)^{3/2} \\ -\frac{2}{3}\gamma\left(V_R + v_y\right)^{3/2} - \gamma V_R{}^{1/2}\left(-v_x - v_y\right)\end{array}\right]. \tag{2.32}$$

$$i_{L1} = \left(\frac{W}{L}\right)\mu C_{ox}\left(V_C - V_T\right)\left(v_x - v_y\right). \tag{2.33}$$

$$i_{L2} = \left(\frac{W}{L}\right)\mu C_{ox}\left(V_C - V_T\right)\left(\left(-v_x\right) - \left(v_y\right)\right). \tag{2.34}$$

Nonlinear term of the current $i_{N1} - i_{N2}$ can be calculated as the following form;

$$i_{N1} - i_{N2} = \left(\frac{W}{L}\right)\mu C_{ox}\left[\frac{2}{3}\gamma\left(V_R + v_x\right)^{3/2} - \frac{2}{3}\gamma\left(V_R - v_x\right)^{3/2} - 2\gamma V_R{}^{1/2}\left(v_x\right)\right]. \tag{2.35}$$

Linear term of the current $i_{L1} - i_{L2}$ can be written as the following form;

$$i_{L1} - i_{L2} = \left(\frac{W}{L}\right)\mu C_{ox}\left(V_C - V_{TB}\right)2\left(v_x\right). \tag{2.36}$$

The transistor current $i_1 - i_2$, which is defined as $\left[i_{L1} - i_{L2}\right] - \left[i_{N1} - i_{N2}\right]$, can be written as;

$$i_1 - i_2 = \left(\frac{W}{L}\right)\mu C_{ox}\left\{\begin{array}{l}\left(V_C - V_T\right)2v_x \\ -\left[\frac{2}{3}\gamma\left(V_R + v_x\right)^{3/2} - \frac{2}{3}\gamma\left(V_R - v_x\right)^{3/2} - 2\gamma V_R{}^{1/2}v_x\right]\end{array}\right\}. \tag{2.37}$$

By using this scheme, the even nonlinearities are eliminated. By neglecting nonlinear terms the resistance value can be calculated as;

$$i = \left(\frac{W}{L}\right)\mu C_{ox}\left(V_C - V_T\right)2v_x \,. \tag{2.38}$$

$$R = \frac{2v_x}{i} = \frac{1}{\left(\frac{W}{L}\right)\mu C_{ox}\left(V_C - V_T\right)}. \tag{2.39}$$

For the body effect coefficient of zero, the remaining odd nonlinearities are eliminated completely.

2.2.4 Fourth Technique for Nonlinearity Cancellation

Figure 2.7 shows another nonlinearity cancellation technique. An NMOS transistor's source and drain are connected to different voltages. Also as shown in Figure 2.7, the gate is not tied to a control voltage directly as before, but instead it has voltages containing a control component (V_C') and a signal dependent component.

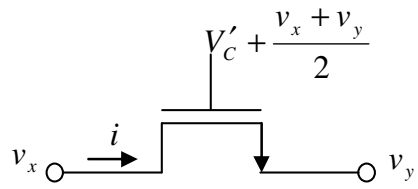

Figure 2.7 The fourth nonlinearity cancellation technique

The current of the transistor is;

$$i = i_L - i_N \,. \tag{2.40}$$

The nonlinear and the linear terms of the Equation (2.40) can be written as;

$$i_N = \left(\frac{W}{L}\right)\mu C_{ox}\left[\frac{1}{2}\left(v_x{}^2 - v_y{}^2\right) + \frac{2}{3}\gamma\left(V_R + v_x\right)^{3/2} - \frac{2}{3}\gamma\left(V_R + v_y\right)^{3/2} - \gamma V_R{}^{1/2}\left(v_x - v_y\right)\right]. \tag{2.41}$$

$$i_L = \left(\frac{W}{L}\right)\mu C_{ox}\left(V_C - V_T\right)\left(v_x - v_y\right). \tag{2.42}$$

If the control voltage of the transistor is $V_C = V_C' + \frac{v_x + v_y}{2}$ then, linear term of the current becomes as;

$$i_L = \left(\frac{W}{L}\right)\mu C_{ox}\left(V_C' + \frac{v_x + v_y}{2} - V_T\right)\left(v_x - v_y\right). \tag{2.43}$$

After required calculations, i_L can be calculated as;

$$i_L = \left(\frac{W}{L}\right)\mu C_{ox}\left(V_C' - V_T\right)\left(v_x - v_y\right) + \left(\frac{v^2{}_x - v^2{}_y}{2}\right). \tag{2.44}$$

Substituting i_L and i_N in Equation (2.40), the transistor current i can be written as the following form;

$$i = \left(\frac{W}{L}\right)\mu C_{ox}\left\{\left(V_C' - V_T\right)\left(v_x - v_y\right) - \left[\frac{2}{3}\gamma\left(V_R + v_x\right)^{3/2} - \frac{2}{3}\gamma\left(V_R - v_y\right)^{3/2} + \gamma V_R{}^{1/2}\left(v_x - v_y\right)\right]\right\}. \tag{2.45}$$

These schemes do not eliminate even nonlinearities completely. This problem can be eliminated if a signal-dependent substrate voltage is supplied, using voltage level shifters. By neglecting nonlinear terms and body effect coefficient, the resistance value can be given by;

$$i = \left(\frac{W}{L}\right)\mu C_{ox}\left(V_C' - V_T\right)\left(v_x - v_y\right). \tag{2.46}$$

$$R = \frac{\left(v_x - v_y\right)}{i} = \frac{1}{\left(\frac{W}{L}\right)\mu C_{ox}\left(V_C' - V_T\right)}. \tag{2.47}$$

Due to the fact that body effect coefficient is zero, the odd nonlinearities are eliminated completely.

2.2.5 Fifth Technique for Nonlinearity Cancellation

The fifth nonlinearity cancellation technique consists of two NMOS transistors, which are connected in parallel, as seen in Figure 2.8. The gate is not tied to a control voltage directly. The gate voltages are $V_C = V_C' + v_y$ and $V_C = V_C' + v_x$ for the first and the second NMOS transistors, respectively.

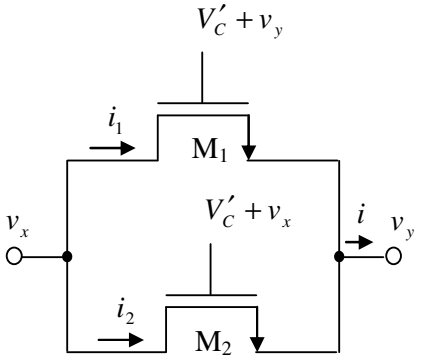

Figure 2.8 The fifth nonlinearity cancellation technique

The current of the transistors is equal to;

$$i_1 + i_2 = [i_{L1} + i_{L2}] - [i_{N1} + i_{N2}]. \tag{2.48}$$

Nonlinear terms are;

$$i_{N1} = \left(\frac{W}{L}\right)\mu C_{ox}\left[\frac{1}{2}\left(v_x{}^2 - v_y{}^2\right) + \frac{2}{3}\gamma\left(V_R + v_x\right)^{3/2} - \frac{2}{3}\gamma\left(V_R + v_y\right)^{3/2} - \gamma V_R{}^{1/2}\left(v_x - v_y\right)\right]. \tag{2.49}$$

$$i_{N2} = \left(\frac{W}{L}\right)\mu C_{ox}\left[\frac{1}{2}\left(v_x{}^2 - v_y{}^2\right) + \frac{2}{3}\gamma\left(V_R + v_x\right)^{3/2} - \frac{2}{3}\gamma\left(V_R + v_y\right)^{3/2} - \gamma V_R{}^{1/2}\left(v_x - v_y\right)\right]. \tag{2.50}$$

$$i_N = \left(\frac{W}{L}\right)\mu C_{ox}\left[\left(v_x{}^2 - v_y{}^2\right) + \frac{4}{3}\gamma\left(V_R + v_x\right)^{3/2} - \frac{4}{3}\gamma\left(V_R + v_y\right)^{3/2} - 2\gamma V_R{}^{1/2}\left(v_x - v_y\right)\right]. \tag{2.51}$$

Linear terms are;

$$i_{L1} = i_{L2} = \left(\frac{W}{L}\right)\mu C_{ox}\left(V_C - V_T\right)\left(v_x - v_y\right). \tag{2.52}$$

By substituting control voltage and threshold voltage, which is given in Equation (2.16) into linear terms, the following equations can be derived.

$$i_{L1} = \left(\frac{W}{L}\right)\mu C_{ox}\left[\left(V_C' + v_y - V_{FB} - \phi_B - \gamma\left(V_R\right)^{1/2}\right)\left(v_x - v_y\right)\right]. \tag{2.53}$$

$$i_{L2} = \left(\frac{W}{L}\right)\mu C_{ox}\left[\left(V_C' + v_x - V_{FB} - \phi_B - \gamma\left(V_R\right)^{1/2}\right)\left(v_x - v_y\right)\right]. \tag{2.54}$$

$$i_L = \left(\frac{W}{L}\right)\mu C_{ox}\left[2\left(V_C' - V_{FB} - \phi_B\right)\left(v_x - v_y\right) + \left[\left(v_x + v_y\right)\left(v_x - v_y\right)\right] - 2\gamma\left(V_R\right)^{1/2}\left(v_x - v_y\right)\right]. \tag{2.55}$$

$$i = \left(\frac{W}{L}\right)\mu C_{ox}\left[2\left(V_C' - V_{FB} - \phi_B\right)\left(v_x - v_y\right) + \frac{4}{3}\gamma\left(V_R + v_x\right)^{3/2} - \frac{4}{3}\gamma\left(V_R + v_y\right)^{3/2}\right]. \tag{2.56}$$

By neglecting nonlinear terms of the i current Equation (2.57) is obtained as;

$$i = \left(\frac{W}{L}\right)\mu C_{ox}\left[\left(V_C' - V_{FB} - \phi_B\right)2\left(v_x - v_y\right)\right]. \tag{2.57}$$

Thus, resistance value can be written as;

$$R = \frac{2(v_x - v_y)}{i} = \frac{1}{\left(\frac{W}{L}\right)\mu C_{ox}(V_C' - V_T)}. \quad (2.58)$$

The schemes, which are given in Figure 2.7 and Figure 2.8, do not eliminate even nonlinearities completely. It is easy to verify that the scheme in Figure 2.8 will work even if the control voltage components on each gate are different. In particular, if the control component of the bottom transistor's gate is set to zero, and if $v_y = 0$, one obtains the circuit of Figure 2.9. Due to the body effect coefficient is zero, the odd nonlinearities are eliminated completely.

2.2.6 Sixth Technique for Nonlinearity Cancellation

In Figure 2.8 if the control voltage of the bottom transistor's gate is set to zero, and if v_y=0, the circuit, which is shown in Figure 2.9, is obtained. To keep the bottom transistor on, the circuit necessitates the usage of "depletion mode" devices (V_T<0). This scheme does not eliminate even nonlinearities completely. The transistors can purposely be mismatched to increase the quality of linearity, by an amount dependent on fabrication process parameters. The scheme has limited resistance variability compared to the other schemes, because one of the transistors are not controlled by V_C and represents a practically fixed resistance in parallel with the other transistor. In practical situations with a limited range for V_C, this may take it difficult to compensate for all fabrication tolerances and environmental changes. The expression for the resistance R for this circuit is different from before, in that V_T should be replaced by $2V_T$.

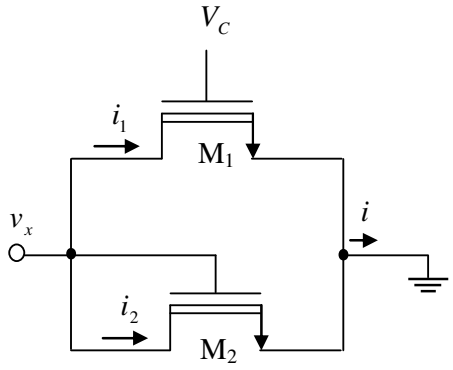

Figure 2.9 The sixth nonlinearity cancellation technique

The current of the transistors is;

$$i_1 + i_2 = [i_{L1} + i_{L2}] - [i_{N1} + i_{N2}]. \tag{2.59}$$

Nonlinear terms are;

$$i_{N1} = i_{N2} = \left(\frac{W}{L}\right)\mu C_{ox}\left[\frac{1}{2}V_x{}^2 + \frac{2}{3}\gamma(V_R + v_x)^{3/2} - \frac{2}{3}\gamma(V_R)^{3/2} - \gamma V_R{}^{1/2}v_x\right]. \tag{2.60}$$

Linear terms are;

$$i_{L1} = i_{L2} = \left(\frac{W}{L}\right)\mu C_{ox}[(V_C + v_x - 2V_T)(v_x)]. \tag{2.61}$$

Substituting linear and nonlinear terms into account the transistor current i is obtained as;

$$i = \left(\frac{W}{L}\right)\mu C_{ox}\left\{(V_C - 2V_T)(v_x) - \left[\frac{4}{3}\gamma(V_R + v_x)^{3/2} - \frac{4}{3}\gamma(V_R)^{3/2} + 2\gamma V_R{}^{1/2}(v_x)\right]\right\}. \tag{2.62}$$

By neglecting nonlinear terms;

$$i = \left(\frac{W}{L}\right)\mu C_{ox}\left[(V_C - 2V_T)(v_x)\right]. \tag{2.63}$$

These schemes do not eliminate even nonlinearities completely. The resistance value is defined as;

$$R = \frac{v_x}{i} = \frac{1}{\left(\frac{W}{L}\right)\mu C_{ox}\left(V_C - 2V_T\right)}. \tag{2.64}$$

The remaining odd nonlinearities are eliminated completely because body effect coefficient is zero.

2.2.7 Seventh Technique for Nonlinearity Cancellation

In the seventh nonlinearity cancellation technique, an NMOS and a PMOS transistor is connected parallel as shown in Figure 2.10. Each type of transistor has its own control voltages.

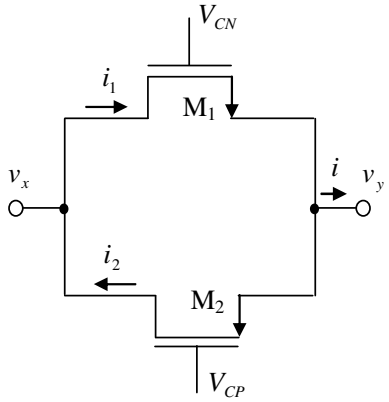

Figure 2.10 The seventh nonlinearity cancellation technique

The current of the transistors is;

$$i_1 - i_2 = \left[i_{L1} - i_{L2}\right] - \left[i_{N1} - i_{N2}\right]. \tag{2.65}$$

Nonlinear terms are;

$$i_{N1} = \left(\frac{W}{L}\right)\mu C_{ox}\left[\frac{1}{2}\left(v_x{}^2 - v_y{}^2\right) + \frac{2}{3}\gamma\left(V_R + v_x\right)^{3/2} - \frac{2}{3}\gamma\left(V_R + v_y\right)^{3/2} - \gamma V_R{}^{1/2}\left(v_x - v_y\right)\right]. \tag{2.66}$$

$$i_{N2} = \left(\frac{W}{L}\right)\mu C_{ox}\left[\frac{1}{2}\left(v_y{}^2 - v_x{}^2\right) + \frac{2}{3}\gamma\left(V_R + v_y\right)^{3/2} - \frac{2}{3}\gamma\left(V_R + v_x\right)^{3/2} - \gamma V_R{}^{1/2}\left(v_y - v_x\right)\right]. \tag{2.67}$$

$$i_N = \left(\frac{W}{L}\right)\mu C_{ox}\left[\frac{4}{3}\gamma\left(V_R + v_x\right)^{3/2} - \frac{4}{3}\gamma\left(V_R + v_y\right)^{3/2}\right]. \tag{2.68}$$

Linear terms are;

$$i_{L1} = \left(\frac{W}{L}\right)\mu C_{ox}\left(V_{CN} - V_T\right)\left(v_x - v_y\right). \tag{2.69}$$

$$i_{L2} = \left(\frac{W}{L}\right)\mu C_{ox}\left(V_{CP} - (-V_T)\right)\left(v_y - v_x\right). \tag{2.70}$$

$$i_L = \left(\frac{W}{L}\right)\mu C_{ox}\left(V_{CN} - V_{CP}\right)\left(v_x - v_y\right). \tag{2.71}$$

Substituting linear and nonlinear terms into account, the transistor current i is obtained as;

$$i = \left(\frac{W}{L}\right)\mu C_{ox}\left\{\left(V_{CN} - V_{CP}\right)\left(v_x - v_y\right) - \left[\frac{4}{3}\gamma\left(V_R + v_x\right)^{3/2} - \frac{4}{3}\gamma\left(V_R + v_y\right)^{3/2}\right]\right\}. \tag{2.72}$$

By neglecting nonlinear terms;

$$i = \left(\frac{W}{L}\right)\mu C_{ox}\left[\left(V_{CN} - V_{CP}\right)\left(v_x - v_y\right)\right]. \tag{2.73}$$

$$\left(\frac{1}{R_N} + \frac{1}{R_P}\right) = \frac{i}{\left(v_x - v_y\right)} = \frac{1}{\left(\frac{W}{L}\right)\mu C_{ox}\left(V_{CN} - V_{CP}\right)}. \tag{2.74}$$

This circuit has been used as a crude linear resistor for several years in CMOS op-amps and other analog circuits. If the n and p channel devices are purposely mismatched (based on a knowledge of fabrication process parameters), their nonlinearities can be approximately cancel out. Since n and p channel devices are made differently, one cannot expect this scheme to provide high linearity. For zero body effect coefficient, the odd nonlinearities are eliminated completely.

2.2.8 Eighth Technique for Nonlinearity Cancellation

Another technique for nonlinearity cancellation, which is shown in Figure 2.11, consists of four NMOS transistors. The transistors have different control voltages, which are named Vc_1 and Vc_2, as seen in Figure 2.11.

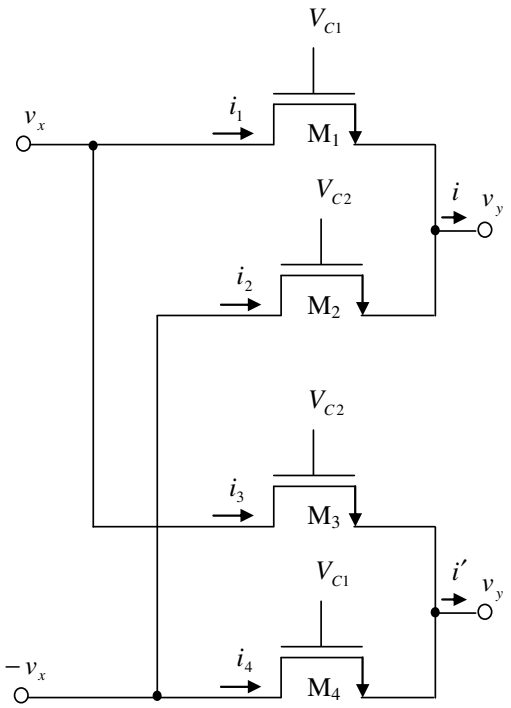

Figure 2.11 The eighth nonlinearity cancellation technique

The current of the transistors is;

$$i - i' = \left[\left(i_{L1} + i_{L2}\right) - \left(i_{L3} + i_{L4}\right)\right] - \left[\left(i_{N1} + i_{N2}\right) - \left(i_{N3} + i_{N4}\right)\right]. \tag{2.75}$$

Nonlinear terms are;

$$i_{N1} = i_{N3} = \left(\frac{W}{L}\right)\mu C_{ox}\begin{bmatrix}\frac{1}{2}\left(v_x{}^2 - v_y{}^2\right) + \frac{2}{3}\gamma\left(V_R + v_x\right)^{3/2} \\ -\frac{2}{3}\gamma\left(V_R + v_y\right)^{3/2} - \gamma V_R{}^{1/2}\left(v_x - v_y\right)\end{bmatrix}. \tag{2.76}$$

$$i_{N2} = i_{N4} = \left(\frac{W}{L}\right)\mu C_{ox}\begin{bmatrix}\frac{1}{2}\left(\left(-v_x\right)^2 - v_y{}^2\right) + \frac{2}{3}\gamma\left(V_R - v_x\right)^{3/2} \\ -\frac{2}{3}\gamma\left(V_R + v_y\right)^{3/2} - \gamma V_R{}^{1/2}\left(\left(-v_x\right) - v_y\right)\end{bmatrix}. \tag{2.77}$$

Linear terms are;

$$i_{L1} = \left(\frac{W}{L}\right)\mu C_{ox}\left(V_{C1} - V_T\right)\left(v_x - v_y\right). \tag{2.78}$$

$$i_{L2} = \left(\frac{W}{L}\right)\mu C_{ox}\left(V_{C2} - V_T\right)\left(-v_x - v_y\right). \tag{2.79}$$

$$i_{L3} = \left(\frac{W}{L}\right)\mu C_{ox}\left(V_{C2} - V_T\right)\left(v_x - v_y\right). \tag{2.80}$$

$$i_{L4} = \left(\frac{W}{L}\right)\mu C_{ox}\left(V_{C1} - V_T\right)\left(-v_x - v_y\right). \tag{2.81}$$

Taking linear and nonlinear terms into account and neglecting nonlinear terms, the transistor current $i - i'$ is obtained as the following form;

$$i - i' = \left(\frac{W}{L}\right)\mu C_{ox}\left[2\left(V_{C1} - V_{C2}\right)\left(v_x\right)\right]. \tag{2.82}$$

$$\left(\frac{1}{R_1} + \frac{1}{R_2}\right) = \frac{2v_x}{i - i'} = \frac{1}{\left(\frac{W}{L}\right)\mu C_{ox}\left(V_{C1} - V_{C2}\right)}. \tag{2.83}$$

The circuit in Figure 2.11 achieves in principle complete cancellation of both even and odd nonlinearities. In this figure, R_1 and R_2 are the resistance values.

2.2.9 Ninth Technique for Nonlinearity Cancellation

This technique is similar to the third nonlinearity cancellation technique. Only difference is both NMOS's source and drain are connected to the same voltage as depicted in Figure 2.12. Each transistor has its own control voltage.

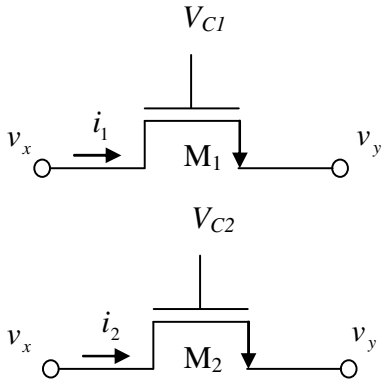

Figure 2.12 The ninth nonlinearity cancellation technique

Nonlinear and linear terms can be defined as the following form;

$$i_{N1} = \left(\frac{W}{L}\right)\mu C_{ox}\begin{bmatrix}\frac{1}{2}\left(v_x{}^2 - v_y{}^2\right) + \frac{2}{3}\gamma\left(V_R + v_x\right)^{3/2} \\ -\frac{2}{3}\gamma\left(V_R + v_y\right)^{3/2} - \gamma V_R{}^{1/2}\left(v_x - v_y\right)\end{bmatrix}. \tag{2.84}$$

$$i_{N2} = \left(\frac{W}{L}\right)\mu C_{ox}\begin{bmatrix}\frac{1}{2}\left((v_x)^2 - (v_y)^2\right) + \frac{2}{3}\gamma\left(V_R + v_x\right)^{3/2} \\ -\frac{2}{3}\gamma\left(V_R + v_y\right)^{3/2} - \gamma V_R{}^{1/2}\left(v_x - v_y\right)\end{bmatrix}. \tag{2.85}$$

$$i_{L1} = \left(\frac{W}{L}\right)\mu C_{ox}\left(V_{C1} - V_T\right)\left(v_x - v_y\right). \tag{2.86}$$

$$i_{L2} = \left(\frac{W}{L}\right)\mu C_{ox}\left(V_{C2} - V_T\right)\left(\left(v_x\right) - \left(v_y\right)\right). \tag{2.87}$$

Nonlinear term of the current $i_{N1} - i_{N2}$ can be calculated as the following form;

$$i_{N1} - i_{N2} = \left(\frac{W}{L}\right)\mu C_{ox}\begin{bmatrix} \frac{2}{3}\gamma\left(V_R + v_x\right)^{3/2} - \frac{2}{3}\gamma\left(V_R - v_x\right)^{3/2} - 2\gamma V_R^{1/2}\left(v_x\right) \\ -\frac{2}{3}\gamma\left(V_R + v_x\right)^{3/2} + \frac{2}{3}\gamma\left(V_R - v_x\right)^{3/2} + 2\gamma V_R^{1/2}\left(v_x\right) \end{bmatrix}. \tag{2.88}$$

Linear term of the current $i_{L1} - i_{L2}$ can be written as the following form;

$$i_{L1} - i_{L2} = \left(\frac{W}{L}\right)\mu C_{ox}\left(V_{C1} - V_{C2}\right)\left(v_x - v_y\right). \tag{2.89}$$

The transistor current $i_1 - i_2$, which is defined as $\left[i_{L1} - i_{L2}\right] - \left[i_{N1} - i_{N2}\right]$, can be written as;

$$i_1 - i_2 = \left(\frac{W}{L}\right)\mu C_{ox}\left[\left(V_{C1} - V_{C2}\right).v_x - v_y\right)\right]. \tag{2.90}$$

Thus, the resistance value can be calculated as;

$$i = \left(\frac{W}{L}\right)\mu C_{ox}\left(V_{C1} - V_{C2}\right)\left(v_x - v_y\right). \tag{2.91}$$

$$R = \frac{\left(v_x - v_y\right)}{i} = \frac{1}{\left(\frac{W}{L}\right)\mu C_{ox}\left(V_{C1} - V_{C2}\right)}. \tag{2.92}$$

By using this scheme, both the even and the odd nonlinearities are eliminated (Ismail & Fiez, 1994; Salama & Soliman, 1999a).

2.2.10 Tenth Nonlinearity Cancellation Technique

This technique uses two NMOS transistors, which are operating in saturation region, as shown in Figure 2.13.

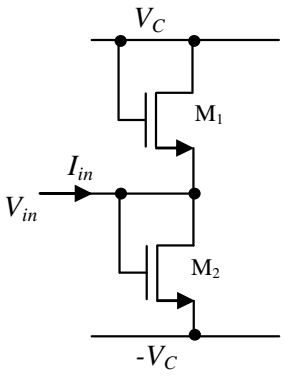

Figure 2.13 The tenth nonlinearity cancellation technique

The matched two transistors M_1 and M_2 are diode connected. Using square law characteristic, the drain currents in M_1 and M_2 can be expressed as;

$$Id_1 = \frac{\mu_n C_{ox}}{2}\frac{W}{L}\left(V_C - V_{in} - V_T\right)^2, \tag{2.93}$$

$$Id_2 = \frac{\mu_n C_{ox}}{2}\frac{W}{L}\left(V_{in} - (-V_C) - V_T\right)^2 . \tag{2.94}$$

A voltage V_{in} is applied to the central node of the electronic resistor circuit, developing a current I_{in} into the node. Using Kirchhoff's current law with Equations (2.93) and (2.94), a simple algebraic expression can be obtained for the resistance as;

$$R = \frac{V_{in}}{I_{in}} = \frac{L}{2\mu_n C_{ox} W (V_C - V_T)}, \tag{2.95}$$

Equation (2.95) is true when both NMOS transistors remain in saturation region, which is true if $|V_{in}| \langle (V_C - V_T)$. The MOSFET resistor is useful for cases with high desired linearity but reduced circuit complexity. The price paid for this is however two control voltage sources (V_C) instead of one (Wang, 1990; Metin, Pal & Cicekoglu, 2010).

2.3 Comparison of The Nonlinearity Cancellation Techniques

For proper cancellation of even order distortion in the presented schemes, one would need perfect transistor matching. In practice, mismatches will induce some residual even order distortion. The dominant source for such mismatches appears to be threshold voltage mismatch. Although, in the filters $V_C - V_T$ can be large, thus reducing this effect and allowing matching as well as 0.1 to 0.5 percent for adjacent MOSFET resistors. Another nonideality is that the mobility μ is not really constant, but changes slightly with the terminal voltages. However, even order distortion is not really affected by this, odd order distortion can be somewhat different than expected by supposing μ is constant. Actually, the behavior of the circuits in Figure 2.4, Figure 2.5, Figure 2.6, Figure 2.11 and Figure 2.12 may be rather similar, especially if their distortion is dominated by even order terms due to mismatches. Connecting substrate to source, the odd nonlinearities are fully cancelled. Table 2 shows the cancellation features of the nonlinearity cancellation techniques which are mentioned above. The performance of these circuits and cancellation techniques 1, 2, 3, 8, 9 and 10 are so good due to the terminal voltages of the transistors. Figure 2.13 is suitable for high frequency oprerations due to operating in saturation region, but it requires two control voltages.

Table 2.1 Comparision of Nonlinearity Cancellation Techniques for γ=0

	Figure 2.4	Figure 2.5	Figure 2.6	Figure 2.7	Figure 2.8	Figure 2.9	Figure 2.10	Figure 2.11	Figure 2.12	Figure 2.13
Number of Transistors	1	2	2	1	2	2	2	4	2	2
Cancelling Odd Nonlinearities	Fully	Fully	Fully	Fully	Fully	Fully	Fully	Fully	Fully	Fully
Cancelling Even Nonlinearities	Fully	Fully	Fully	Not Fully	Not Fully	Not Fully	Not Fully	Fully	Fully	Fully

CHAPTER THREE
SUITABLE ACTIVE COMPONENTS FOR NONLINEARITY CANCELLATION TECHNIQUES

In this Chapter, suitable active components namely op-amp, operational transresistance amplifier, first generation current conveyor, second generation current conveyor, third generation current conveyor, inverting second generation curret conveyor, differential voltage current conveyor, differential difference current conveyor in IC technology for nonlinearity cancellation techniques are presented. The historical background, block diagram and terminal port relations of the components are given.

3.1 Operational Amplifiers

An op-amp is a high gain electronic voltage amplifier with differential inputs and, usually, a single output. The symbol of the op-amp with the associated terminals is shown in Figure 3.1.

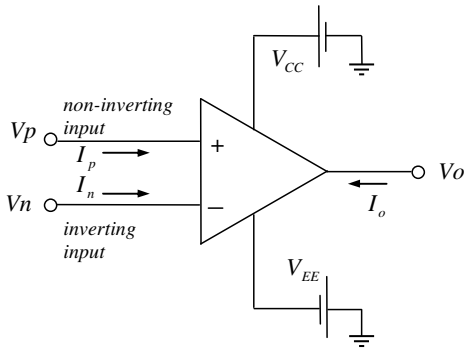

Figure 3.1 Symbol notation of op-amp

The power supply voltages V_{CC} and V_{EE} power the op-amp and generally define the output voltage range of the amplifier. The terminals, which are tagged with the "+" and the "-" signs, are called non-inverting and inverting inputs, respectively. The input voltage V_p and V_n and the output voltage V_o are referenced to ground.

The equivalent circuit model of an op-amp is shown in Figure 3.2.

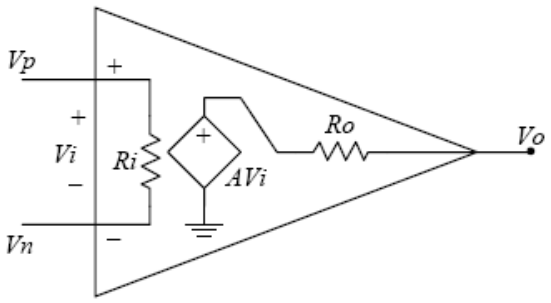

Figure 3.2 Equivalent circuit model of op-amp

The voltage V_i is the differential input voltage $V_i = V_p - V_n$. R_i is the input resistance of the device and R_o is the output resistance. The gain parameter A is called the open loop gain.

The output voltage is;

$$Vo = AVi = A(Vp - Vn) . \tag{3.1}$$

The ideal op-amp model is shown schematically in Figure 3.3.

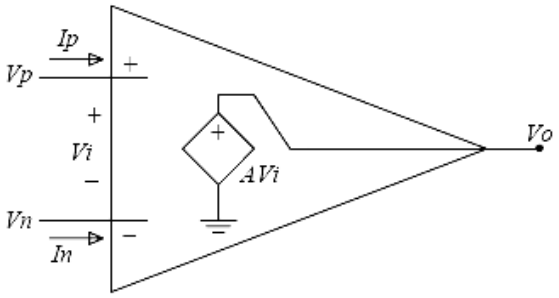

Figure 3.3 Ideal op-amp model

The ideal op-amp conditions in the negative feedback are;

$$\begin{aligned} &Vp = Vn \\ &Ip = In = 0 \\ &Ri \to \infty \quad . \\ &Ro = 0 \\ &A \to \infty \end{aligned} \tag{3.2}$$

The voltage transfer curve of the op-amp, which relates the output voltage to the input voltage, is shown in Figure 3.4.

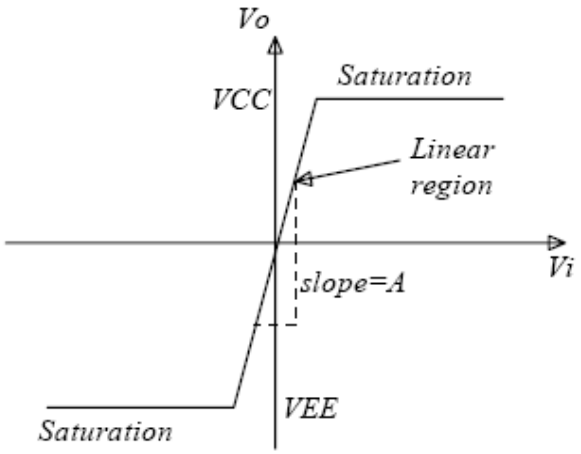

Figure 3.4 Op-amp voltage transfer characteristics

3.2 Current Conveyors

As an alternative active element to classical voltage mode op-amps current conveyor received great attention in recent years. The classical op-amp with its high input impedance and low output impedance is a suitable element for voltage mode circuits. However, the current conveyor (CC) has one high (ideally infinite) and one low (ideally zero) input impedance and one high output impedance. These properties make the current conveyor a suitable element for both voltage mode and current mode applications. The first current conveyor, named a first generation current conveyor (CCI) is a 3-port device, which was introduced by Smith and Sedra in 1968 (Smith & Sedra, 1968). Its block diagram representation is shown in Figure 3.5.

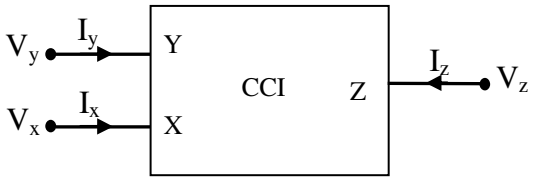

Figure 3.5 Circuit symbol of the CCI

In mathematical terms, CCI is described by the following matrix equation;

$$\begin{bmatrix} V_x \\ I_y \\ I_z \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_y \\ I_x \\ V_z \end{bmatrix}. \tag{3.3}$$

Taking the non-idealities of the CCI into account, the above hybrid equation can be rewritten as;

$$\begin{bmatrix} V_x \\ I_y \\ I_z \end{bmatrix} = \begin{bmatrix} \beta & 0 & 0 \\ 0 & 1 & 0 \\ 0 & \pm \alpha & 0 \end{bmatrix} \begin{bmatrix} V_y \\ I_x \\ V_z \end{bmatrix}. \tag{3.4}$$

In Equation (3.4), $\beta=1-\varepsilon_v$ is the voltage gain, and $\alpha=1-\varepsilon_i$ is the current gain of the CCI, where ε_v denotes the voltage tracking error between the X and Y terminals and ε_i denotes the current tracking error between the Z and X terminals. In Equation (3.3), the positive sign indicates the positive-type first generation current conveyor (CCI+) and the negative sign indicates the negative-type first generation current conveyor (CCI–).

CCI had distortion and accuracy limitations due to base current errors and output impedance restrictions (Wandsworth, 1990). Therefore, Sedra and Smith, (1970) introduced a more versatile building block named as the second generation current conveyor (CCII) that have different features over CCI. The block diagram representation of CCII is shown in Figure 3.6.

Figure 3.6 Circuit symbol of the CCII

The operation of the CCII can be characterized by the following equations;

$$\begin{bmatrix} I_y \\ V_x \\ I_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_y \\ I_x \\ V_z \end{bmatrix}. \tag{3.5}$$

Taking the non-idealities of the CCII into account, the above terminal equations can be rewritten as;

$$\begin{bmatrix} I_y \\ V_x \\ I_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ \beta & 0 & 0 \\ 0 & \pm \alpha & 0 \end{bmatrix} \begin{bmatrix} V_y \\ I_x \\ V_z \end{bmatrix}. \tag{3.6}$$

The third generation current conveyor (CCIII) was introduced by Alain Fabre, (1995). The main difference between CCI, CCII and CCIII is relation between terminal Y and terminal X current. In CCI, Y current is equal to X current in the same direction and in the CCII, there is no current flows in terminal Y. But in the CCIII, terminal Y current is equal to X terminal current in the opposite direction (Fabre, 1995). The block diagram representation of CCIII is shown in Figure 3.7 where the positive and negative signs define a positive and negative current conveyor, respectively.

Figure 3.7 Circuit symbol of the CCIII

The operation of the CCIII can be characterized by the following equations;

$$\begin{bmatrix} I_y \\ V_x \\ I_{z+} \\ I_{z-} \end{bmatrix} = \begin{bmatrix} 0 & -1 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & -1 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_y \\ I_x \\ V_{z+} \\ V_{z-} \end{bmatrix}. \tag{3.7}$$

Taking the non-idealities of the CCIII into account, the above terminal equations can be rewritten as;

$$\begin{bmatrix} I_y \\ V_x \\ I_{z+} \\ I_{z-} \end{bmatrix} = \begin{bmatrix} 0 & -1 & 0 & 0 \\ \beta & 0 & 0 & 0 \\ 0 & \alpha & 0 & 0 \\ 0 & -\alpha & 0 & 0 \end{bmatrix} \begin{bmatrix} V_y \\ I_x \\ V_{z+} \\ V_{z-} \end{bmatrix}. \tag{3.8}$$

In 1999, the inverting type current conveyor is introduced by Awad and Soliman, (1999), that exhibits an inverting property between the input terminal voltages. The circuit symbol of the second generation inverting current conveyor (ICCII) is shown in Figure 3.8,

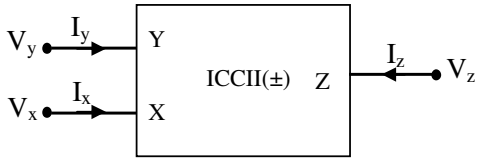

Figure 3.8 Circuit symbol of the ICCII

where the positive sign indicates the positive type inverting second generation current conveyor (ICCII+) and the negative sign indicates the negative type inverting second generation current conveyor (ICCII–).

The operation of the ICCII can be characterized by the following equations;

$$\begin{bmatrix} I_y \\ V_x \\ I_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ -1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_y \\ I_x \\ V_z \end{bmatrix}. \tag{3.9}$$

In non-ideal case, ICCII is characterized by the following port relations;

$$\begin{bmatrix} I_y \\ V_x \\ I_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ -\beta & 0 & 0 \\ 0 & \pm \alpha & 0 \end{bmatrix} \begin{bmatrix} V_y \\ I_x \\ V_z \end{bmatrix}. \tag{3.10}$$

3.3 Differential Voltage Current Conveyor

H. O. Elwan and A. M. Soliman proposed Differential Voltage Current Conveyor (DVCC), which is an extension of the CCII in 1997. CCII allowed opportunities to the designers as a versatile building block to implement many high performance circuits. On the other hand, CCII has only one input terminal with infinite impedance, so it does not allow the designers to perform circuits, which are supposed to handle differential inputs by using a single CCII (Elwan & Soliman, 1997). Moreover, one of the most productive dual CCII based amplifier circuits proposed in the literature, which is supposed to handle differential input signals despite its high common mode rejection ratio brings a disadvantage because of the non-zero input impedance of X terminal of CCII (Elwan & Soliman, 1997). For overcoming these disadvantages of having unique high impedance input terminal, DVCC was proposed.

DVCC is a five ports device, which is a versatile building block specifically designed for floating inputs, as depicted in Figure 3.9. So, it is formed up to have two distinct infinite impedance input terminals (Y_1 and Y_2), which allows no current flowing through Y terminals. DVCC has fundamentally designed for differential inputs. Therefore the potential difference between terminals Y_1 and Y_2 is equal to X terminal potential (Incekaraoglu, 2007).

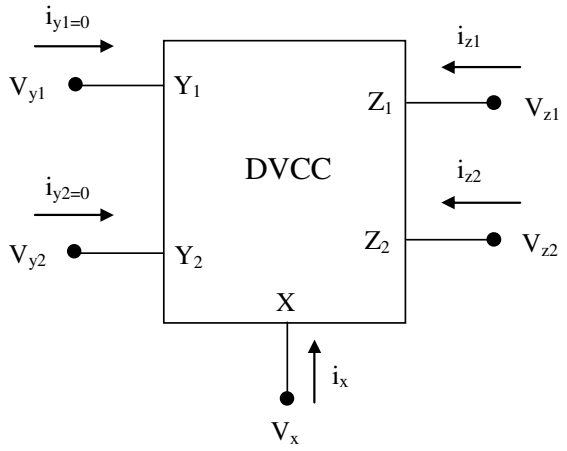

Figure 3.9 Circuit symbol of DVCC

The current, which flows through terminal X, is conveyed to the dual Z terminal. One of them is the same and the other one is inverse polarity, as shown in matrix Equation (3.11).

$$\begin{bmatrix} V_x \\ i_{y1} \\ i_{y2} \\ i_{z1} \\ i_{z2} \end{bmatrix} = \begin{bmatrix} 0 & 1 & -1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 \\ -1 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} i_x \\ V_{y1} \\ V_{y2} \\ V_{z1} \\ V_{z2} \end{bmatrix}. \tag{3.11}$$

3.4 Differential Difference Current Conveyor

Differential Difference Current Conveyor (DDCC) is introduced in 1996 by Chiu, Liu, Tsao and Chen. DDCC is a five port device as given in Figure 3.10. DDCC is designed to have three distinct infinite impedance input terminals (Y_1,Y_2 and Y_3) which allows no current flowing through Y terminals. X terminal has the equal potential to the potential difference between terminals Y_1 and Y_2 plus the potential of Y_3 (Chiu, Liu, Tsao & Chen, 1996). Relying on the common current conveying characteristic, current flowing through terminal X is conveyed to the Z terminal. DDCC is named as either DDCC+ or DDCC- depending on the polarity of the current flowing through Z terminal. In DDCC+, the current flowing through terminal

Z has the same polarity with the current flowing through X terminal, whereas in DDCC-, the current is conveyed from X terminal to Z terminal with an inverse polarity (Incekaraoglu, 2007).

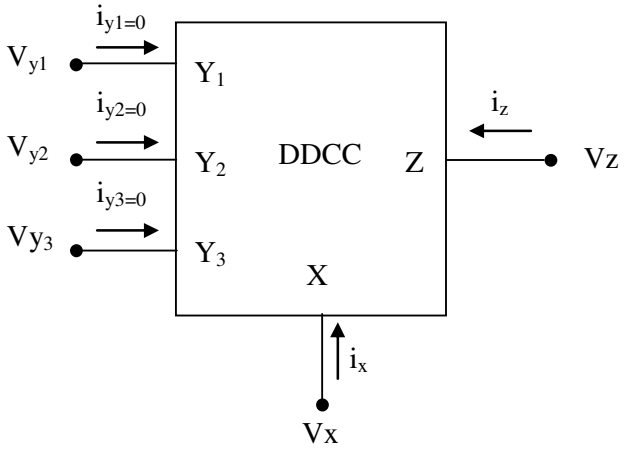

Figure 3.10 Circuit symbol of DDCC

The matrix representation of DDCC is given in Equation (3.12) (Chiu, Liu, Tsao & Chen, 1996).

$$\begin{bmatrix} V_x \\ i_{Y1} \\ i_{Y2} \\ i_{Y3} \\ i_Z \end{bmatrix} = \begin{bmatrix} 0 & 1 & -1 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ \pm 1 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} i_X \\ V_{Y1} \\ V_{Y2} \\ V_{Y3} \\ V_Z \end{bmatrix}. \tag{3.12}$$

All of the above mentioned conveyors and the derived conveyor types have been used in construction of many complex circuits and systems so far. Today, current conveyor can be considered as one of the most famous building blocks for analog integrated circuit and system design.

3.5 Operational Transresistance Amplifier

OTRA is a high gain current input, voltage output device. The circuit symbol of the OTRA is illustrated in Figure 3.11.

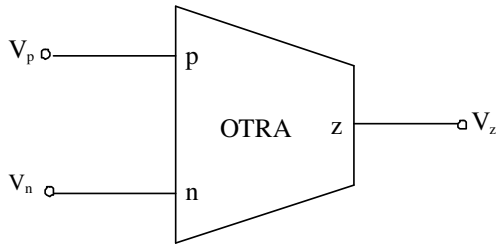

Figure 3.11 Circuit symbol of the OTRA

The operation of the OTRA can be characterized by the following equations;

$$\begin{aligned} V_z &= R_m (I_p - I_n) \\ V_p &= V_n = 0 \end{aligned} \quad . \tag{3.13}$$

The OTRA, which is known also as current differencing amplifier or Norton amplifier, is an important active element in analog ICs and systems. Both input and output terminals of OTRA are characterized by low impedance, thereby eliminating response limitations incurred by capacitive time constants. Since the input terminals of OTRA are at ground potential, most effects of parasitic capacitances and resistances disappear. The output terminal of OTRA exhibits low impedance so that OTRA based voltage mode circuits can easily be cascaded without additional buffers. For ideal operation, the transresistance R_m approaches infinity forcing the input currents to be equal. Thus, the OTRA must be used in a feedback configuration in a way that is similar to the classical op-amp (Salama & Soliman, 1999a; Kılınç, 2006).

OTRA has the advantages of high slew rate and wide bandwidth due to the fact that it benefits from the current processing capabilities at the input terminals. On the

other hand, since its output terminal is characterized as low impedance, OTRA is suitable for voltage mode operations keeping the compatibility with existing signal processing circuits (Salama & Soliman, 1999a).

The first and second nonlinearity cancellation techniques can be used with ICCII, DDCC and DVCC. The opposite but same terminal voltage values can achieve by grounding the required ports of the DDCC and DVCC.

The third nonlinearity cancellation technique can be used with OP-AMP, OTRA, DDCC and DVCC. The source voltages of the NMOS transistors can be connect to the input terminals of the active elements which are mentioned above.

The fourth, fifth, sixth, seventh and tenth nonlinearity cancellation techniques can be used with CCs, OP-AMP and OTRA. These techniques need signal dependent control voltages.

The eighth and ninth nonlinearity cancellation techniques can be used with OP-AMP, OTRA, DDCC and DVCC.

The nonlinearity cancellation techniques which are used for grounded resistors can be used all active elements.

CHAPTER FOUR
COMPARING NONLINEARITY CANCELLATION TECHNIQUES WITH INTEGRATOR

In this chapter, performance comparison of mostly used four nonlinearity cancellation techniques, which are previously mentioned in Chapter 2, is presented. An integrator circuit was used for the comparison. All active components and capacitors used for integrator expect resistors are ideal. The resistors are implemented via MOS transistors. Thus, only MOS transistors affect the linearity of the integrator circuit. Transient, THD and frequency analyses of the MOS transistors are compared. In all of the comparisons for integrators, the same input signal (V_{in}) of amplitude 10mV and 1.2 MHz frequency are used. PSPICE simulation program and 0.35μm TSMC MOSIS process model parameters are used for the analyses.

4.1 Op-Amp Based Integrators

4.1.1 Miller Integrator

The Miller integrator circuit active and passive components of which are ideal is shown in Figure 4.1. Applying input signal to integrator the output waveform is obtained as depicted in Figure 4.2.

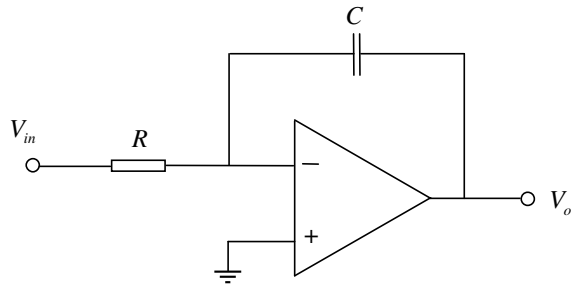

Figure 4.1 Miller integrator with ideal R

For an ideal integrator amplifier, the output voltage is written as;

$$V_{out} = -\frac{1}{RC}\int V_{in}\,dt\,. \tag{4.1}$$

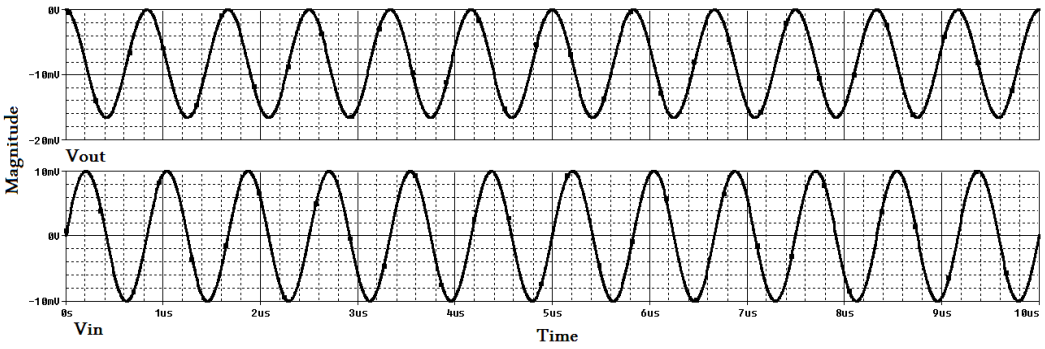

Figure 4.2 Output waveform of Miller integrator with ideal R

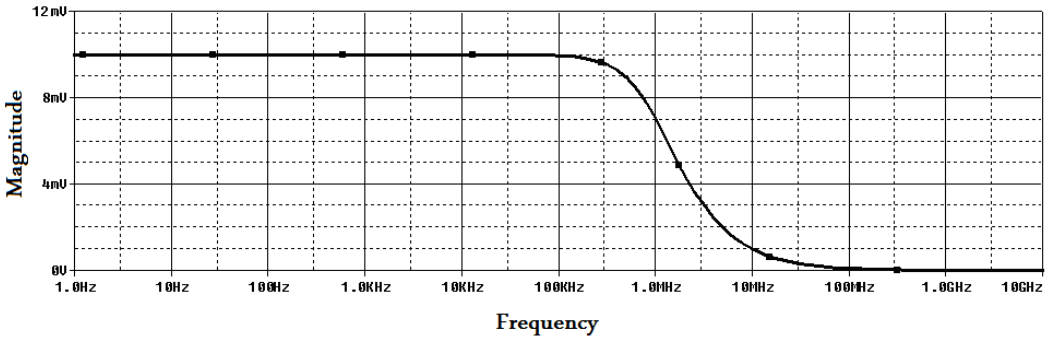

Figure 4.3 Frequency analysis of Miller integrator with ideal R

Figure 4.3 shows the frequency analysis of the Miller integrator amplifier with the output gain equal to 1. The resistor in Figure 4.1 can be implemented by two NMOS transistors which are previously expressed in Section 2.2.6. Using the sixth implementation technique, the resistance value can be controlled via changing V_C voltage. So integrator parameters can be controlled electronically. Figure 4.4 shows the MOS-C realization of the Miller integrator with the sixth nonlinearity cancellation technique.

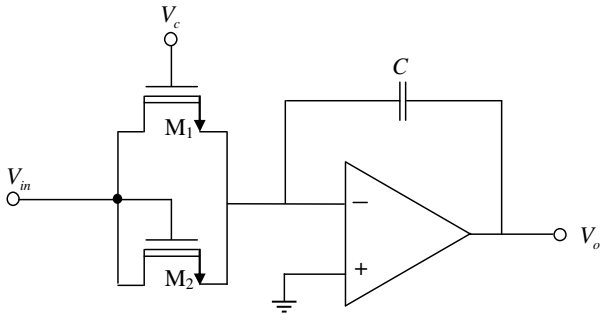

Figure 4.4 MOS-C realization of Miller integrator (Babanezhad & Temes, 1984)

Simulating MOS-C Miller integrator which is shown in Figure 4.4 with the input signal V_{in} the obtained output waveform is shown in Figure 4.5.

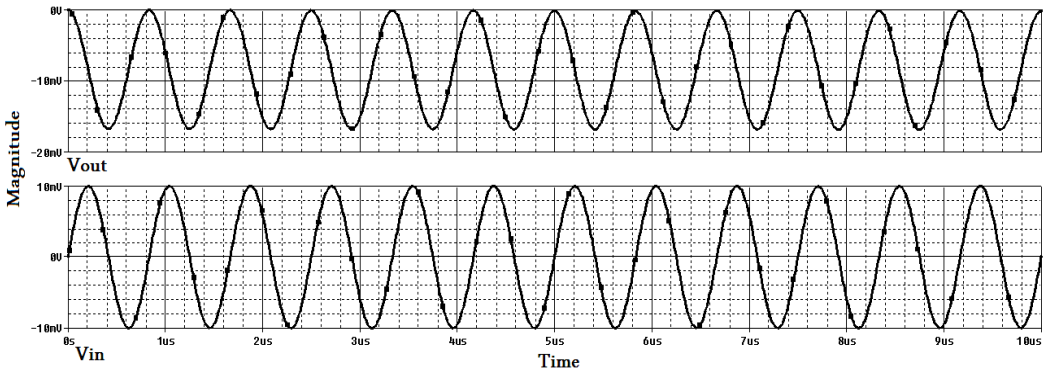

Figure 4.5 Output waveform of MOS-C Miller integrator

With the output gain equal to 1; the frequency analysis of the integrator, which is shown in Figure 4.4, is depicted in Figure 4.6.

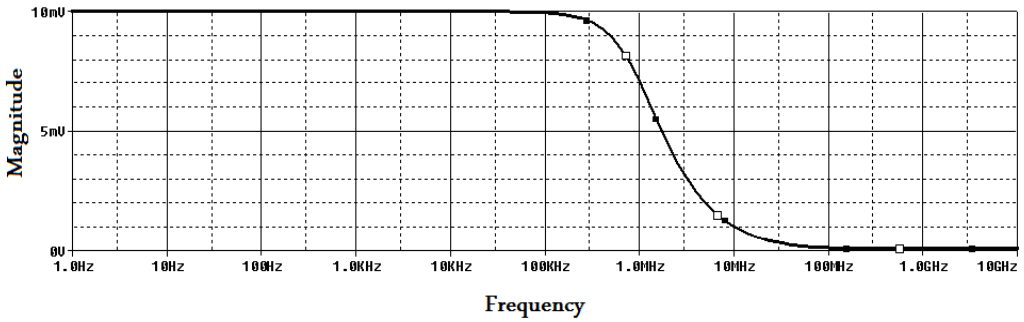

Figure 4.6 Frequency analysis of Miller integrator

4.1.2 Op-amp Integrator

Another op-amp based integrator circuit is shown in Figure 4.7 (Ismail, Smith & Beale, 1988). The circuit consists of two resistors suitable for realization with four NMOS transistors, two capacitors and an op-amp for an active element.

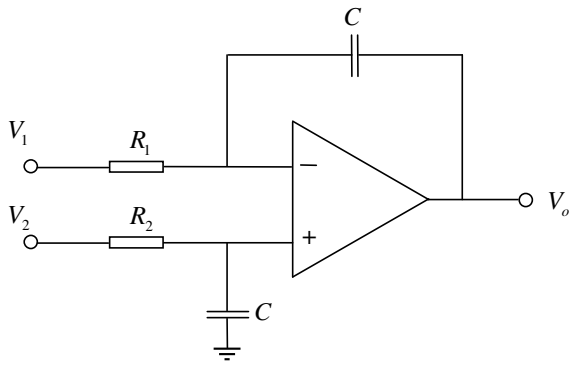

Figure 4.7 Op-amp based integrator circuit

If the resistors R_1 and R_2 are implemented via MOS transistors as mentioned in Section 2.2.8. The resultant MOS-C integrator becomes as depicted in Figure 4.8.

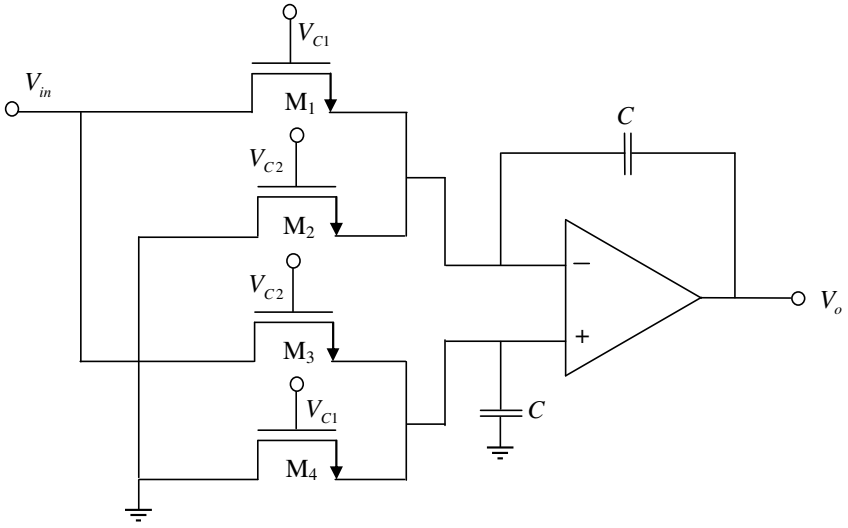

Figure 4.8 MOS-C realization of op-amp integrator circuit

Via changing gate voltages of NMOS transistors the resistance value and so integrator parameters can be changed electronically. Figure 4.9 shows the output waveform of the MOS-C op-amp integrator circuit shown in Figure 4.8. Input signal is given from the V_1 port and the V_2 port has been grounded.

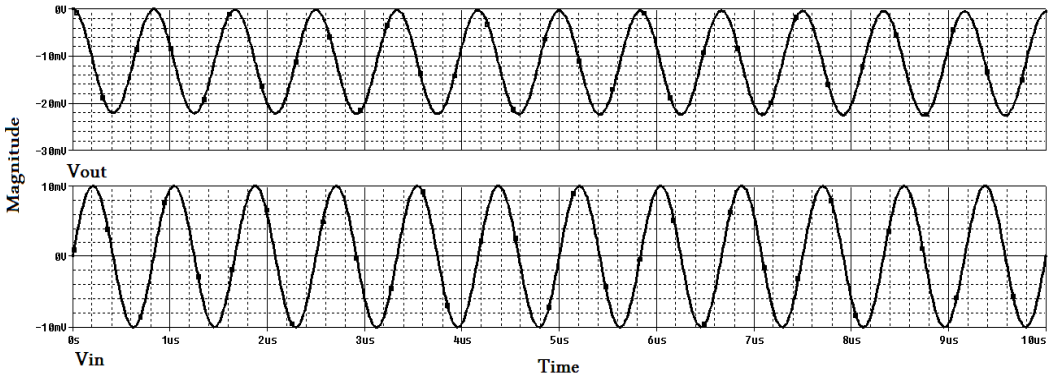

Figure 4.9 Output waveform of the MOS-C op-amp integrator

Figure 4.10 depicts the frequency analysis of the op-amp integrator shown in Figure 4.8 with the output gain equal to 1.

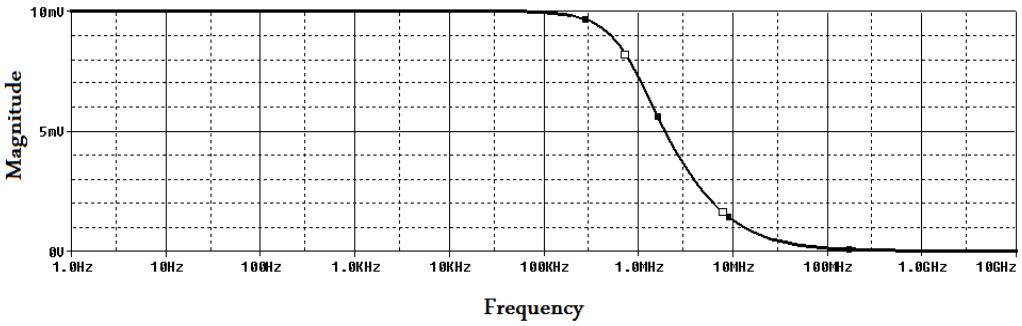

Figure 4.10 Frequency analysis of Op-amp. integrator

4.2 OTRA Based Integrator

An OTRA based integrator is shown in Figure 4.11.

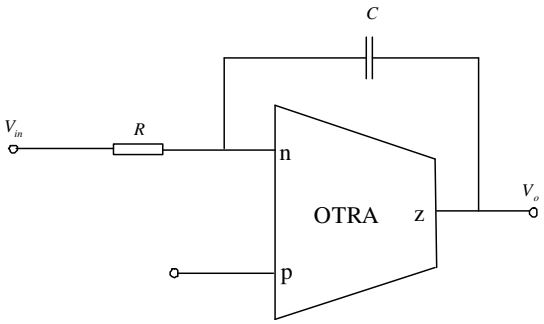

Figure 4.11 OTRA based integrator

Implementing the resistor with two matched MOS transistors as mentioned previously in Section 2.2.9, the OTRA based integrator becomes as Figure 4.12. Changing the gate voltages of the transistors M_1 and M_2 the tunable resistance value and integrator parameters can be obtained.

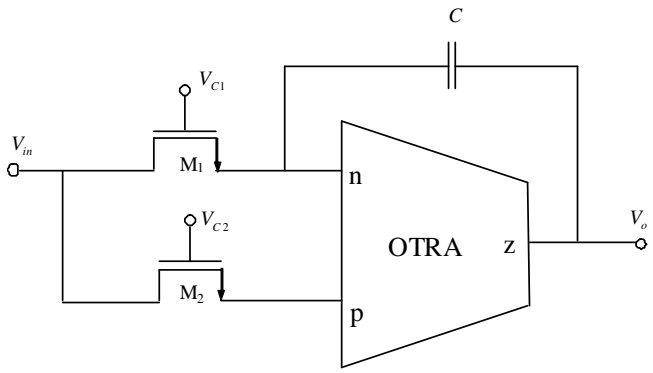

Figure 4.12 MOS-C realization of OTRA based integrator

Figure 4.13 depicts the output waveform of the MOS-C realization of OTRA based integrator with the input signal V_{in}. Figure 4.14 shows the frequency analysis of the OTRA based integrator with the output gain equal to 1.

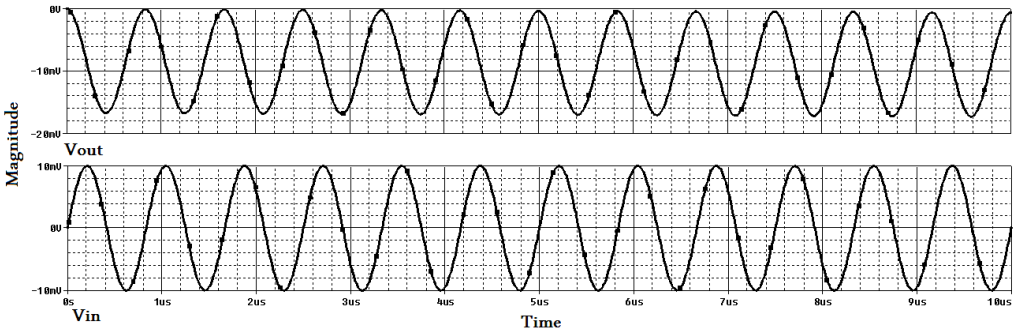

Figure 4.13 Output waveform of MOS-C integrator in Figure 4.12

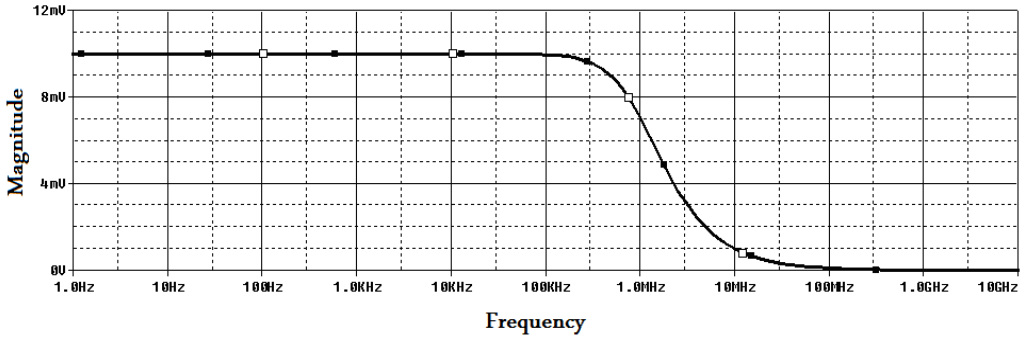

Figure 4.14 Frequency analysis of OTRA based integrator

4.3 ICCII Based Integrator

An ICCII based integrator is shown in Figure 4.15 (Toker & Zeki, 2007).

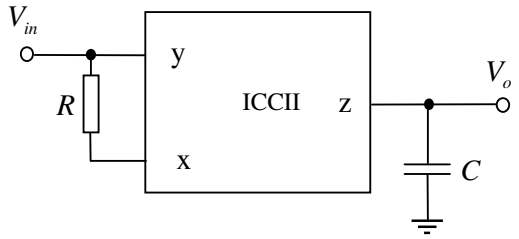

Figure 4.15 ICCII based integrator

Because of the input terminals of ICCII which are the same positive and negative voltages the resistor can be implemented easily using a MOS transistor. The MOS-C realization of the ICCII based integrator is shown in Figure 4.16. Resistor implementation technique was mentioned previously in Section 2.2.1.

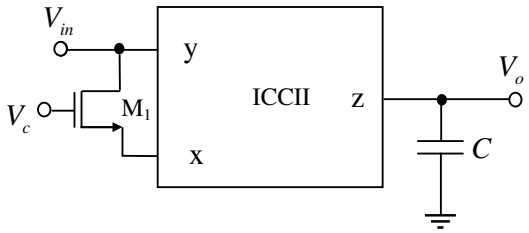

Figure 4.16 MOS-C realization of ICCII based integrator

Changing the gate voltage of the NMOS transistor electronically adjustable resistance and integrator parameters can be obtained. The output waveform of the MOS-C realization of ICCII based integrator is shown in Figure 4.17.

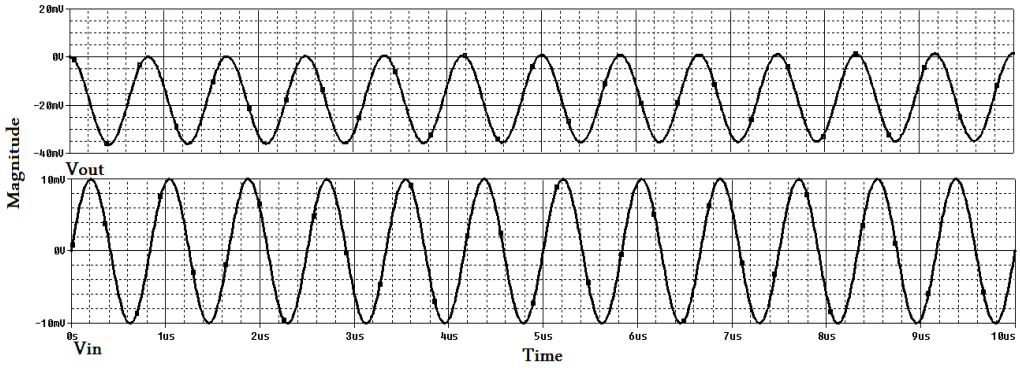

Figure 4.17 Output waveform of MOS-C ICCII based integrator

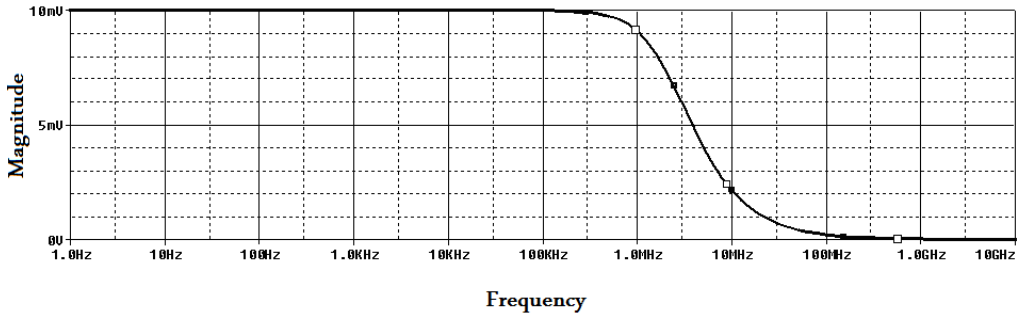

Figure 4.18 Frequency analysis of ICCII based integrator

With the output gain equal to 1; the frequency analysis of the ICCII based integrator is depicted in Figure 4.18.

4.4 Performance Comparison

In this section, performance comparison of the integrator is presented. The THDs of the integrators, which are mentioned above with the MOS-C realization techniques, are shown in Table 4.1. As seen in Table 4.1, Miller integrator has the best THD analysis performance. But the implementation technique, which is used for Miller integrator, is not suitable for higher frequencies.

Table 4.1. THD Analysis of the MOS-C based integrator amplifiers

	THD Analysis
Miller integrator	0.076%
Op-Amp. integrator	0.158%
OTRA based integrator	0.176%
ICCII based integrator	0.219%

The frequency analysis of the four integrators, which are mentioned above, is shown in Figure 4.19.

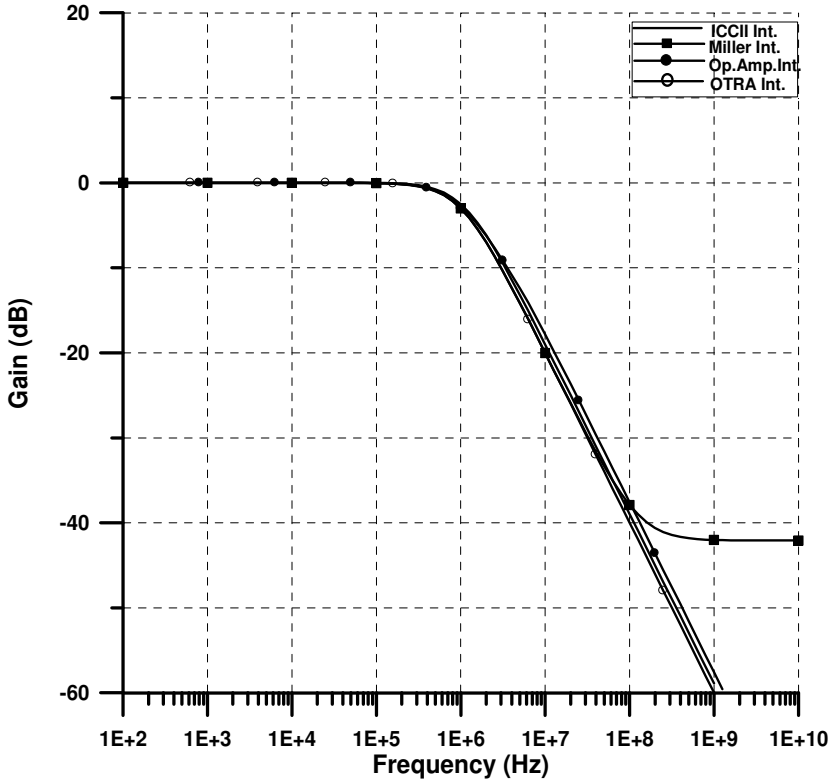

Figure 4.19 Frequency analysis of four integrators

CHAPTER FIVE
PROPOSED MOS-C BASED CIRCUITS

In this Chapter, new filter and oscillator topologies with MOS-C realization approach are presented. Chapter 5 started with two new first order allpass filters which include one active element. Then, three biquadratic filter configurations are presented. The second order lowpass, highpass, bandpass, and notch filters are realized using these biquadratic filter configurations. An electronically variable frequency oscillator configuration is obtained from the previously reported general configuration with a modification is modified. Tow Thomas and quadrature oscillator configurations are also given. The proposed configurations can be made fully integrated based on MOS-C realization. In addition, the proposed filters and oscillators have electronically tunable feature without affecting other critical parameters. The natural frequency and the quality factor are controllable independently. The CMOS equivalents of the active elements consist of MOS transistors. The ideal equivalents of active elements consist of only controlled sources.

5.1 First Order Allpass Filters

Filters are one of the necessary building blocks of many analog signal processing applications. Especially, first order filters are widely used in audio and video, as well as in many applications where the simplicity and power consumption are important parameters. Allpass (AP) filters are generally used for frequency-dependent delays yielding constant output amplitude over a desired frequency range. Other types of active circuits such as oscillators and high Q band pass filters are also realized by using allpass filters (Schauman & Van Valkenburg, 2001; Toker, Ozoguz, Cicekoglu & Acar, 2000).

A large number of first order allpass filter exist in the literature. Allpass filter based on op-amps are proposed in (Soliman, 1973). Op-amp based filters suffer from limited bandwidth performance.

Hereby, several allpass filters using active devices have been reported such as a CCII, (Soliman, 1997; Cicekoglu, Kuntman & Berk, 1999; Khan & Maheshwari, 2000; Horng, Hou, Chang, Chung, Liu & Lin, 2006), ICCII (Ibrahim, Kuntman, Ozcan & Çiçekoglu, 2004) CCIII (Maheshwari & Khan, 2001), DVCC (Minaei & Ibrahim, 2005), DDCC (Horng, Hou, Chang, Lin, Shiu & Chiu, 2006), OTRA (Cakir, Çam & Cicekoglu, 2005). Nevertheless, most of them lack an electronically controllable phase response. Some others have a phase response that is adjusted by a biasing current of the current conveyors (Pandey & Paul, 2004; Minaei & Cicekoglu, 2006; Maheshwari, 2005; Öztayfun, Kılınç, Çelebi, & Çam, 2008; Tangsrirat, Pukkalanun, & Surakampontorn, 2010). However, among the above mentioned studies do not include voltage controlled phase shifter.

5.1.1 First Topology for First Order Allpass Filter

A novel application of ICCII as a voltage controlled electronically tunable allpass filter is proposed. The proposed topology for the first order allpass filter is shown in Figure 5.1.

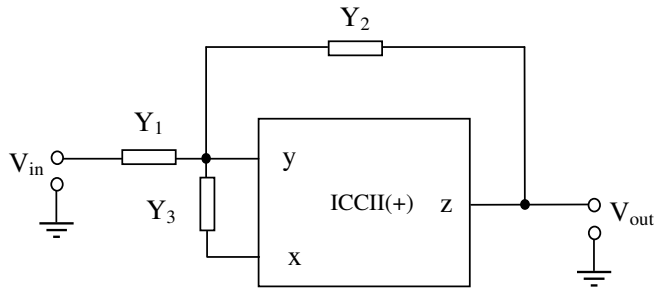

Figure 5.1 First order allpass filter topology

In ideal case, the transfer function of the proposed topology in Figure 5.1 is found as;

$$\frac{V_{out}}{V_{in}} = \frac{Y_1(Y_2 - 2Y_3)}{Y_2(Y_1 + 4Y_3)}. \tag{5.1}$$

Choosing appropriate admittances in Equation (5.1) as $Y_1=s2C$, $Y_2=sC$, $Y_3=G$, allpass filter response can be obtained as shown in Figure 5.2. Hereby, the proposed

allpass circuit employs ICCII(+), two capacitors and a resistor that is suitable for MOS realization.

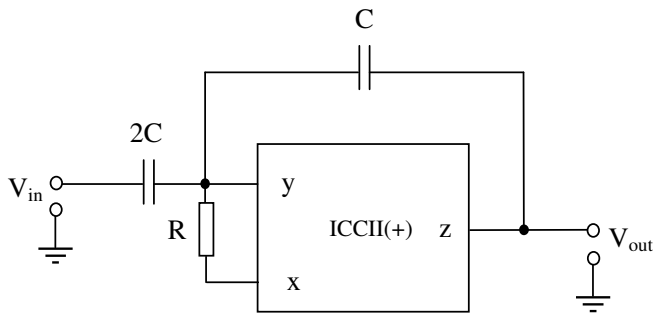

Figure 5.2 First order allpass filter configuration

Routine analysis yields the transfer function as;

$$\frac{V_{out}}{V_{in}} = \frac{s - \frac{2}{RC}}{s + \frac{2}{RC}}. \tag{5.2}$$

The natural frequency, ω_o, can be found as;

$$\omega_o = \frac{2}{RC}. \tag{5.3}$$

The phase response of the filter can be calculated as;

$$\varphi(\omega) = 180^o - 2\arctan(\omega/\omega_0). \tag{5.4}$$

In non-ideal case, ICCII is characterized by the following port relations;

$$I_y = 0, V_x = -\beta.V_y, I_z = \pm\alpha.Ix. \tag{5.5}$$

In Equation (5.5), $\beta=1-\varepsilon_v$ is the voltage gain, and $\alpha=1-\varepsilon_i$ is the current gain of the ICCII, where ε_v denotes the voltage tracking error between the X and Y terminals and ε_i denotes the current tracking error between the Z and X terminals. The voltage transfer function of the proposed topology is given for the ideal case previously. Taking the non-idealities of ICCIIs given in Equation (5.5) into account, the transfer function is recalculated as follows;

$$\frac{V_{out}}{V_{in}} = \frac{Y_1\left(Y_2 - Y_3(1+\alpha)\beta\right)}{Y_2\left(Y_1 + Y_3(1+\alpha)(1+\beta)\right)}. \tag{5.6}$$

For eliminating non-ideal effects of the ICCII, the capacitance values must be chosen as $Y_1=((1+\alpha).(1+\beta)).sC$ and $Y_2=((1+\alpha).\beta).sC$.

Tsividis, Banu & Khoury, (1986) gives a technique for the realization of MOS-C based circuits. That is, a resistor whose terminals connected to the same positive and negative voltage can easily be implemented using a MOS transistor with complete nonlinearity cancellation. This method, illustrated in Figure 5.3, cancels out the nonlinearity of the MOSFET significantly. The ICCII, which has the same positive and negative input terminals, introduced by Awad and Soliman (Awad & Soliman, 1999), is the best candidate for such type MOS-C realization.

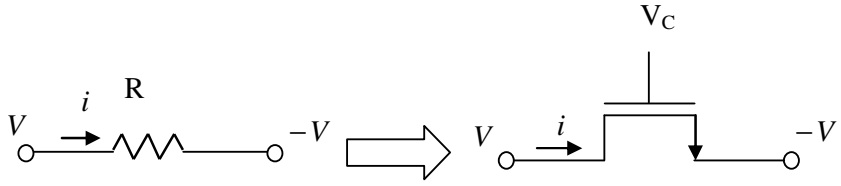

Figure 5.3 Nonlinearity cancellation in one NMOS transistor

The current i, which flows drain to source, is given by;

$$i = \frac{2V}{R}\ , \tag{5.7}$$

where of a MOSFET, R is given by;

$$R = \frac{1}{\mu_n C_{ox}(W/L)(V_c - V_T)}, \tag{5.8}$$

where W and L are the channel width and length, respectively and V_T is the threshold voltage of the MOSFET, μ_n is the free electron mobility in the channel and C_{ox} is the gate oxide capacitance per unit area. The MOSFET is tunable via V_C and since the even-order nonlinearities are cancelled out, it operates linearly over an extended voltage range.

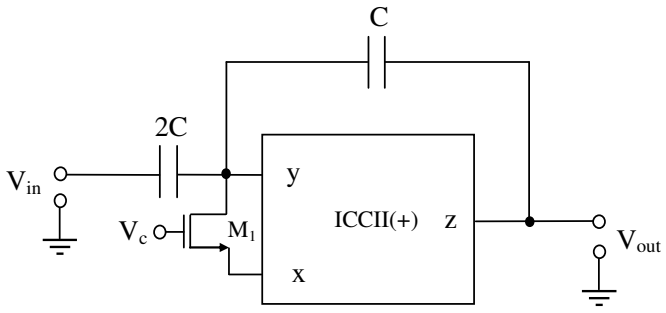

Figure 5.4 MOS-C realization of allpass filter in Figure 5.2

Figure 5.4 shows MOS-C realization of the proposed circuit. It is clear from Figure 5.4 that the phase response of the circuit can be controlled by gate voltage of the NMOS transistor.

The proposed first order allpass filter is constructed and simulated with PSPICE program. For SPICE simulations a CMOS realization of ICCII is used which is shown in Figure 5.5 with the same transistor aspect ratios as in (Ibrahim & Kuntman, 2002a).

In the simulation, MIETEC 0.5µm CMOS process model parameters are used. Supply voltages are taken as V_{DD} = 2.5V and V_{SS} = -2.5V. In the simulation, we take W=4.5µm and L=1.5µm for the resistor. We also take V_C=1.5V. Therefore, the resistor value is calculated as R≈2.94kΩ. The capacitor value is taken as C=50pF. From these values, the theoretical natural frequency is found as f_0≈2.16 MHz. The

simulated natural frequency is equal to $f_0 \approx 2.23$ MHz. For input signal of amplitude 0.1V and 2.16 MHz frequency, the THD is 0.91%.

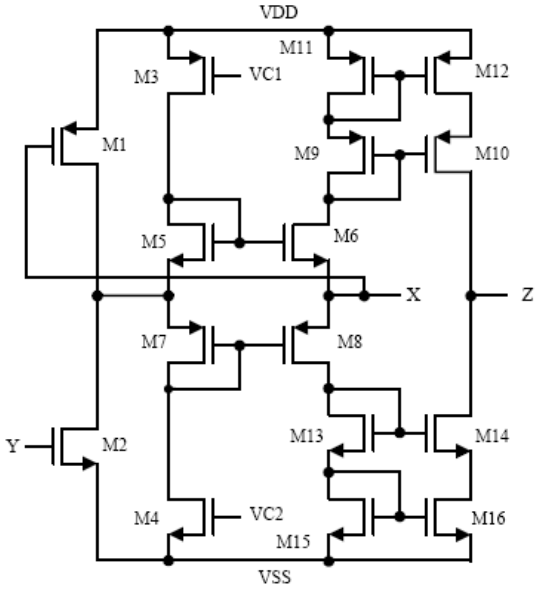

Figure 5.5 CMOS realization of ICCII (Ibrahim & Kuntman, 2002a)

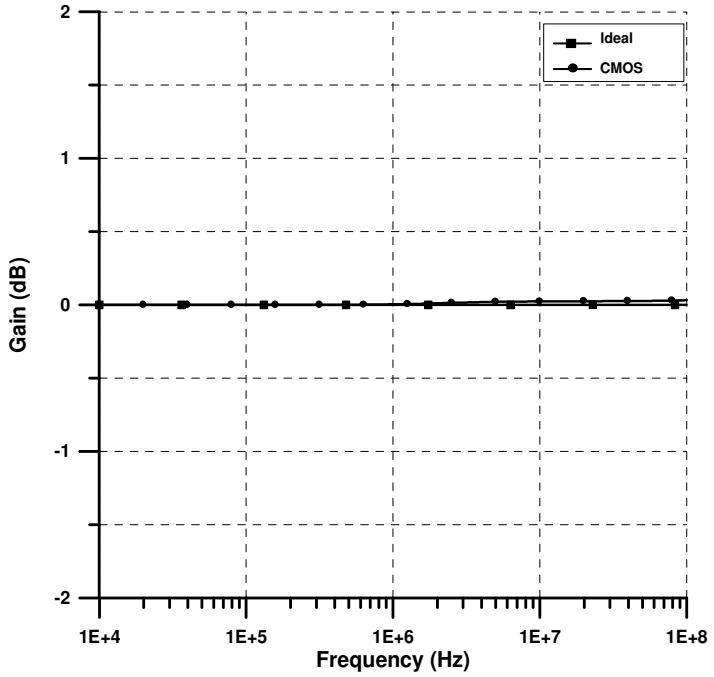

Figure 5.6 The magnitude response for allpass filter in Figure 5.2

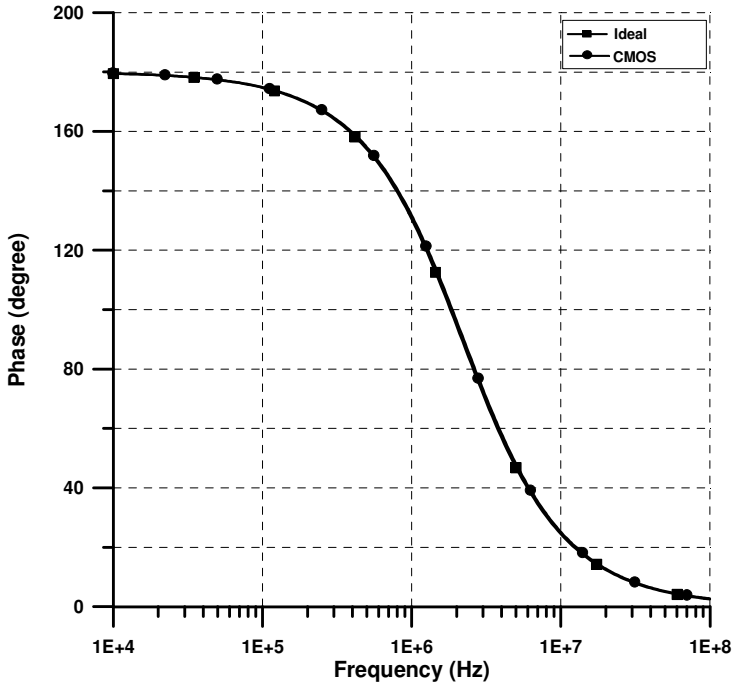

Figure 5.7 The phase response for allpass filter in Figure 5.2

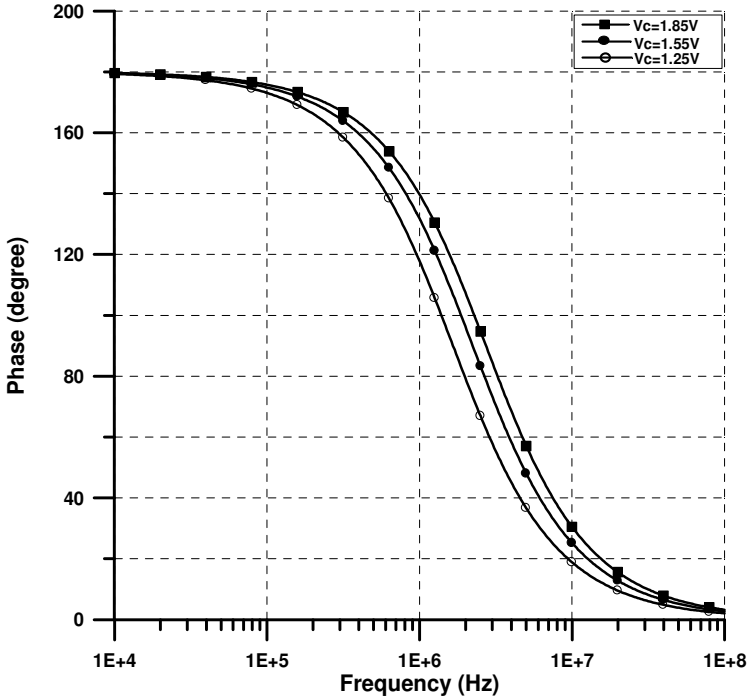

Figure 5.8 Electronically tunability feature for allpass filter in Figure 5.2

Simulated magnitude and phase responses of the proposed first-order allpass filter showing ideal and CMOS ICCII are given in Figures 5.6 and 5.7, respectively. Electronically tunability property of the proposed filter for different gate voltage values and corresponding phase responses are depicted in Figure 5.8.

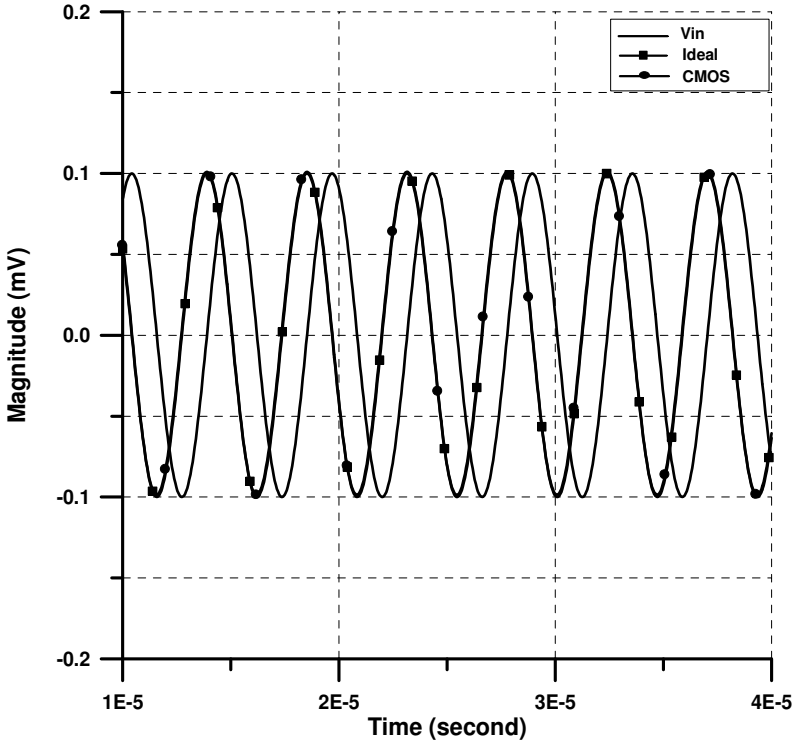

Figure 5.9 Time domain response for allpass filter in Figure 5.2

Figure 5.9 shows the time domain response of the proposed allpass filter. A sinusoidal input at a frequency of 2.16 MHz is applied to the allpass network constructed with the above mentioned passive element values. This causes a 0.115µs time delay at the output of the filter which corresponds to 89.03° phase differences. They are very close to the theoretical value that is equal to 90°. Figure 5.10 depicts operating frequency interval of the allpass filter.

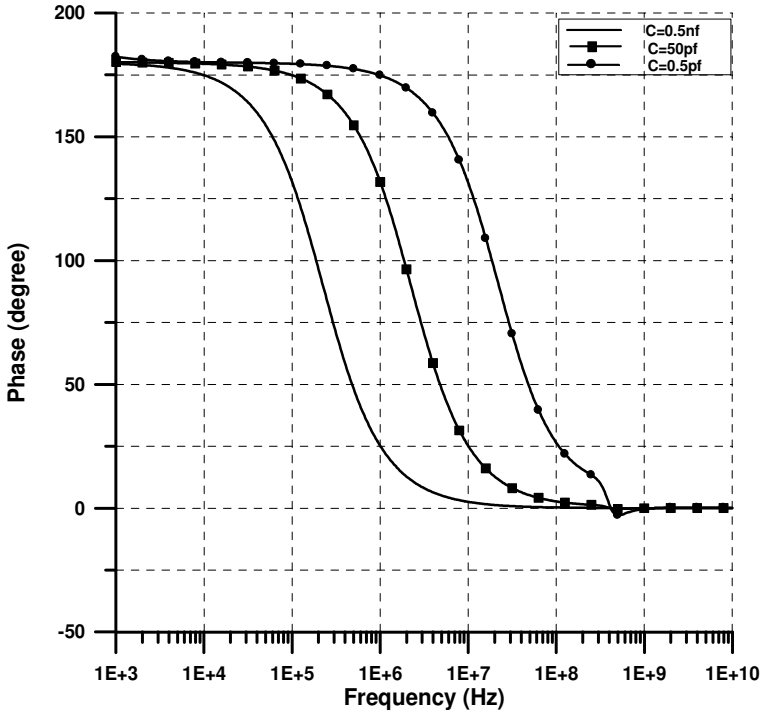

Figure 5.10 Operating frequency intervals for allpass filter in Figure 5.2

5.1.2 Second Topology for First Order Allpass Filter

In this section, a new first order allpass filter using ICCII is proposed (Gökçen & Çam, 2009b). The proposed circuit is suitable for MOS-C realization and consists of an ICCII, a capacitor and four NMOS transistors which are operated in triode region and depletion mode. The proposed topology is suitable for the electronically tunable phase frequency response.

Another method for canceling nonlinearities was proposed previously in Section 2.2.6 (Han & Park, 1984; Babanezhad & Temes, 1984). A linear resistor has been realized by using parallel connection of two depletion type NMOS transistors operated in the triode region as illustrated in Figure 5.11 (Han & Park, 1984).

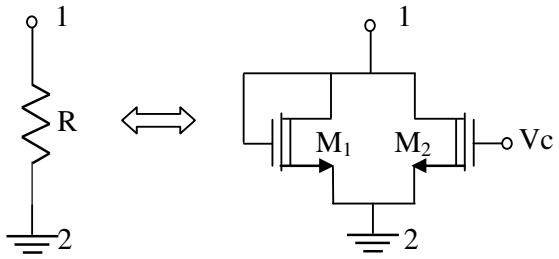

Figure 5.11 Nonlinearity cancellation technique in parallel connection of two NMOS

The circuit requires depletion mode devices to keep the M_1 transistor on. The equivalent resistance between terminal 1 and 2 is given by;

$$R = \frac{1}{\mu_n C_{ox}(W/L)(V_c - 2V_T)}, \tag{5.9}$$

which is controllable electronically by the gate voltage *Vc*. The proposed configuration for the first order allpass filter is shown in Figure 5.12.

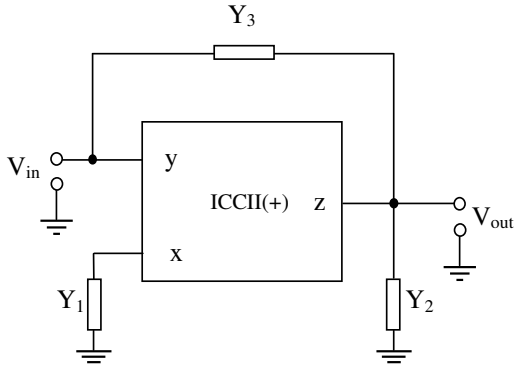

Figure 5.12 First order allpass filter topology II

The transfer function of the proposed first order allpass filter topology in Figure 5.12 is found as;

$$\frac{V_{out}}{V_{in}} = \frac{Y_3 - Y_1}{Y_3 + Y_2}. \tag{5.10}$$

Choosing appropriate admittances in Equation (5.10) as $Y_1=G$, $Y_2=G$, $Y_3=sC$, allpass filter response can be obtained as shown in Figure 5.13. Hereby, the proposed allpass circuit employs ICCII (+), a capacitor and two resistors that are suitable for MOS realization.

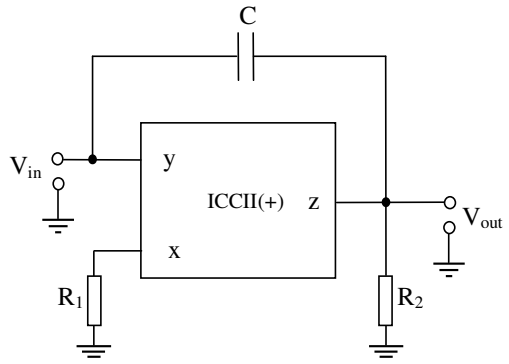

Figure 5.13 First order allpass filter configuration

To realize allpass filter feature, the resistance values of the proposed topology are chosen as following,

$$R_1 = R_2 . \tag{5.11}$$

Routine analysis yields the transfer function as;

$$\frac{V_{out}}{V_{in}} = \frac{sC - \frac{1}{R}}{sC + \frac{1}{R}} . \tag{5.12}$$

The natural frequency, ω_o, can be found as;

$$\omega_o = \frac{1}{RC} . \tag{5.13}$$

Figure 5.14 shows MOS-C realization of the proposed circuit.

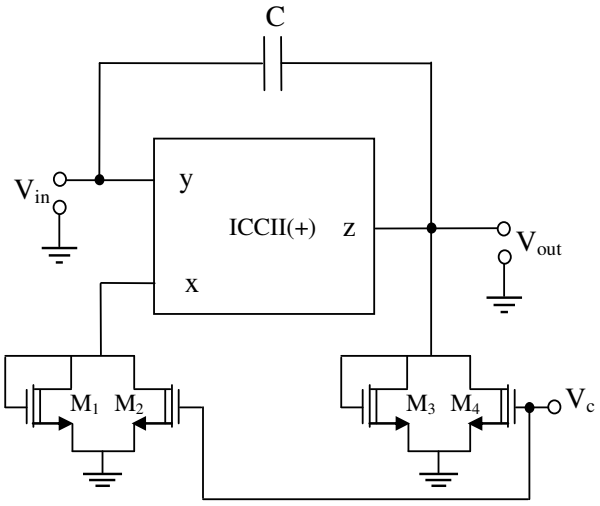

Figure 5.14 MOS-C realization of the allpass filter in Figure 5.13

Changing the gate voltages (*Vc*) of M_2 and M_4 transistors, the resistor values are changed and electronically controllable natural frequency are obtained. To provide Equation (5.11), both M_2 ve M_4 transistors gate voltages must be the same.

To verify the theoretical study, the first order allpass filter is constructed and simulated with PSPICE program. For SPICE simulations, CMOS ICCII is obtained from CMOS DDCC in (Ibrahim & Kuntman, 2002b) by grounding Y_1, Y_3 ports which is shown in Figure 5.15 and 0.35µm TSMC MOSIS process model parameters are used. Supply voltages are taken as V_{DD} = 2.5V and V_{SS} = -2.5V. We take W=25µm and L=15µm for the resistors. We also take V_C=7.5V. Therefore, the resistor value is calculated as R≈780Ω. The capacitor value is taken as C=1nF. From these values, the theoretical natural frequency is found as f_0≈204.05 KHz. The simulated natural frequency is equal to f_0≈208.5 KHz. For input signal of amplitude 0.1V and 204 KHz frequency, the THD is 0.312%.

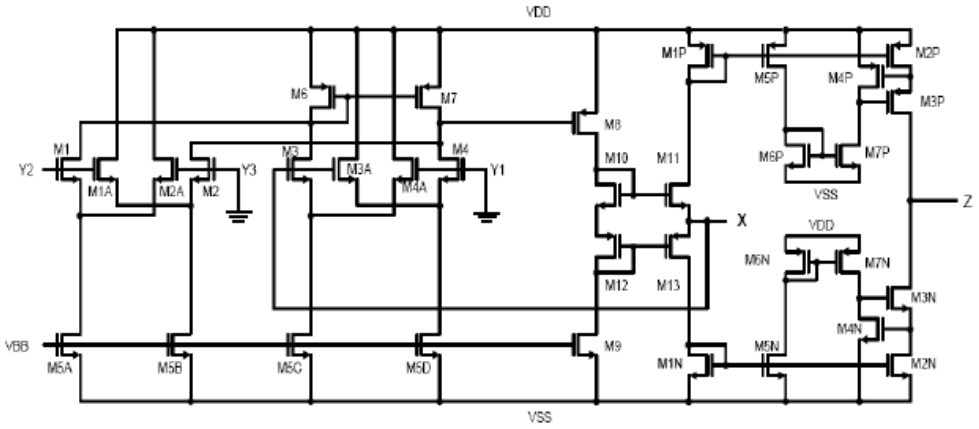

Figure 5.15 CMOS realization of DDCC based ICCII (Ibrahim & Kuntman, 2002b)

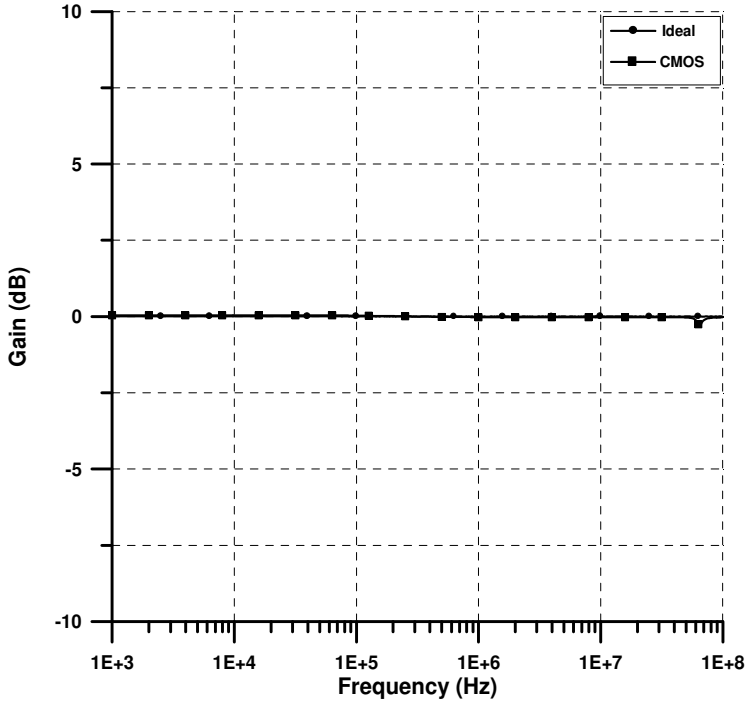

Figure 5.16 The magnitude response for allpass filter in Figure 5.13

Simulated magnitude and phase responses of the proposed first-order allpass filter are given in Figures 5.16 and 5.17, respectively. Electronically tunability property of the proposed filter for different gate voltage values and corresponding phase responses are depicted in Figure 5.18.

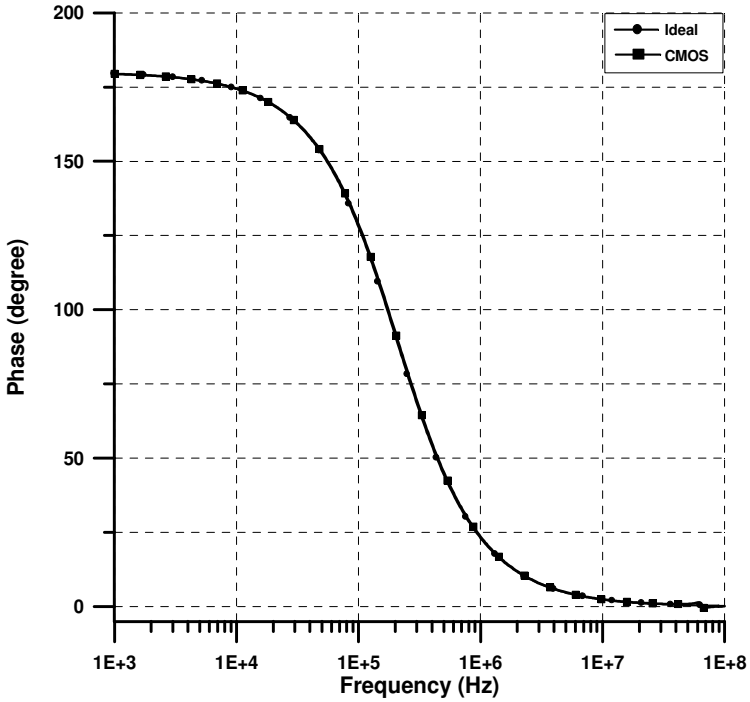

Figure 5.17 The phase response for allpass filter in Figure 5.13

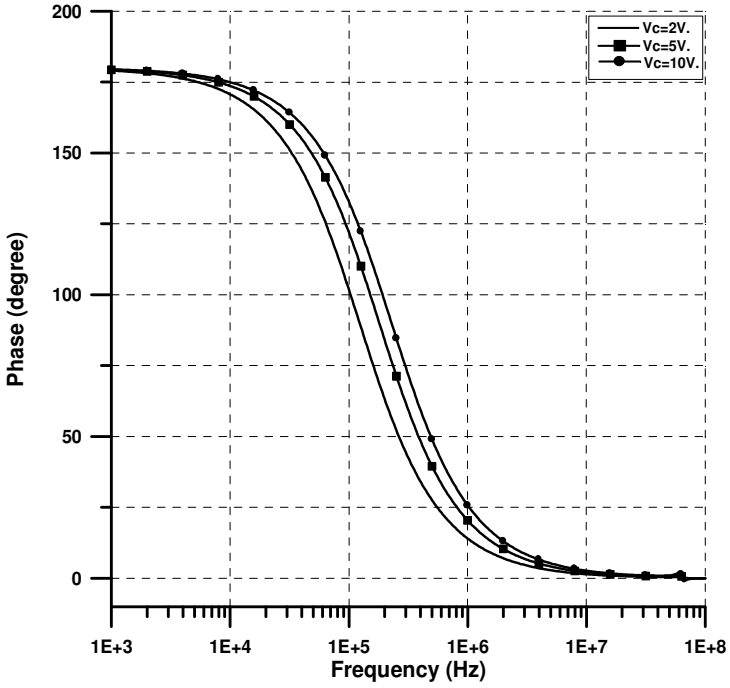

Figure 5.18 Electronically tunability feature for allpass filter in Figure 5.13

A sinusoidal input at a frequency of 204.05 KHz is applied to the allpass network constructed with above mentioned passive element values. This causes 1.25µs time delay at the outputs of the filter corresponding to 91.8º phase difference. This is very close to the theoretical value which is equal to 90º. Figure 5.20 shows operating frequency interval of the proposed circuit via changing capacitor values.

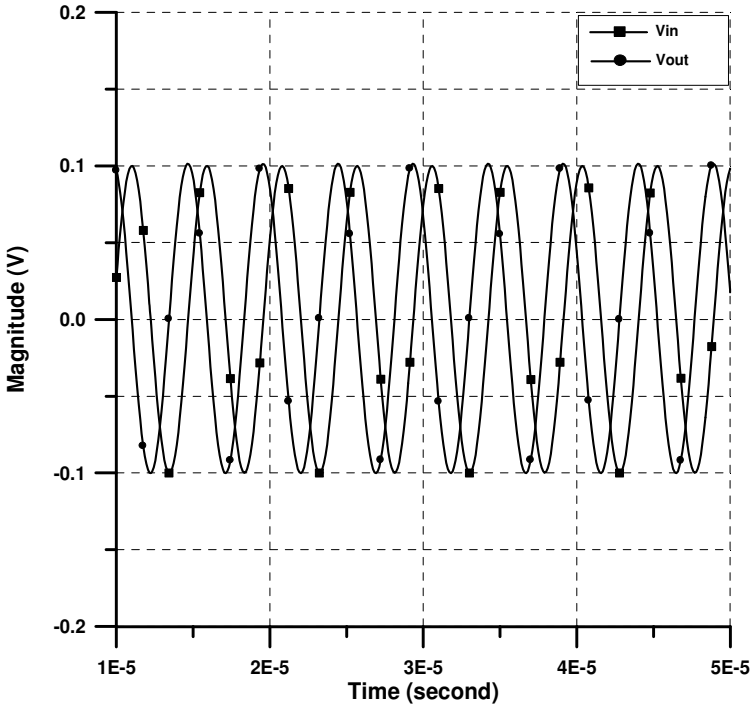

Figure 5.19 Transient response for allpass filter in Figure 5.13

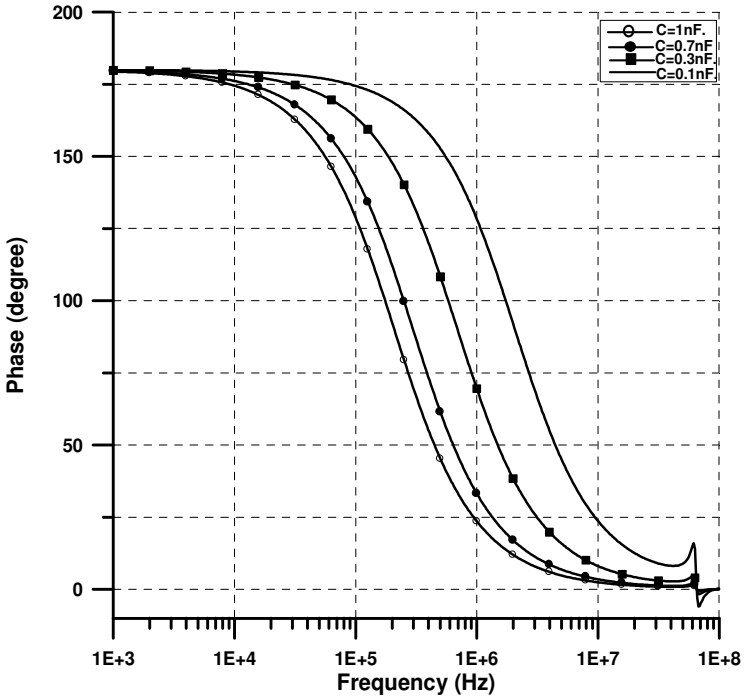

Figure 5.20 Operating frequency intervals for allpass filter in Figure 5.13

5.2 Single Amplifier Biquad

Active filters employing single active element are especially useful for applications where the power consumption is an important design constraint. Several voltage mode filters that use an active element rather than operational amplifier have been developed (Horng, Lay, Chang & Lee, 1997; Liu & Lee, 1996; Salama & Soliman, 2000a; Liu, Chen, Tsao & Tsay, 1993; Liu & Tsao, 1991) to overcome well-known op-amp limitations such as constant gain-bandwidth product, low slew rate, etc. Some of these filters use more than one active element (Horng, Lay, Chang & Lee, 1997; Liu & Lee, 1996; Salama & Soliman, 2000a). Some others, e.g. (Liu, Chen, Tsao & Tsay, 1993; Liu & Tsao, 1991) employ a single current follower or a single current conveyor which are unity-gain active elements. It has been shown in Chapter 4 that the internally grounded and current differencing input terminals of OTRA make MOS-C realization possible. In other words, the resistors connected to the input terminals of OTRA can easily be implemented using MOS transistors with

complete nonlinearity cancellation (Salama & Soliman, 1999a). The resulting circuit will consist of only MOS transistors and capacitors. This will save a significant amount of chip area and lead to circuits that are electronically tunable. That is, the resistance values and hence the related filter parameters can be adjusted by simply changing the bias (gate) voltages (Kılınç, 2006).

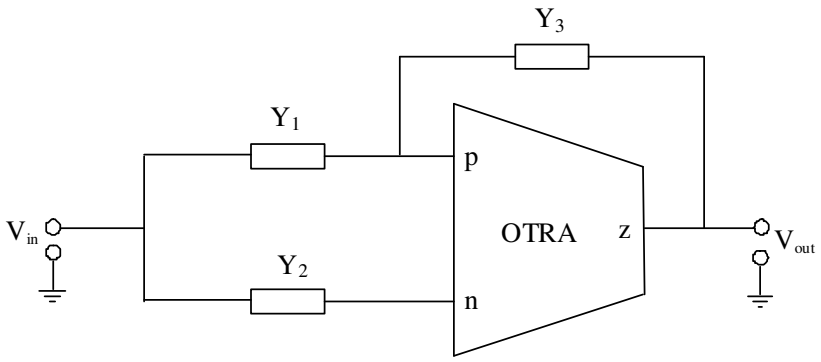

Figure 5.21 Single OTRA filter topology

The topology for the single OTRA biquad is shown in Figure 5.21 (Gökçen, Kılınç & Çam, 2007; Gökçen & Çam 2009a). Routine analysis yields the transfer function as;

$$\frac{V_{out}}{V_{in}} = \frac{Y_2 - Y_1}{Y_3}. \tag{5.14}$$

With proper selection of admittances in Equation (5.14), voltage mode second order lowpass (LP), highpass (HP), bandpass (BP) and notch filters can be realized as described below. The LP and HP filters need simple component matching to perform their functions. Voltage mode second order LP filter configuration of the proposed topology is depicted in Figure 5.22.

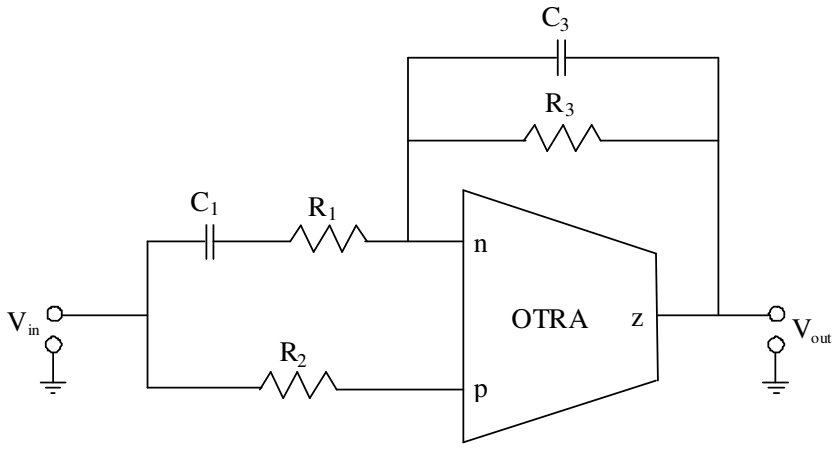

Figure 5.22 Voltage mode second order lowpass filter

For the following choices of admittances;

$$Y_1 = 1\Big/\left(\frac{1}{G_1}+\frac{1}{sC_1}\right),$$

$$Y_2 = G_2 = G_1,$$

$$Y_3 = G_3 + sC_3,$$

as shown in Figure 5.22, Equation (5.14) becomes;

$$T(s) = \frac{s(C_1G_2 - C_1G_1) + G_1G_2}{s^2C_1C_3 + s(C_1G_3 + C_3G_1) + G_1G_3}. \tag{5.15}$$

For $G_1 = G_2$, transfer function reduces to

$$T(s) = \frac{G_1G_2}{s^2C_1C_3 + s(C_1G_3 + C_3G_1) + G_1G_3}. \tag{5.16}$$

The natural frequency, the quality factor and the gain of the lowpass filter can be expressed as;

$$\omega_0 = \sqrt{\frac{G_1 G_3}{C_1 C_3}}, \tag{5.17}$$

$$Q = \frac{\sqrt{G_1 G_3 C_1 C_3}}{G_1 C_3 + G_3 C_1}, \tag{5.18}$$

$$K = \frac{G_1}{G_3}. \tag{5.19}$$

The OTRA is suitable for nonlinearity cancellation, as the two input terminals are virtually grounded. Assume that the two NMOS transistors, M_1 and M_2, shown in Figure 5.23, are matched and operating in the triode region. Since the transistors M_1 and M_2 have equal drain and source voltages, both even and odd nonlinearities are cancelled (Salama & Soliman, 1999a). Note that the equivalent resistance value, which appears between negative input terminal and output terminal of OTRA, is given as

$$R = \frac{1}{\mu_n C_{ox} (W/L)(V_a - V_b)}, \tag{5.20}$$

where V_a and V_b are the gate voltages.

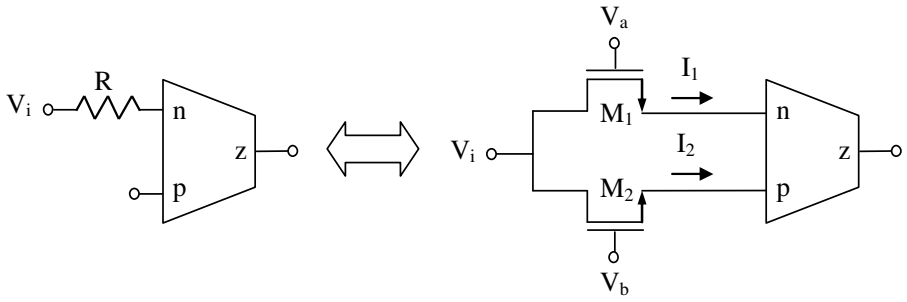

Figure 5.23 Realizing the resistor connected to the input terminal of OTRA with MOS transistors

Using this property of nonlinearity cancellation the resistors can be implemented by MOS transistors. Thus, the resultant circuit becomes suitable for MOS-C realization.

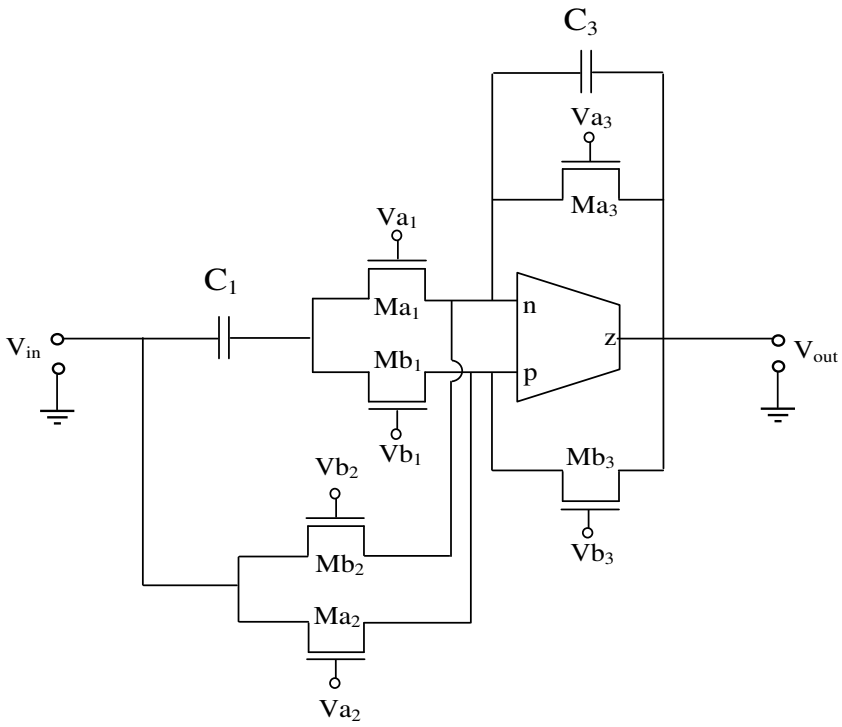

Figure 5.24 MOS-C realization of the voltage mode second order lowpass filter

The MOS-C realization of the voltage mode second order lowpass filter configuration is shown in Figure 5.24. Figure 5.25 shows the highpass filter configuration of the proposed topology.

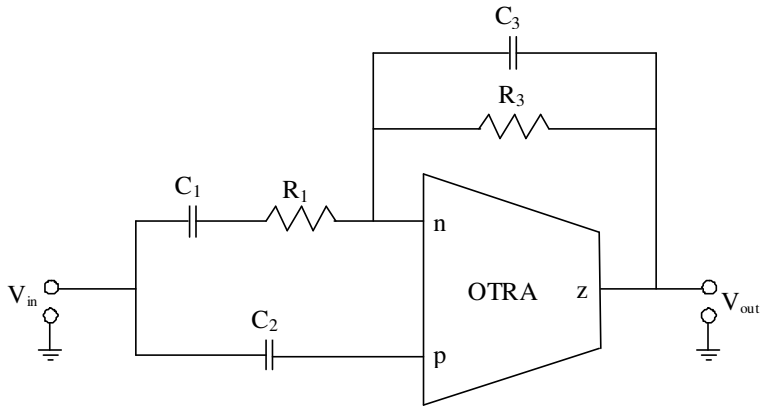

Figure 5.25 Voltage mode second order highpass filter

If admittances are chosen as;

$$Y_1 = 1\Big/\left(\frac{1}{G_1}+\frac{1}{sC_1}\right),$$

$$Y_2 = sC_2 = sC_1,$$

$$Y_3 = G_3 + sC_3,$$

the resultant circuit of which is shown in Figure 5.25, Equation (5.14) becomes;

$$T(s) = \frac{s^2C_1C_2 + s(C_2G_1 - C_1G_1)}{s^2C_1C_3 + s(C_3G_1 + C_1G_3) + G_1G_3}. \tag{5.21}$$

For $C_2 = C_1$, transfer function reduces to

$$T(s) = \frac{s^2C_1C_2}{s^2C_1C_3 + s(C_3G_1 + C_1G_3) + G_1G_3}. \tag{5.22}$$

The natural frequency, the quality factor and the gain of the highpass filter can be expressed as;

$$\omega_0 = \sqrt{\frac{G_1G_3}{C_1C_3}}, \tag{5.23}$$

$$Q = \frac{\sqrt{G_1G_3C_1C_3}}{G_1C_3 + G_3C_1}, \tag{5.24}$$

$$K = \frac{C_1}{C_3}. \tag{5.25}$$

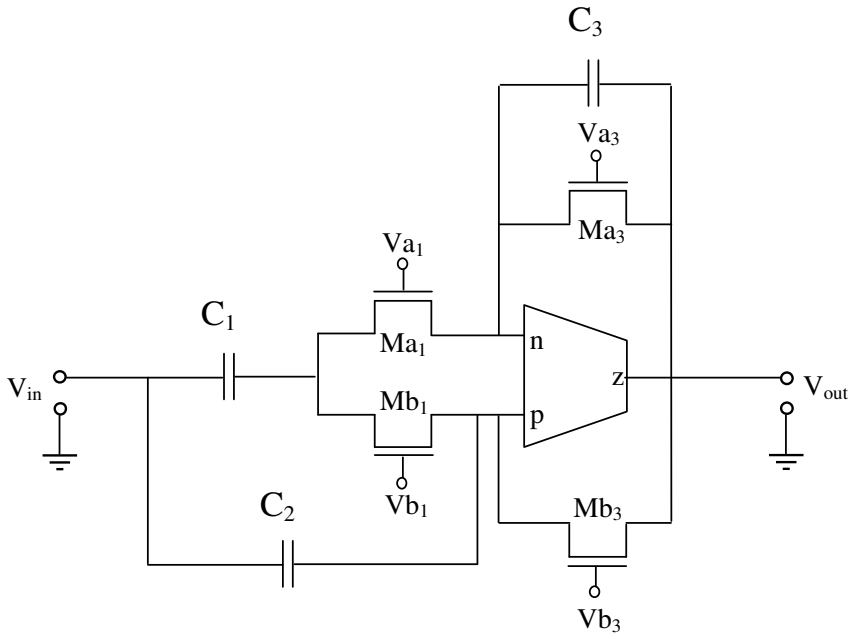

Figure 5.26 MOS-C realization of the voltage mode second order highpass filter

MOS-C realization of the voltage mode second order highpass filter configuration is shown in Figure 5.26. Bandpass filter configuration is shown in Figure 5.27.

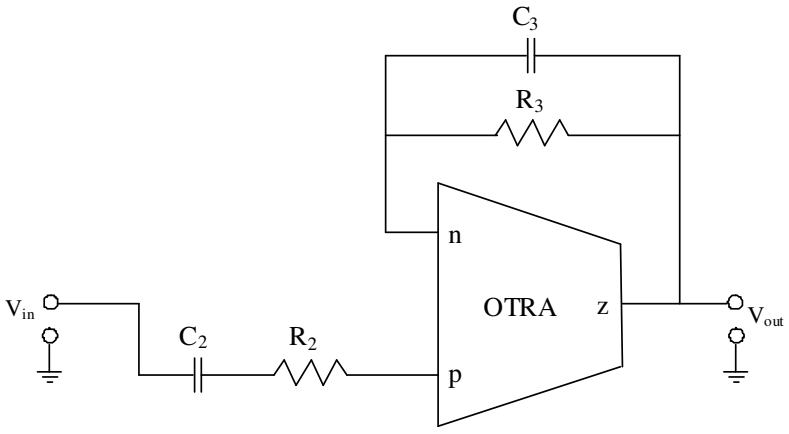

Figure 5.27 Voltage mode second order bandpass filter

If we choose the admittances as;

$$Y_1 = 0,$$

$$Y_2 = 1 \Big/ \left(\frac{1}{G_2} + \frac{1}{sC_2} \right),$$

$$Y_3 = G_3 + sC_3,$$

as shown in Figure 5.27, Equation (5.14) becomes;

$$T(s) = \frac{sC_2G_2}{s^2C_2C_3 + sC_2G_3 + sC_3G_2 + G_2G_3}. \tag{5.26}$$

Equation (5.26) can be written as;

$$T(s) = \frac{sC_2G_2}{s^2C_2C_3 + s(C_2G_3 + C_3G_2) + G_2G_3}. \tag{5.27}$$

The natural frequency, the quality factor and the gain of this bandpass filter can be expressed as

$$\omega_0 = \sqrt{\frac{G_2G_3}{C_2C_3}}, \tag{5.28}$$

$$Q = \frac{\sqrt{G_2G_3C_2C_3}}{G_2C_3 + G_3C_2}, \tag{5.29}$$

$$K = \frac{G_2C_2}{G_2C_3 + G_3C_2}. \tag{5.30}$$

MOS-C realization of the voltage mode second order bandpass filter configuration is depicted in Figure 5.28.

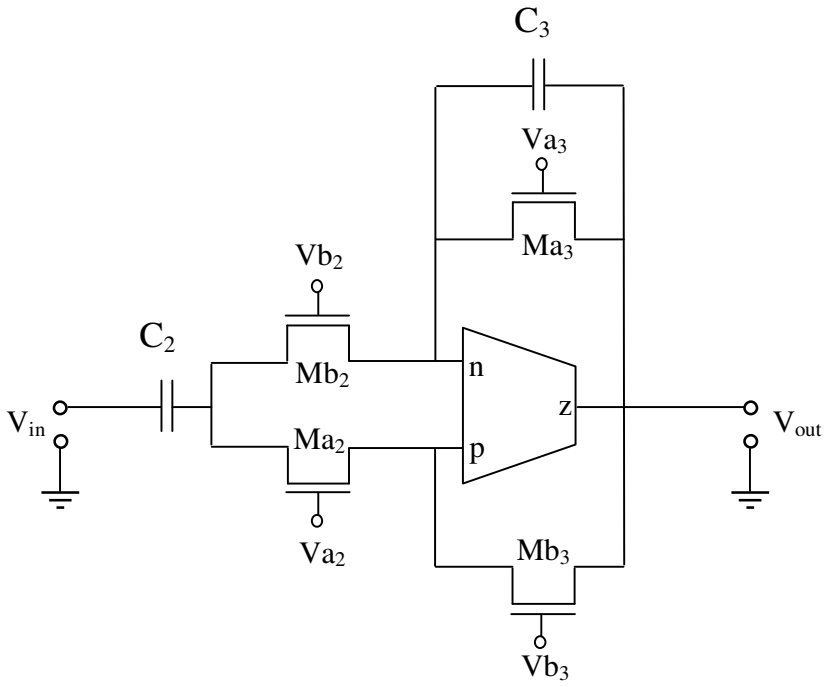

Figure 5.28 MOS-C realization of the voltage mode second order bandpass filter

Notch and allpass responses can be obtained using in the same circuit shown in Figure 5.29.

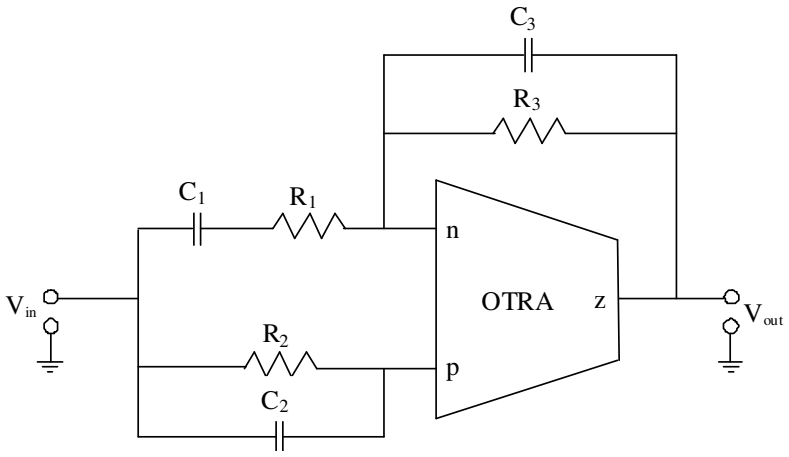

Figure 5.29 Voltage mode second order notch/allpass filter

In this circuit admittances are chosen as;

$$Y_1 = 1 \Big/ \left(\frac{1}{G_1} + \frac{1}{sC_1} \right),$$

$$Y_2 = G_2 + sC_2,$$

$$Y_3 = G_3 + sC_3 = G_2 + sC_2.$$

Also, the conditions for notch and allpass filters are $C_1G_2 + C_2G_1 = C_1G_1$ and $2(C_1G_2 + C_2G_1) = C_1G_1$, respectively.

Then, Equation (5.14) becomes;

$$T(s) = \frac{s^2C_1C_2 + s(C_1G_2 + C_2G_1 - C_1G_1) + G_1G_2}{s^2C_1C_3 + s(C_1G_3 + C_3G_1) + G_1G_3}. \tag{5.31}$$

For required condition transfer function reduces to

$$T(s) = \frac{s^2C_1C_2 + G_1G_2}{s^2C_1C_3 + s(C_1G_3 + C_3G_1) + G_1G_3}. \tag{5.32}$$

The natural frequency, the quality factor and the gain of the notch filter can be expressed as;

$$\omega_0 = \sqrt{\frac{G_1G_2}{C_1C_2}}, \tag{5.33}$$

$$Q = \frac{\sqrt{C_1C_2G_1G_2}}{C_1G_2 + C_2G_1}, \tag{5.34}$$

$$K = 1. \tag{5.35}$$

Figure 5.30 shows the MOS-C realization of the voltage mode second order notch/allpass filter.

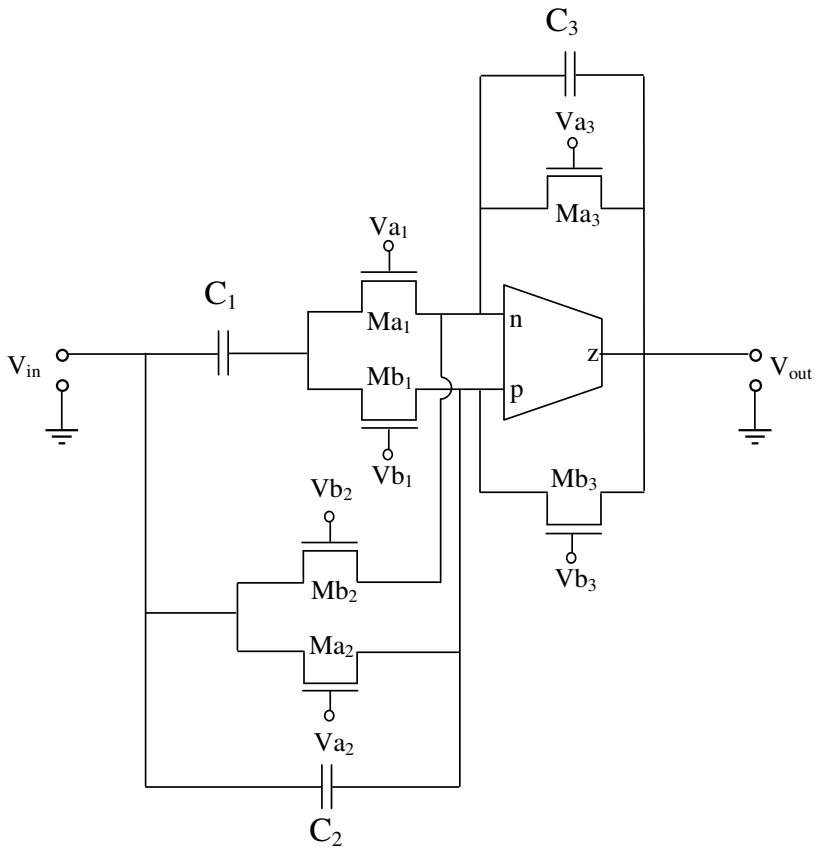

Figure 5.30 MOS-C realization of the voltage mode second order notch/allpass filter

The effects of the major non-idealities inherent in the OTRA on the presented filters are considered and self compensation introduced in (Salama & Soliman, 1999b) is employed for high frequencies. Considering a single pole model for the transresistance gain, R_m, then

$$R_m(s) = \frac{R_0}{1 + \dfrac{s}{\omega_0}}. \qquad (5.36)$$

For filter applications, which are intended for high frequencies, the transresistance gain, $R_m(s)$, reduces to;

$$R_m(s) \approx \frac{1}{sC_p}, \tag{5.37}$$

where $C_p = 1/(R_0\omega_0)$. Taking into account this effect, the transfer function in Equation (5.14) becomes;

$$\frac{V_{out}}{V_{in}} = \left(\frac{1}{sC_p + Y_3}\right) Y_2 - Y_1. \tag{5.38}$$

For complete compensation, the admittance Y_3 must contain capacitor branch. In that case the filters can be designed taking the magnitude of C_p into consideration, by subtracting its magnitude from the capacitance value in Y_3. Thus, the effect of C_p can be absorbed in the integrating capacitance without using any additional elements and achieving complete self compensation (Salama & Soliman, 1999b). All contain capacitor elements in the admittance Y_3 so the concept of self compensation is applicable to transfer function.

To verify the theoretical study, the presented filters were simulated by using PSPICE program. In the simulation AMI 1.2µm CMOS technology parameters are used. We take W = 14.4µm and L = 4.8µm for all transistors realizing the resistors. In these simulations chosen resistances and capacitances are;

All Pass: R_1=3233.33Ω, R_2=R_3=14078.37Ω, C_1=400pF, C_2=C_3=100pF.
Band Pass: R_2=5392Ω, R_3=4853Ω C_2=330pF, C_3= 33pF.
High Pass: R_1=R_3=9700Ω, C_1=C_2=C_3=47pF.
Low Pass: R_1=R_2=R_3= 9700Ω, C_1=C_3= 60pF.
Notch: R_1= 4409.09Ω, R_2=R_3=12125Ω, C_1=100pF, C_2=C_3=50pF.

These component values result in natural frequency of 331.83 KHz. The PSPICE simulations were performed using a CMOS realization of OTRA which is shown in

Figure 5.31 (Salama & Soliman, 1999a). The simulation results of circuits are given in Figure 5.32.

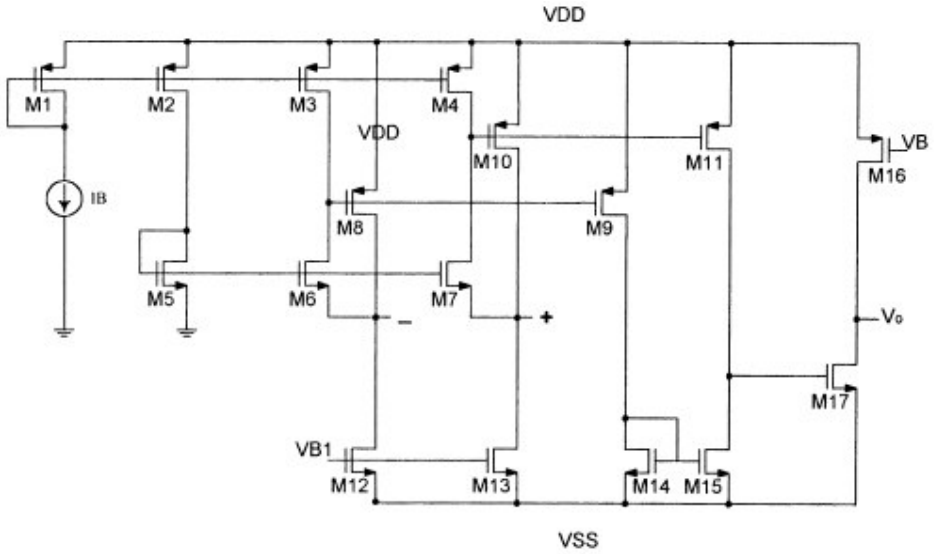

Figure 5.31 CMOS realization of OTRA (Salama & Soliman, 1999a)

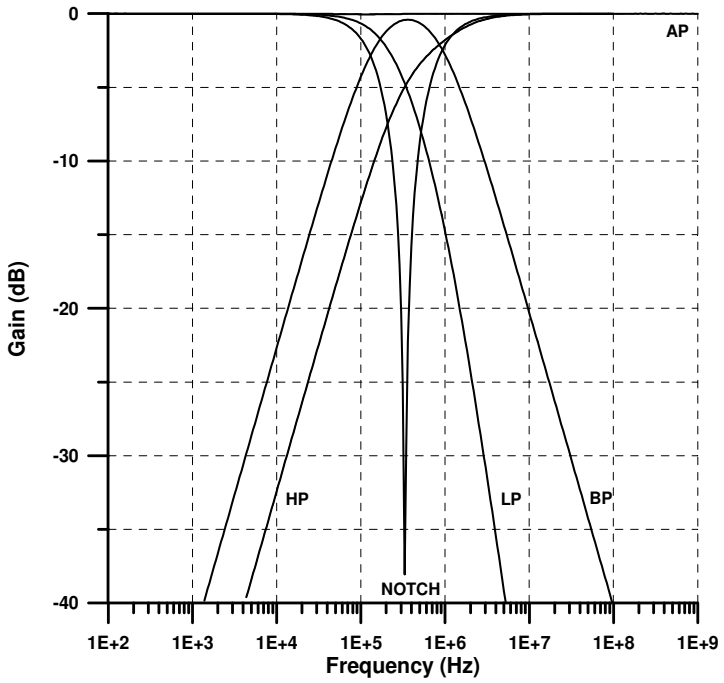

Figure 5.32 Simulation results of the single OTRA biquad

The electronically tunable feature of the lowpass (LP) filter is also evaluated and confirmed through PSPICE simulations. For this purpose, R_1, R_2, R_3 is changed by choosing the gate voltage V_{b3} as 2.0V, 1.8V, 1.6V and 1.4V while keeping V_{a3} at

2.3V. These voltages correspond to resistance values of 16.18kΩ, 9.7kΩ, 6.93kΩ and 5.39kΩ. Figure 5.33 shows the simulation results for the LP filter that demonstrates the electronically tunable feature. The simulated resonant frequencies are 215.444 KHz, 344.679 KHz, 456.954 KHz and 542.868 KHz, respectively. For input signal of amplitude 0.1V and 331 KHz frequency for band pass filter, the THD is 0.346%.

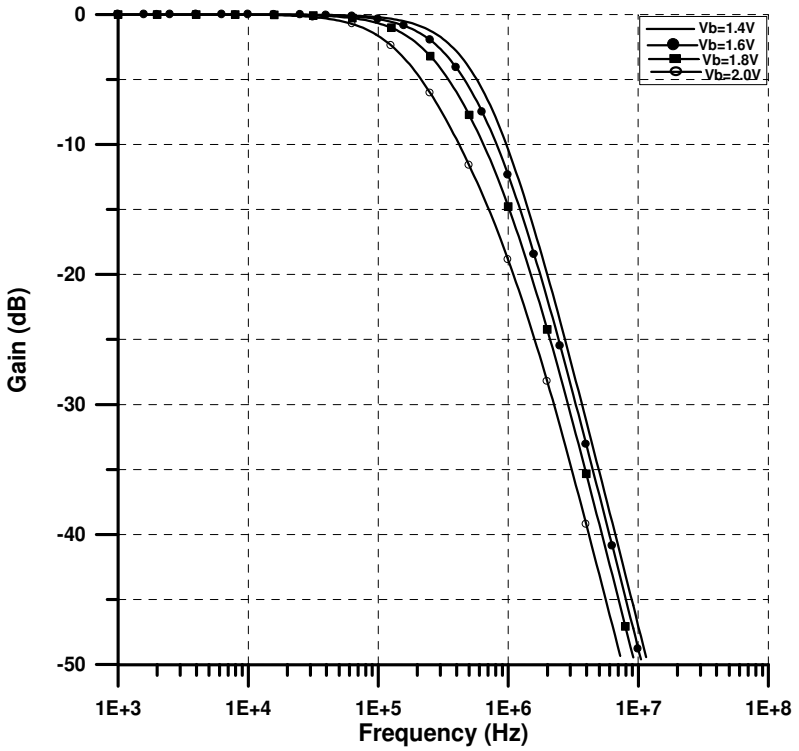

Figure 5.33 Electronically tunable feature for LP filter

5.3 The Fleischer-Tow Biquad

As discussed previously, many applications of OTRA have been reported in the literature (Salama & Soliman, 1999a; Chen, Tsao & Chen, 1992; Chen, Tsao, Liu & Chui, 1995; Elwan, Soliman & Ismail, 2001; Ravindran, Savla, Younus & Ismail, 2002; Salama & Soliman, 1999b; Salama & Soliman, 2000b; Çam, 2002; Çam, Kaçar, Cicekoglu, Kuntman & Kuntman, 2003; Kılınç & Çam, 2003; Çam, Cakir & Cicekoglu, 2004; Kılınç & Çam, 2005a; Kılınç & Çam, 2005b; Kılınç & Çam, 2006; Kılınç, Salama & Çam, 2006). They include universal filters, single resistance

controlled oscillators, immitance simulators, allpass filters. On the other hand, a literature survey shows that both Kerwin-Huelsman-Newcomb (KHN) and Tow-Thomas biquads are implemented using current conveyors, OTRAs, and OTAs (Salama & Soliman, 1999a; Kerwin, Huelsman & Newcomb, 1967; Thomas, 1971; Tow, 1968; Senani & Singh, 1995; Soliman, 1994; Shah & Bhaskar, 2002). However, Fleischer- Tow biquad, which is improved version of Tow-Thomas configuration, offers the realization of all five different second order filtering functions, namely lowpass, highpass, bandpass, notch and allpass (Fleischer & Tow, 1973).

Salama and Soliman have also introduced an OTRA based second order universal filter configuration besides the other circuits. It uses two active elements and thus it might be more desirable for low power applications. However, the filters derived from the topology in (Salama & Soliman, 1999a) have some disadvantages. One of them is that the circuits employ three dynamical elements, namely capacitors, to obtain second order transfer functions meaning that the filters are not canonical. Since capacitors occupy large silicon area on integrated circuits, the resulting filters would be disadvantageous for on-chip applications.

The proposed OTRA based Fleischer-Tow biquad, which uses two capacitors, has been presented for the realization of second order transfer functions. Therefore, the realized filters are canonical and occupy less area on the chip. Additionally, resonant frequency and quality factor of the filters can be controlled independently. All of the resistors used in the filters have been realized by MOS transistors. The resultant MOS-C implementation of OTRA based Fleischer-Tow biquad is suitable for fully integration (Gökçen, Kılınç & Çam, 2010).

The original op-amp based Fleischer-Tow biquad is given by Fleischer & Tow, (1973). The OTRA based equivalent of this configuration is shown in Figure 5.34. Routine analysis yields the transfer function as

$$\frac{V_o}{V_i} = -\frac{\frac{R_8}{R_6}s^2 + \frac{1}{R_1C_1}\left(\frac{R_8}{R_6} - \frac{R_1R_8}{R_4R_7}\right)s + \frac{R_8}{R_3R_5R_7C_1C_2}}{s^2 + \frac{1}{R_1C_1}s + \frac{1}{R_2R_3C_1C_2}\cdot\frac{R_8}{R_7}}. \tag{5.39}$$

The resonant frequency and quality factor are;

$$\omega_0 = \sqrt{\frac{R_8}{R_2R_3R_7C_1C_2}}, \tag{5.40}$$

$$Q = \frac{R_1C_1\sqrt{R_8}}{\sqrt{R_2R_3R_7C_1C_2}}. \tag{5.41}$$

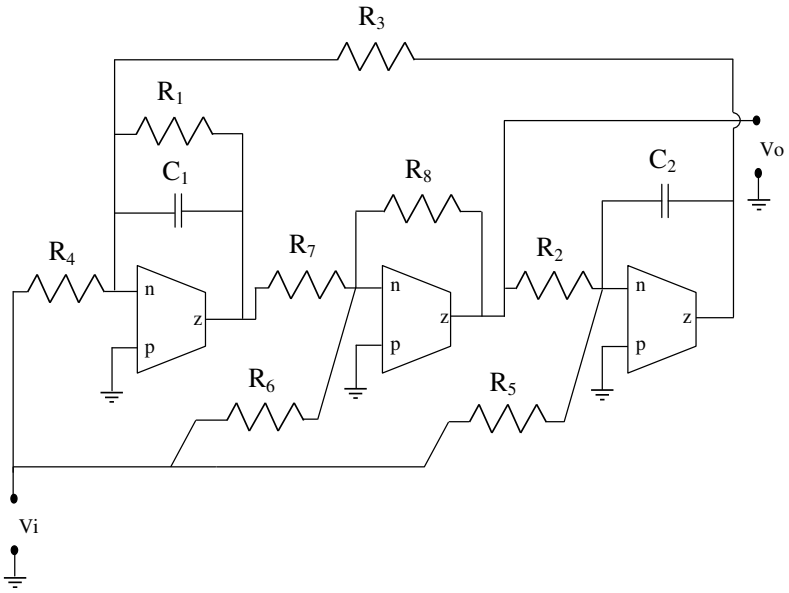

Figure 5.34 OTRA-RC based realization of the Fleischer-Tow Biquad

As it is seen from Equations (5.40) and (5.41), quality factor can be controlled without disturbing resonant frequency. Also, the sensitivity analysis reveals that sensitivities of filter parameters (Q and ω_0) to the passive component values are all less than unity in magnitude. The required condition to realize five basic filtering functions for the Fleischer-Tow Biquad is given in Table 5.1.

Table 5.1 Required conditions to realize five basic filtering functions for the Fleischer-Tow Biquad

Filter Type	Condition
Low-pass	$R_4 = \infty$, $R_6 = \infty$
High-pass	$R_4 = R_1$, $R_5 = \infty$, $R_6 = R_7 = R_8$
Band-pass	$R_4 = R_1$, $R_5 = \infty$, $R_6 = \infty$
Band-reject	$R_4 = \frac{R_6 R_1}{R_8}$, $R_7 = R_8$
All-pass	$R_4 = \frac{R_1}{2}$, $R_5 = R_2$, $R_6 = R_7 = R_8$

In practice, the transresistance gain is finite and more importantly it changes with frequency. The effects of this non-ideality inherent in the OTRA on the presented filters are considered. It has been seen that the methods to compensate these effects introduced in (Salama & Soliman, 1999a) are also applicable to the filters presented in this study. Considering a single pole model for the transresistance gain, R_m, then

$$R_m(s) = \frac{R_0}{1 + \frac{s}{\omega_0}} . \tag{5.42}$$

For filter applications, which are intended for high frequencies, the transresistance gain, R_m(s), reduces to

$$R_m(s) \approx \frac{1}{sC_p} , \tag{5.43}$$

where

$$C_p = \frac{1}{R_0 \omega_0} . \tag{5.44}$$

Taking into account this effect, the transfer function in Equation (5.39) becomes

$$\frac{V_o}{V_i} = -\frac{\frac{R_8}{R_6}(sC_1 + sC_p)(sC_2 + sC_p) + \left(\frac{R_8}{R_1R_6} - \frac{R_8}{R_4R_7}\right)(sC_2 + sC_p) + \frac{R_8}{R_3R_5R_7}}{(1 + sC_pR_8)(sC_1 + sC_p)(sC_2 + sC_p) + \frac{1}{R_1}(1 + sC_pR_8)(sC_2 + sC_p) + \frac{R_8}{R_2R_3R_7}} \quad (5.45)$$

As it is seen, the transfer function has been deteriorated due to non-ideal transresistance gain. The effect of this non-ideality can be compensated by connecting a capacitor, C_p, between the output terminal and the non-inverting terminal of the second OTRA placed in the middle (Salama & Soliman, 1999a). The effect of the stray capacitance, C_p, in the other two OTRAs having feedback capacitor branches can be absorbed in the capacitors C_1 and C_2 as it has been done in Salama & Soliman, (1999a). In other words, the filters can be designed taking the magnitude of C_p into consideration, by subtracting its magnitude from the capacitance values of C_1 and C_2. Thus, the effect of C_p can be absorbed in the integrating capacitances without using any additional elements and the complete self compensation (Salama & Soliman, 1999a) is achieved for the OTRAs at the left and right sides of the circuit. After these modifications, the circuit shown in Figure 5.35 has been obtained for compensating the effect of non-ideality. It can be shown that this circuit has the same transfer function as in Equation (5.39), which is the ideal one, and therefore the effect of non-ideal R_m is totally compensated with these slight changes in the circuit.

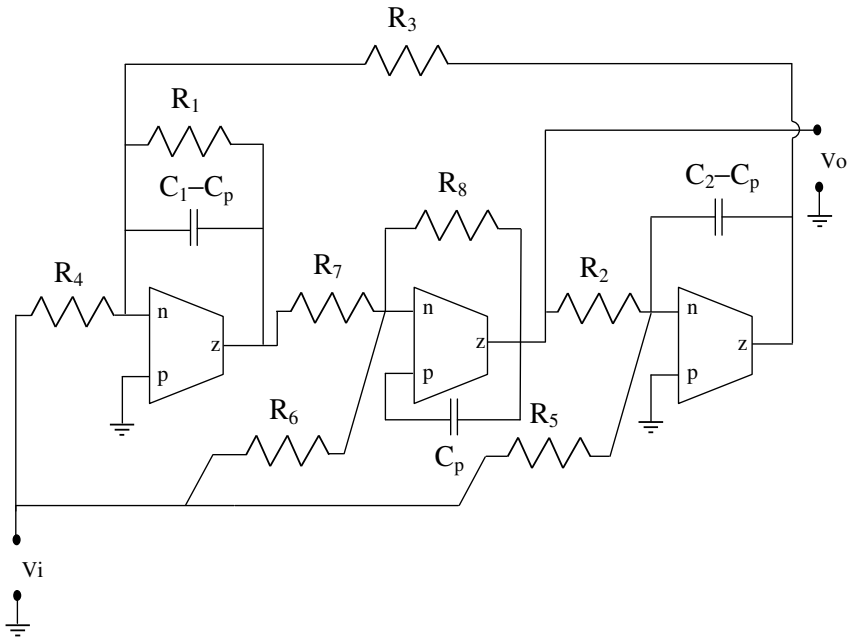

Figure 5.35 Fleischer-Tow Biquad with modifications for compensating the effect of non-ideal R_m

In the following, the resistors employed in the filter configuration have been implemented with MOS transistors. The effect of non-ideal R_m and the compensation methods is still valid for MOS-C realization of the filter.

The resistor, which is connected between one of the input terminals of OTRA and a node elsewhere with two MOS transistors, is realized as shown in Figure 5.23. Since by definition the input terminals are at the same potential (both virtually grounded), they can be both regarded as one of the terminals of the resistor. Due to the current differencing property of the OTRA, the currents in the transistors (I_1 and I_2) are subtracted yielding non-linearity cancellation (Salama & Soliman, 1999a). Note that, the two NMOS transistors, M_1 and M_2, should be matched and they should operate in the ohmic region.

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By replacing each resistor in Figure 5.34 with the MOS implementation of Figure 5.23, the fully integrated realization of Fleischer-Tow biquad shown in Figure 5.36 has been obtained. The resistor values can be calculated by using Equation (5.20). It

is easy to show that each resistor in Figure 5.23 can be electronically controlled with an external voltage. Thus, the quality factor can be adjusted electronically without disturbing the resonant frequency with an external control voltage.

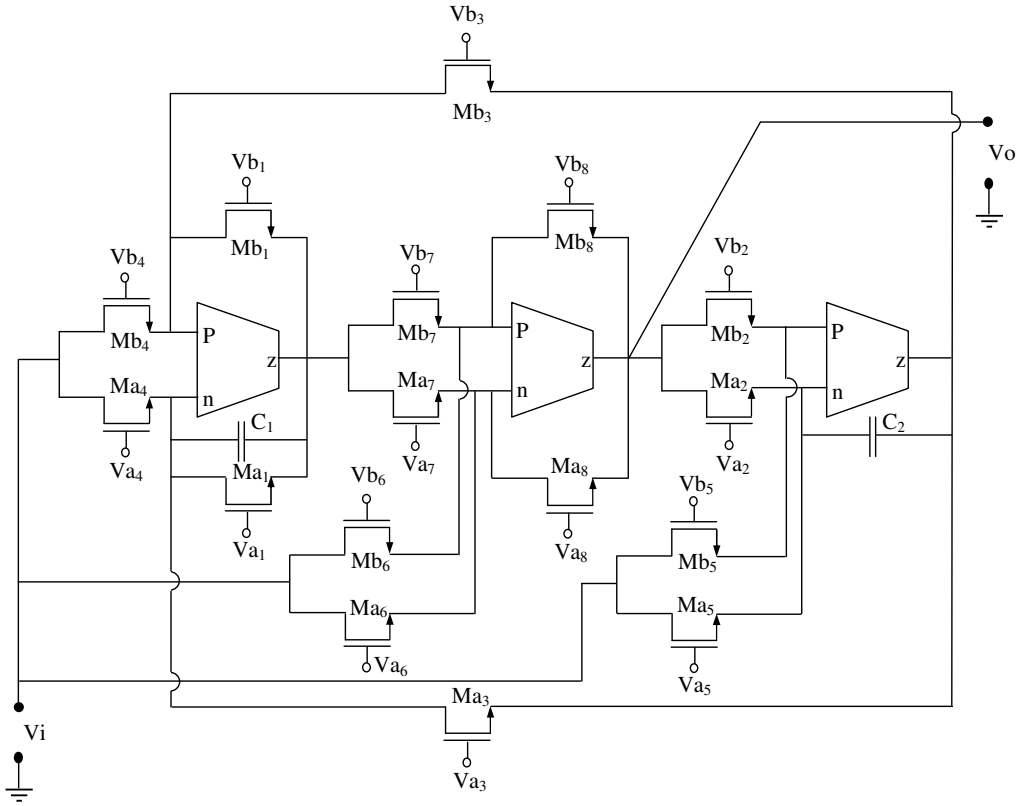

Figure 5.36 Fully integrated realization of the universal biquads with MOS-C implementation

To verify the theoretical study, the second-order LP, HP, BP, notch or bandstop (BS) and AP filters are simulated with PSPICE program. In the simulations, a CMOS realization of OTRA (Salama & Soliman, 1999a), which is shown in Figure 5.31, is used with the same transistor aspect ratios as in (Salama & Soliman, 1999a). Supply voltages are taken as $V_{DD} = 2.5$ V and $V_{SS} = -2.5$ V.

In the simulation, AMI 1.2 μm CMOS technology parameters are used. According to this parameter set, gate oxide thickness is given as $T_{ox} = 2.96 \times 10^{-8}$ m. Since the oxide dielectric constant is $\varepsilon_{ox} = 3.46 \times 10^{-11}$ F/m, oxide capacitance is found as

$C_{ox} = \varepsilon_{ox} / T_{ox} = 1.1689 \times 10^{-3}$ F. Electron mobility, μ_n, can be taken as equal to electron low-field mobility, μ_0, for long-channel devices and it is $\mu_n = \mu_0 = 675.4$ cm^2 / V.s for AMI 1.2 μm technology.

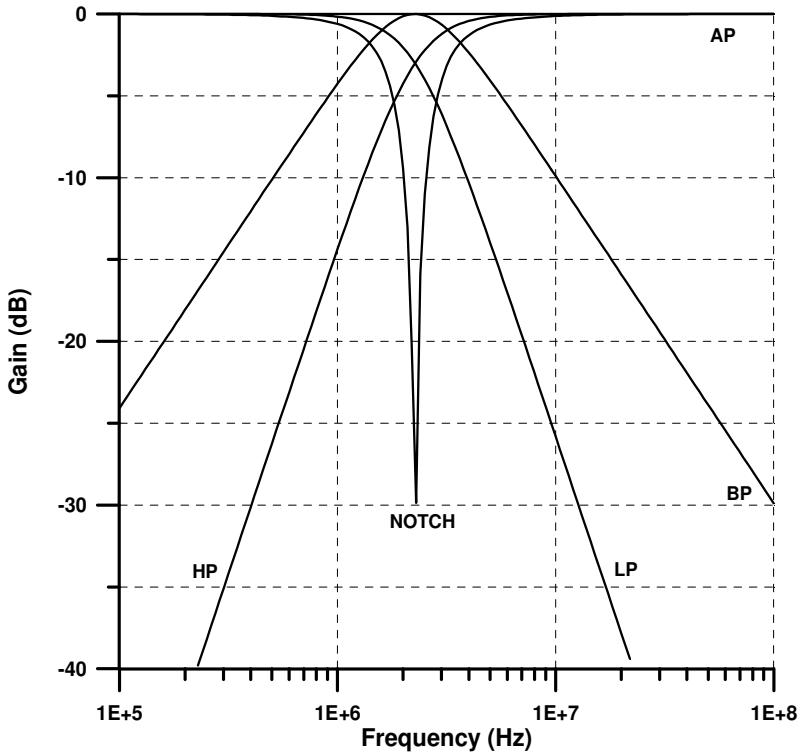

Figure 5.37 Simulated gain responses of biquadratic filters

In the simulations, we take $W_{drawn} = 14.4$ μm and $L_{drawn} = 4.8$ μm for all transistors realizing the resistors. The effective values for the size of these transistors would be $W = W_{drawn} - 2WINT$ and $L = L_{drawn} - 2LINT$ where $WINT = 9.276 \times 10^{-7}$ m and $LINT = 9.091 \times 10^{-10}$ m. We also take V_{ai}=2.3 V and V_{bi}=1.3 V for all i=1, 2, …, 8. Therefore, all of the resistor values are calculated as $R_i \approx 4.85$ kΩ where i=1, 2, …, 8. The capacitor values are taken as $C_1 = 10$ pF and $C_2 = 20$ pF. From these values, the theoretical resonant frequency is found as $f_0 \approx 2.32$ MHz. Figure 5.37 shows the simulation results for all of the five filter. The simulated resonant frequency is equal to $f_0 \approx 2.29$ MHz which is very close to the theoretical one. The electronically tunable feature of the notch filter is also evaluated and confirmed through PSPICE simulations. For this purpose, R_3 is changed by choosing the gate voltage V_{a3} as

1.8 V, 2.0 V, 2.2 V and 2.4 V while keeping V_{b3} at 1.3 V. These voltages correspond to resistance values of 9.69 kΩ, 6.92 kΩ, 5.38 kΩ and 4.41 kΩ for R_3 and in turn theoretical resonant frequencies of 1.64 MHz, 1.94 MHz, 2.20 MHz and 2.43 MHz, respectively with the same values as given above for the passive elements other than R_3. Figure 5.38 shows the simulation results for the notch filter that demonstrates the electronically tunable feature. The simulated resonant frequencies are 1.66 MHz, 1.91 MHz, 2.19 MHz and 2.40 MHz, respectively which are very close to theoretical ones.

The electronically tunable feature of the bandpass filter is also evaluated and confirmed through PSPICE simulations. For this purpose, R_1 is changed by choosing the gate voltage V_{a1} as 1.6 V, 1.8 V, 2.0 V and 2.2 V while keeping V_{b1} at 1.3 V. These voltages correspond to resistance values of 16.16 kΩ, 9.7 kΩ, 6.92 kΩ and 5.38 kΩ for R_1.

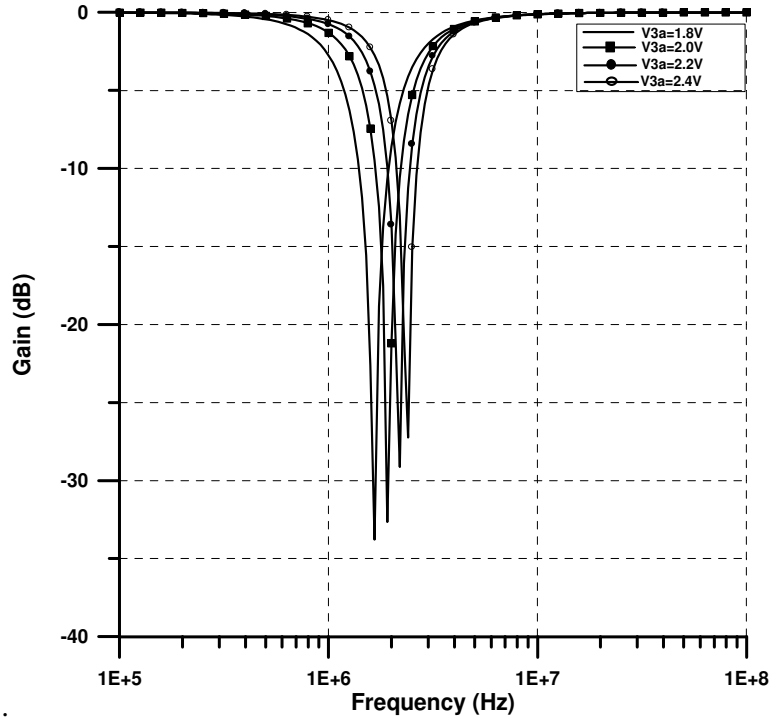

Figure 5.38 PSPICE simulation results showing the electronically tunable feature of the resonant frequency for the notch filter

Figure 5.39 shows the simulation results for the bandpass filter that demonstrates the electronically tunable feature. The quality factors are 2.356, 1.414, 1.00, 0.784, respectively. For input signal of amplitude 0.1V and 2.3 MHz frequency for band pass filter, the THD is 1.10%.

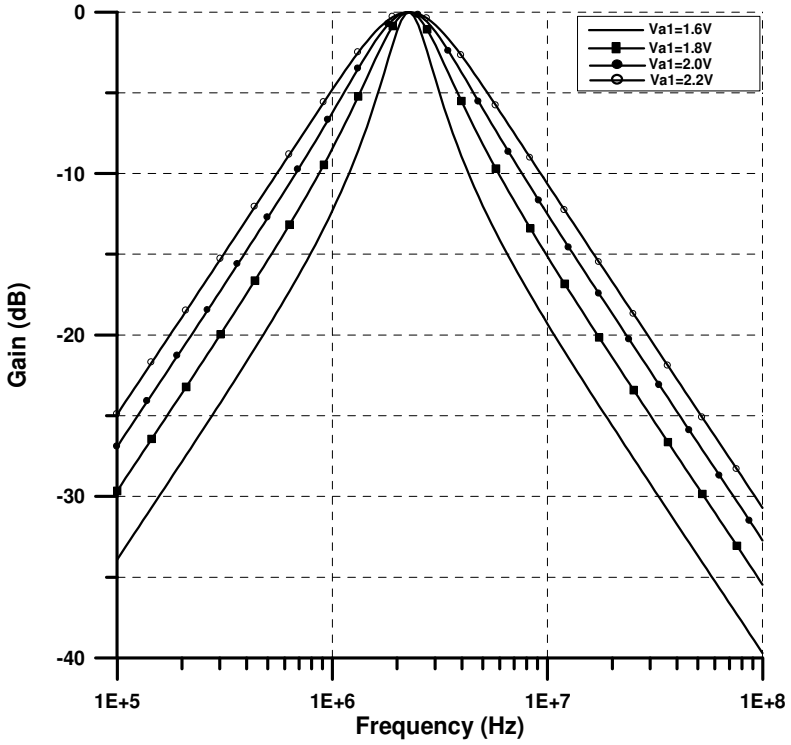

Figure 5.39 PSPICE simulation results showing the electronically tunable feature of the quality factor for the bandpass filter

5.4 The Kerwin-Huelsman-Newcomb Biquad

KHN biquad offers several advantages such as low passive and active sensitivity performance, low component spread and good stability behavior (Kerwin, Huelsman, & Newcomb, 1967). However, classical operational amplifiers have both slew-rate and fixed gain bandwidth product problem. In order to overcome the limited frequency bandwidth properties of the op-amps, KHN-equivalent biquads employ CCIIs and OTRA has been proposed in the literature (Soliman, 1994; Senani & Singh, 1995; Shah & Bhaskar, 2002).

The KHN biquad consists of resistors and capacitors; however these resistors occupy large areas on the chips. Implementing resistors using transistors reduce the size and attribute adjustable filter parameters via bias (gate) voltage. MOSFET-C KHN-type filters, which use above-mentioned technique, have been proposed in the literature employing OTRA and (Current Differencing Buffered Amplifier) CDBA (Salama & Soliman, 1999a; Khaled & Soliman, 2000).

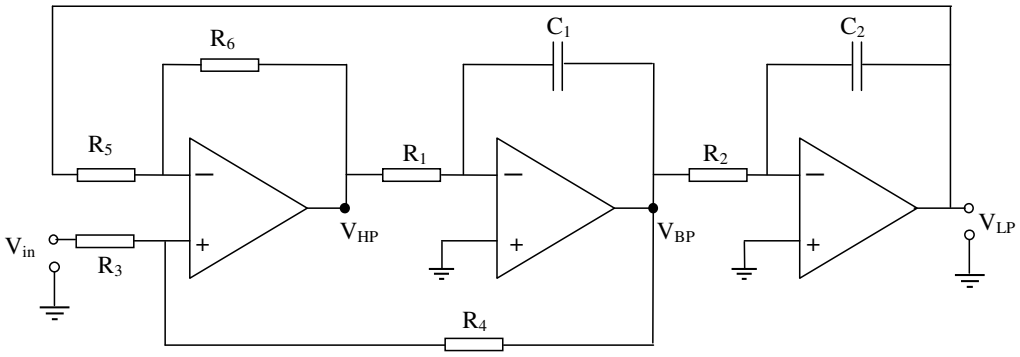

Figure 5.40 Classical op-amp based KHN filter

The original voltage-mode KHN filter employing operational amplifiers is shown in Figure 5.40. The transfer functions and related filter parameters of the KHN filter are given in Table 5.2.

Table 5.2 The transfer functions and related filter parameters of the original KHN

LP Filter	**BP Filter**	**HP Filter**
$\frac{V_{LP}}{V_{in}} = \frac{\left[\frac{R_4}{R_5}\right]\left(\frac{R_6 / R_4}{R_1 R_2 C_1 C_2}\right)}{D(s)}$	$\frac{V_{BP}}{V_{in}} = -\frac{\left[\frac{R_3}{R_5}\right]\left(\frac{R_6}{R_1 R_3 C_1}\right)\cdot s}{D(s)}$	$\frac{V_{HP}}{V_{in}} = -\frac{\left[\frac{R_6}{R_5}\right]\cdot s^2}{D(s)}$
$K_{LP} = \frac{R_4}{R_5}$	$K_{BP} = -\frac{R_3}{R_5}$	$K_{HP} = \frac{R_6}{R_5}$
$D(s) = s^2 + \left(\frac{R_6}{R_1 R_3 C_1}\right)\cdot s + \left(\frac{R_6}{R_1 R_2 R_4 C_1 C_2}\right),\ \omega_0 = \sqrt{\frac{R_6}{R_1 R_2 R_4 C_1 C_2}},\ Q = R_3\sqrt{\frac{R_1 C_1}{R_2 R_4 R_6 C_2}}$		

A method using a single triode MOSFET connected between the input and output of an inverting unity-gain amplifier was mentioned previously. This method, illustrated in Figure 5.3, cancels out the non-linearity of the MOSFET significantly. The equations were achieved in Equation 5.7 and Equation 5.8, previously. Also, another method for canceling the nonlinearity was presented in Section 5.1.2 in Figure 5.11. First of all, for achieving ICCII based KHN, amplification and integration blocks were realized with ICCII. ICCII based amplification and integration is depicted in Figure 5.41. At the same time, MOS-C realizations of the blocks are shown in Figure 5.41 (Toker & Zeki, 2007).

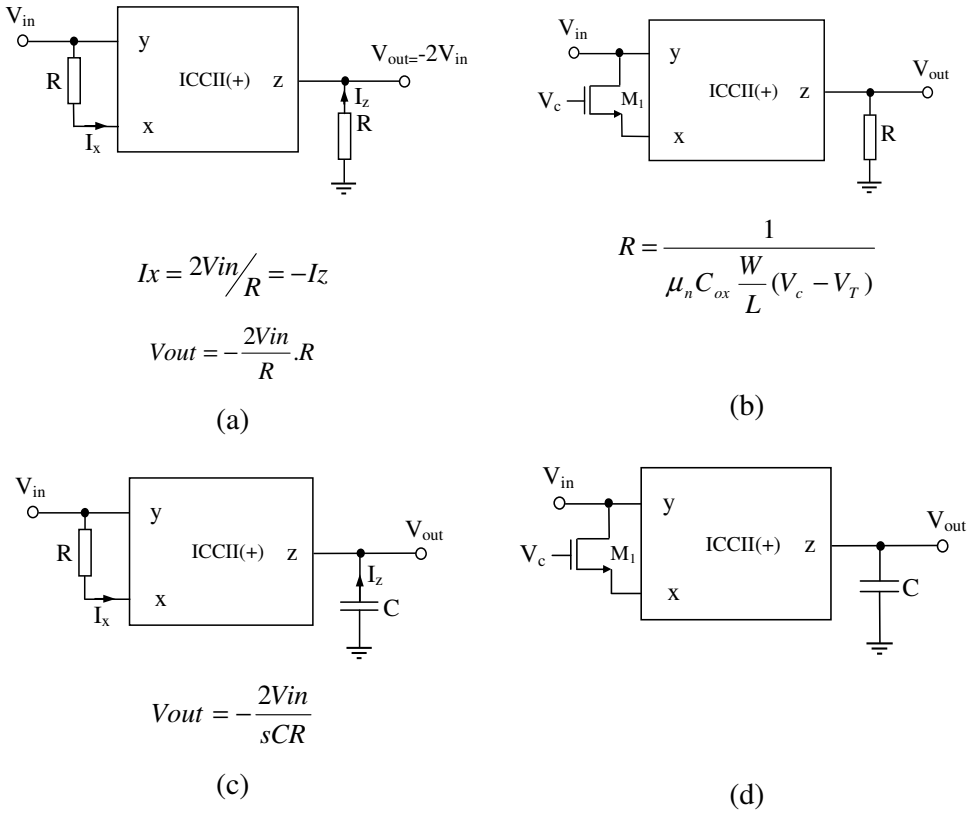

Figure 5.41 Basic blocks using ICCII (a) amplification (b) MOS Realization of amplification (c) integration (d) MOS Realization integration (Toker, 2007)

The proposed ICCII-based KHN equivalent circuit, which is suitable for MOS-C realization, is shown in Figure 5.42. It employs five ICCIIs and four voltage followers (VF) as active elements together with two grounded capacitors and six

resistors that are suitable for MOS-C realization. It can be noticed that the inverting voltage cell between the Y and X terminals of an ICCII has the same property as the active device in Figure 5.42. Hence, ICCIIs can be used to perform the nonlinearity cancellation technique. Routine analysis yields the transfer function of the proposed circuits as in Table 5.3.

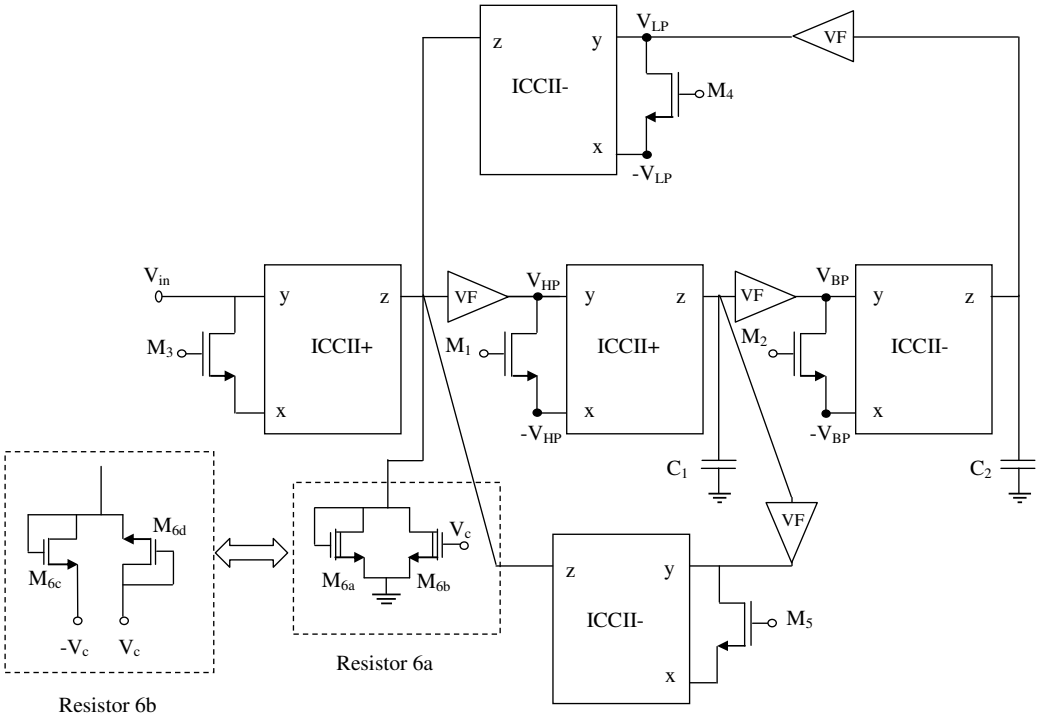

Figure 5.42 MOS-C realization of KHN filter with ICCII

The transistors M_{6a} and M_{6b} are used for implementing a grounded resistor. Another MOSFET based gorunded resistor implementing technique is introduced by Wang, (1990), as mentioned in Chapter 2.2.10. This implementation technique is used instead of the Resistor 6a.

Table 5.3 The transfer functions and related filter parameters of the proposed KHN

LP Filter	BP Filter	HP Filter
$H_{LP}=\frac{V_{LP}}{V_{in}}=\frac{\frac{8R_6}{C_1C_2R_1R_2R_3}}{\Delta}$	$H_{BP}=\frac{V_{BP}}{V_{in}}=\frac{s\cdot\frac{4R_6}{C_1R_1R_3}}{\Delta}$	$H_{HP}=\frac{V_{HP}}{V_{in}}=\frac{s^2\cdot\frac{2R_6}{R_3}}{\Delta}$
$K_{LP}=\frac{R_4}{R_3}$	$K_{BP}=\frac{R_5}{R_3}$	$K_{HP}=\frac{2R_6}{R_3}$
$\Delta=s^2+s\left[\frac{4R_6}{C_1R_1R_5}\right]+\frac{8R_6}{C_1C_2R_1R_2R_4}$, $\omega_0=\sqrt{\frac{8R_6}{C_1C_2R_1R_2R_4}}$, $Q=R_5\sqrt{\frac{C_1R_1}{2C_2R_2R_4R_6}}$		

It is clear that the proposed KHN circuit can simultaneously realize three basic filtering function and gain, quality factor and resonant frequency of the filters can be controlled electronically. It should be noted that inverting LP, HP, BP can also be obtained from proposed KHN filter without changing circuit configuration due to inverting voltage copying nature of ICCII. As a result of this, allpass and notch filter response can also be evaluated from the proposed configuration, as shown in Figure 5.43, by using a DDCC and imposing R_3=R_4=R_6. Note that a DDCC has the following port relations (Chiu, Liu, Tsao & Chen, 1996).

$$V_x=V_{y1}-V_{y2}+V_{y3}\,,\ I_{y1}=I_{y2}=I_{y3}=0\,,I_z=I_x\,. \tag{5.46}$$

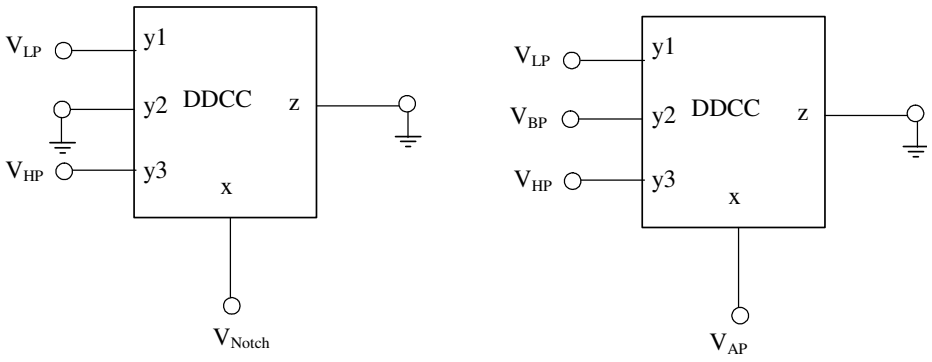

Figure 5.43 Allpass and Notch evaluation circuit by using proposed KHN biquad

To verify the theoretical study, the presented filter is simulated by using PSPICE program. For SPICE simulations, CMOS ICCII is obtained from CMOS DVCC in (Ibrahim, Minaei & Kuntman, 2006) by grounding Y_1 port as shown in Figure 5.44 and 0.35μm TSMC parameters are chosen. As a VF, a simple translinear loop is used. According to this parameter set, gate oxide thickness is given as T_{ox}= 7.9x10^{-9} *m*. Since the oxide dielectric constant is ε_{ox}=3.46x10^{-11}F/m, oxide capacitance per unit area is found as $C_{ox}=\varepsilon_{ox}/T_{ox}$=4.38x10^{-3}F/m^2. In the simulations, we take W_{drawn}=4.2μm and L_{drawn}=1.2μm for all transistors realizing the resistors except R_{6a}. We also take V_c=1.65V for all i=1, 2, …, 5. R_{6a} uses depletion mode transistors and W_{drawn}=10μm and L_{drawn}=13μm, V_c=7.5V. The capacitor values are taken as $C_1=C_2$=100pF. Using these values, the theoretical resonant frequency is found as f_0≈1.914 MHz. The simulated resonant frequency is equal to f_0≈1.995 MHz which is very close to theoretical one. In the simulation of other R_{6b} implementing technique, we take W_{drawn}=3.6μm and L_{drawn}=1μm, V_c=1.1V. In this case, the simulation frequency is equal to f_0≈1.945 MHz which is very close to other R_{6a} implementation technique. For input signal of amplitude 10mV and 1.9 MHz frequency and using R_{6a} for BP filter, THD is 0.194%. Using R_{6b}, the THD is 0.216%. As it is seen from these values, implementation technique for R_{6a} has better THD and has only one control voltage, but these technique uses depletion mode transistors. Although, implementation technique for R_{6b} bad THD and has two control voltages, it uses enhancement transistors and suitable for high frequencies as mentioned in Section 2.2.10. The implementation technique for R_{6a} is not suitable for high frequencies as it is seen in Figure 4.19. The simulation results of the proposed KHN filter are given in Figure 5.45.

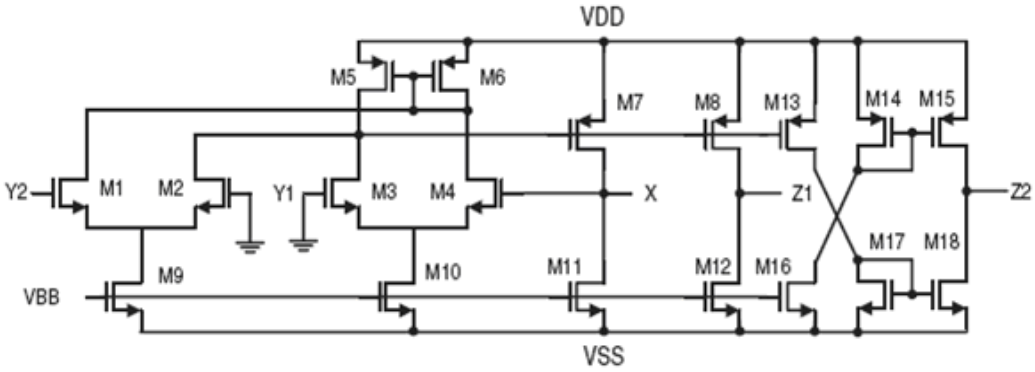

Figure 5.44 CMOS realization of DVCC based ICCII referans (Ibrahim, Minaei & Kuntman, 2006)

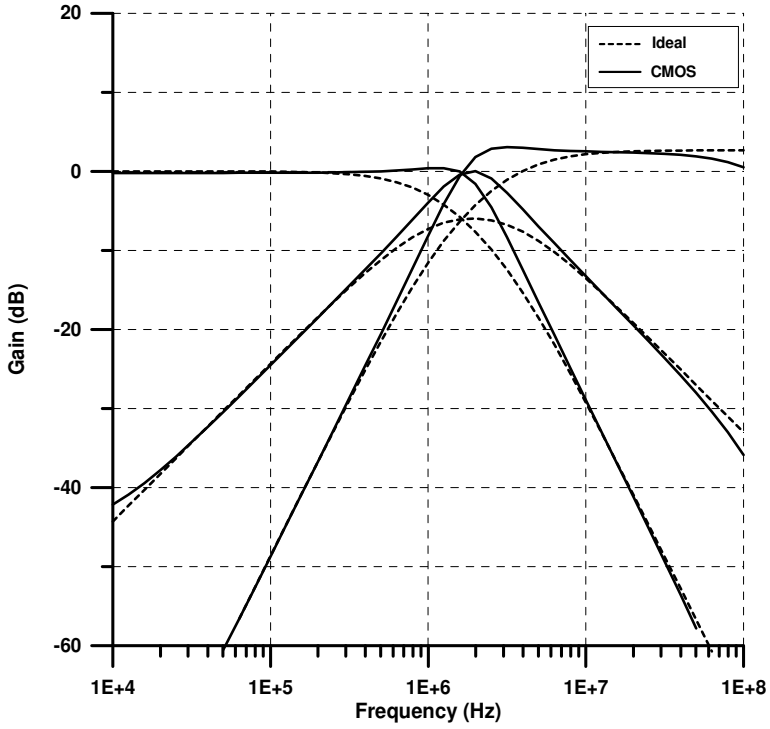

Figure 5.45 PSPICE simulation results of the proposed KHN filter

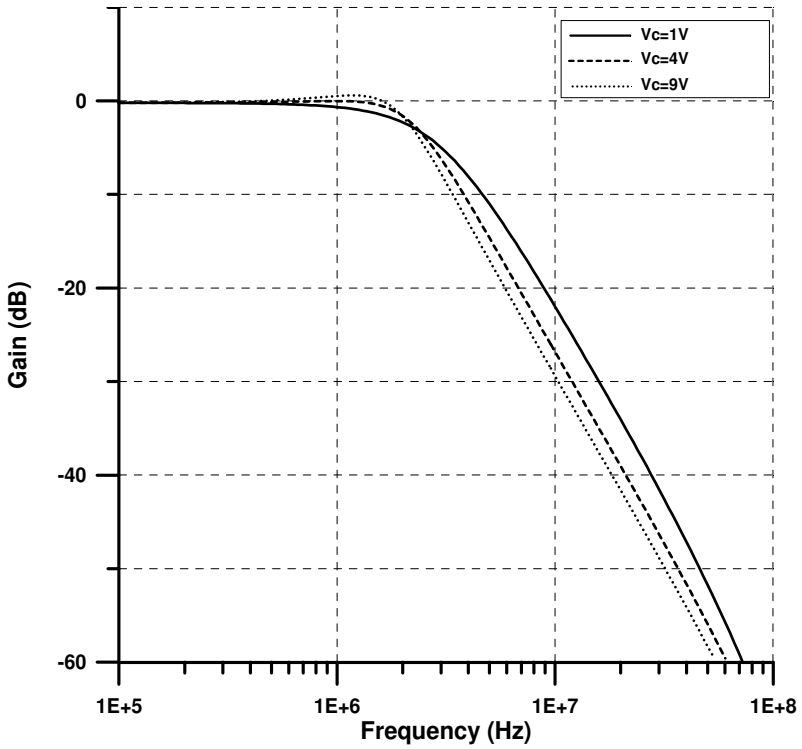

Figure 5.46 The electronically tunable feature of the resonant frequency of LP filter

The electronically tunable feature of the LP filter is also evaluated and confirmed through PSPICE simulations. For this purpose, R_1 is changed by choosing the gate voltage V_c as 1V, 4Vand 9V. Figure 5.46 demonstrates the electronically tunable feature of the proposed KHN filter as a LP filter.

The circuit simultaneously provides three basic filter functions, namely BP, HP and LP functions. Gain, quality factor and resonant frequency of the filters are electronically adjustable as in original KHN biquad. Furthermore, both inverting and non-inverting type of three basic filtering functions are available. No any component matching is imposed for the realization of LP, BP and HP responses. Allpass and notch responses can be evaluated by the use of a DDCC and allowing three resistors matching. Moreover, all outputs of the proposed circuit exhibit low output impedances so that the filters can be cascaded without additional buffers. The proposed configuration can be made fully integrated based on MOS-C realization by making use of inverting voltage copying inputs of ICCII.

5.5 Electronically Variable Frequency Oscillator

Oscillators are widely used in signal and control processing circuits, measurement and communication systems. Therefore, in the literature many active-RC oscillator circuits have been proposed which use single active element such as classical voltage op-amp, CCII, current feedback operational amplifier (CFOA) (Toumazou, Lidjey & Haigh, 1990; Celma, Martinez & Carlosena, 1992; Senani & Singh, 1996; Hou, Yean & Chang, 1996). In oscillator circuits, the usage of classical op-amp for an active element suffers from limited gain-bandwidth product problems and from low slew rate at its output. On the other hand, the current conveyor as an active element offers several advantages such as large band width, high linearity, wide dynamic range, simple circuitry and low power consumption.

Several oscillator circuits have been proposed previously; however, they can not provide a simple and an efficient voltage controlled oscillation frequency. In the introduced electronically variable frequency oscillator configuration is obtained from the previously reported general configuration with a modification (Toker, Kuntman, Cicekoglu & Discigil, 2002). The oscillator circuit employs a second generation inverting current conveyor, two capacitors and three resistors as shown in Figure 5.47.

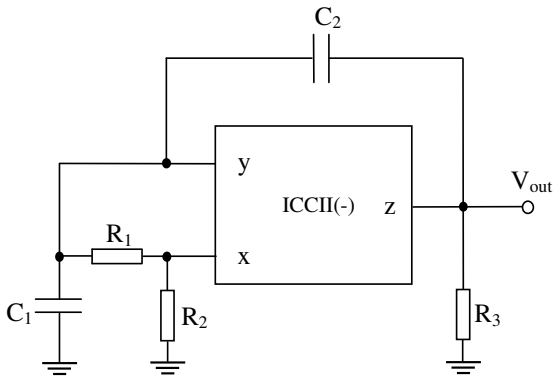

Figure 5.47 ICCII based oscillator configuration
(Toker, Kuntman, Cicekoglu & Discigil, 2002)

Routine analysis yields the characteristic equation as follows;

$$s^2 C_1 C_2 + s\left[C_1 G_3 + C_2 G_3 - C_2 G_2\right] + 2G_1 G_3 = 0\,. \tag{5.47}$$

The frequency of oscillation and condition of oscillation are given, respectively, by

$$f_0 = \frac{1}{2\pi}\sqrt{\frac{2G_1 G_3}{C_1 C_2}}\ , \tag{5.48}$$

$$C_1 G_3 + C_2 G_3 = C_2 G_2\,. \tag{5.49}$$

Thus, f_0 can be independently controlled trough a single resistor R_1 without affecting oscillation condition.

The resistor R_1 is changed with an NMOS transistor which is mentioned in Section 2.2.1. The resistors R_2 and R_3 are changed with NMOS transistor pairs, which are mentioned in Section 2.2.6. The circuit becomes as shown in Figure 5.48 (Gökçen & Çam, 2010c).

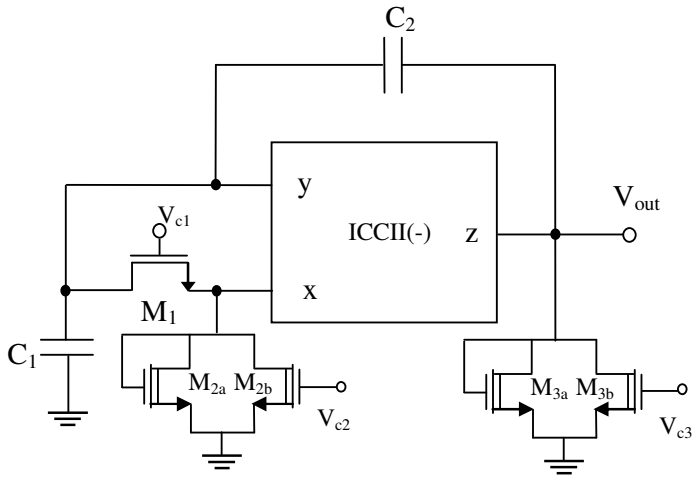

Figure 5.48 The electronically variable frequency oscillator configuration

To verify the theoretical study, the oscillator circuit is simulated using PSPICE program. The capacitor values are chosen as, C_1 = 407 pF, C_2 = 400 pF with 20mV

initial condition. The PSPICE simulations are performed using a CMOS realization of ICCII which obtained from CMOS DDCC in (Ibrahim & Kuntman, 2002b) by grounding Y_1, Y_3 ports which is shown in Figure 5.15 and 0.35µ TSMC MOSIS process model parameters. Supply voltages are taken as V_{DD} = 2.5V and V_{SS} = -2.5V We take W=4.2µm, L=1.4µm and V_c =1.75V for the gate voltage of the M_1 transistor. The resistor value is calculated as R≈1.8kΩ. We take W=5µm, L=15.5µm and W=5µm, L=31µm for resistors R_2 and R_3, respectively, with the gate voltage $V_{c2} = V_{c3}$ = 7.5V. The resistor values are calculated as R_2≈5kΩ and R_3≈10kΩ. These values yield 133.4 KHz oscillation frequency. Resulting output waveform of the circuit is given in Figure 5.49.

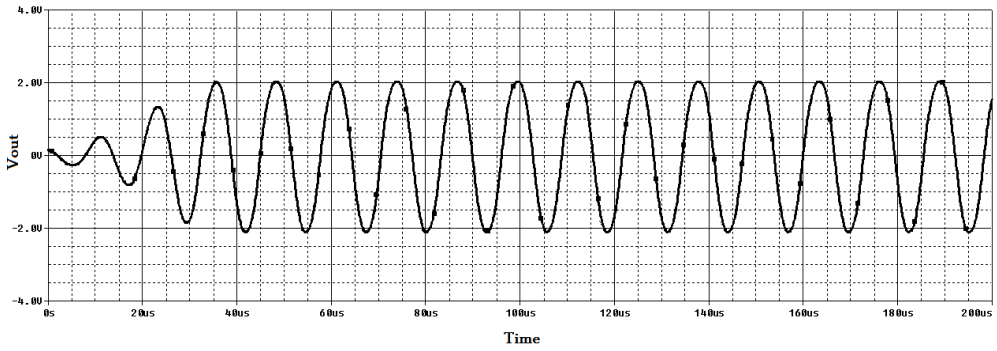

Figure 5.49 The output waveform of the oscillator

The tunability of oscillation frequency trough the gate voltage of the M_1 transistor without effecting oscillation condition is shown in Figure 5.50. The THD for 133.4 KHz and 0.1V amplitude signal is 0.464%.

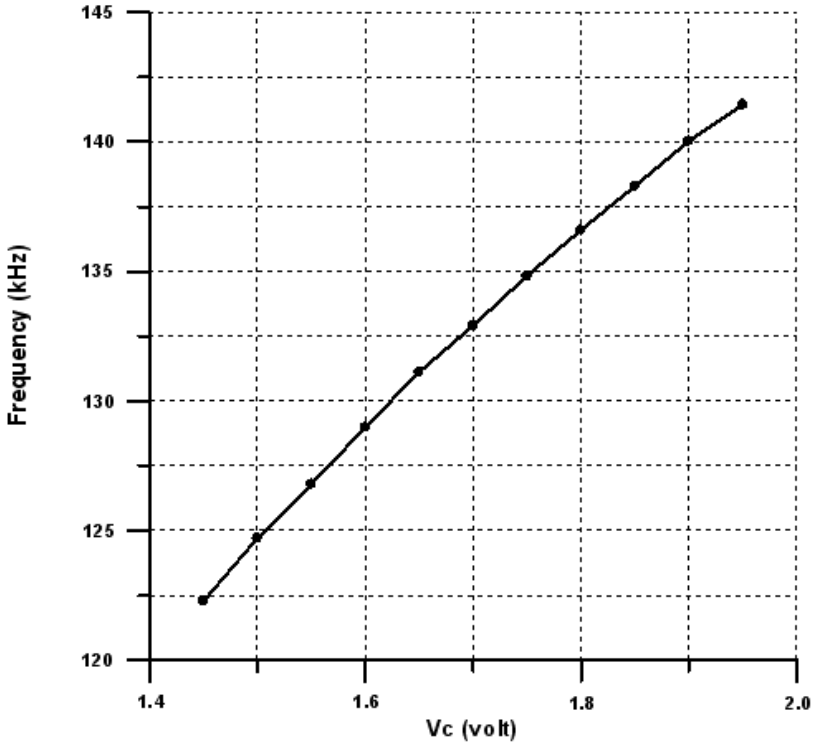

Figure 5.50 Variation of the oscillation frequency trough V_c.

5.6 Tow-Thomas Biquad and Quadrature Oscillator as an ICCII Applications

In this section, ICCII based Tow-Thomas biquad and quadrature oscillator circuit are presented. The resistors in these circuits have been realized using MOS transistors as explained in Chapter Two leading to MOS-C realization. In the simulations of the following circuits, we use the CMOS DVCC in (Ibrahim, Minaei & Kuntman, 2006) by grounding Y_1 terminal which is shown in Figure 5.44 together with 0.5µm MIETEC process parameters. As a VF, a simple translinear loop is used.

5.6.1 Tow-Thomas Biquad

The proposed ICCII based Tow-Thomas biquad is shown in Figure 5.51.

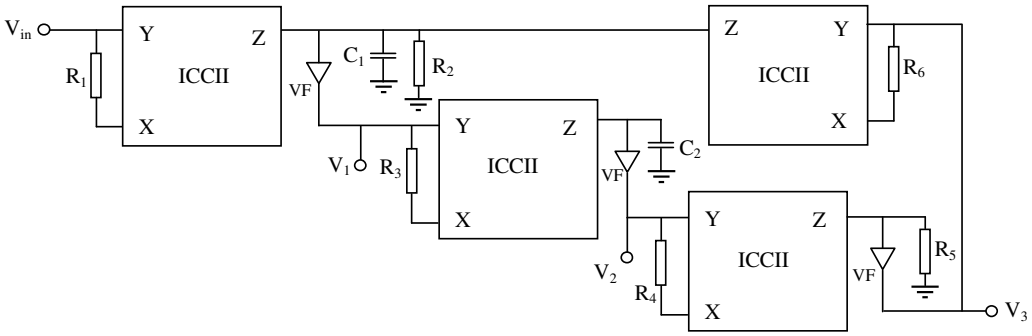

Figure 5.51 ICCII based Tow-Thomas biquad

MOS-C realization of Tow-Thomas biquad using ICCII is shown in Figure 5.52.

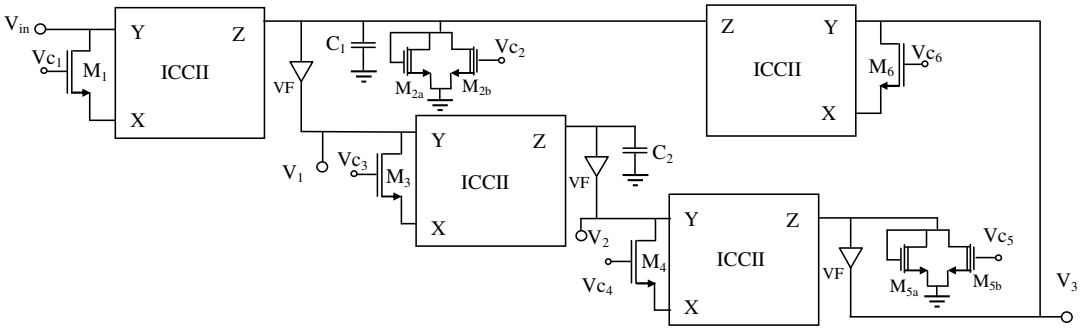

Figure 5.52 MOS-C realization of Tow-Thomas biquad

Routine analysis yields the following transfer functions.

$$\frac{V_1}{V_{in}} = -\frac{s\dfrac{2}{C_1R_1}}{s^2 + s\dfrac{1}{C_1R_2} + \dfrac{8R_5}{C_1C_2R_3R_4R_6}}, \tag{5.50}$$

$$\frac{V_2}{V_{in}} = \frac{\dfrac{4}{C_1C_2R_1R_3}}{s^2 + s\dfrac{1}{C_1R_2} + \dfrac{8R_5}{C_1C_2R_3R_4R_6}}, \tag{5.51}$$

$$\frac{V_3}{V_{in}} = -\frac{\dfrac{8R_5}{C_1C_2R_1R_3R_4}}{s^2 + s\dfrac{1}{C_1R_2} + \dfrac{8R_5}{C_1C_2R_3R_4R_6}}. \tag{5.52}$$

The natural frequency and quality factor can be given by

$$\omega_0 = \sqrt{\frac{8R_5}{C_1C_2R_3R_4R_6}}, \tag{5.53}$$

$$Q = 2R_2\sqrt{\frac{2C_1R_5}{C_2R_3R_4R_6}}. \tag{5.54}$$

As it is seen from these equations, inverting bandpass, non-inverting lowpass and inverting lowpass filters can be realized using this topology.

In the PSPICE simulations of this circuit, we take W = 4.5 μm and L = 1.5 μm for all transistors realizing the resistors R_1, R_3, R_4 and R_6. We also take V_c=1.65V. Therefore, the above mentioned resistor values are equal to $R \approx 2.8$ kΩ. For resistors R_2 and R_5, the transistor's channel width and length are taken as W = 25 μm and L= 15 μm. We also take V_C=7.5V. Thus, the resistor values are equal to $R \approx 1.15$ kΩ. The capacitor values are taken as $C_1 = C_2 = 100$ pF. From these values, the theoretical resonant frequency is found as 1.03 MHz. Figure 5.53 shows the simulation results for the filter. The simulated resonant frequency is equal to $f_0 \approx 1.0$ MHz which is very close to the theoretical one. The tunability of the quality factor is shown in Figure 5.54. As it is seen, the quality factor of the bandpass filter is adjusted by changing the gate voltage of M_2 transistor without changing its center frequency. For input signal of amplitude 0.1V and 1 MHz frequency for BP filter, the THD is 0.403%.

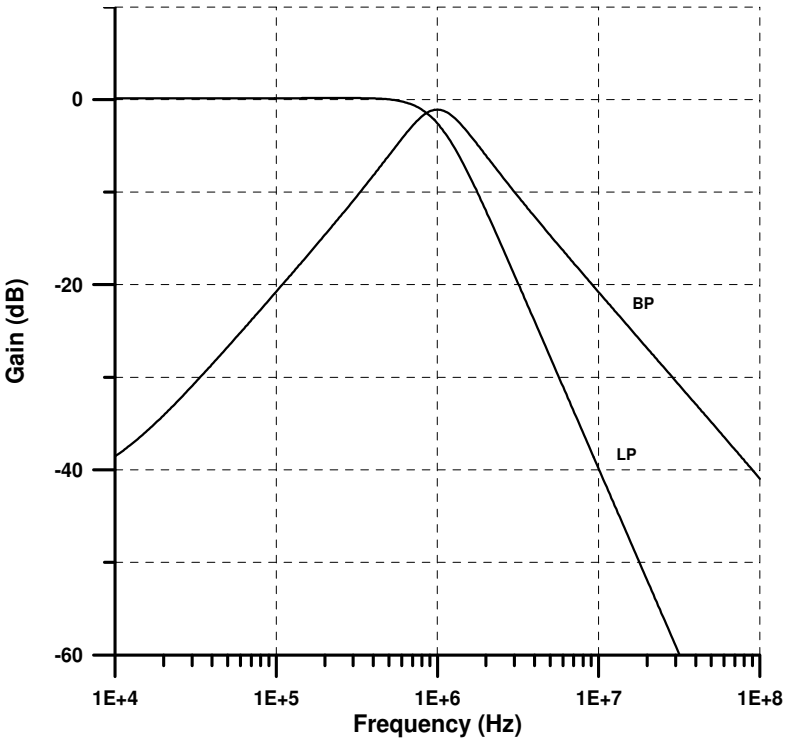

Figure 5.53 Simulated gain responses of Tow-Thomas biquad

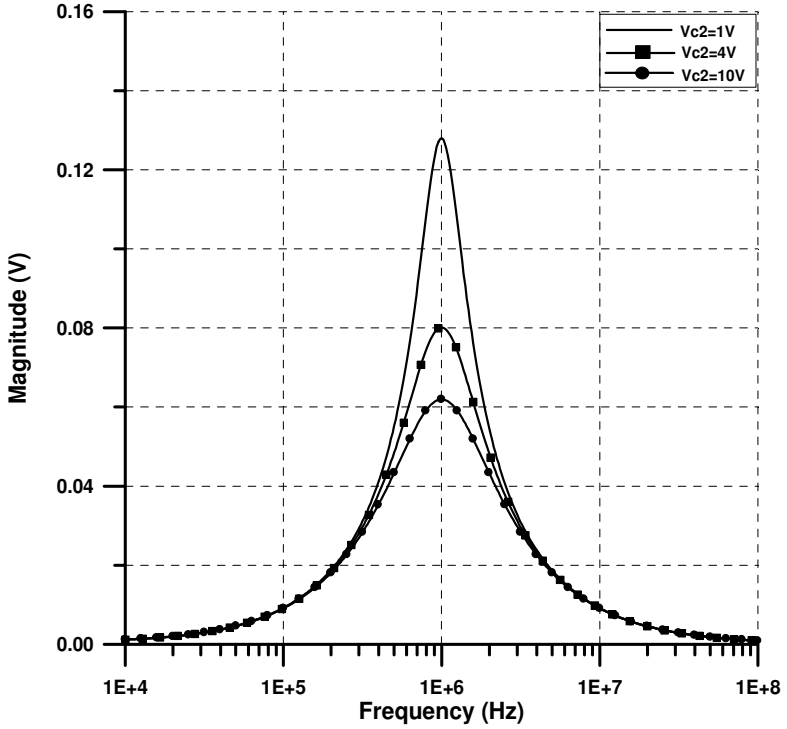

Figure 5.54 Electronic adjustability of Tow-Thomas biquad

5.6.2 Quadrature Oscillator

It is a well-known fact that a sinusoidal quadrature oscillator can be realized by cascade connection of an allpass section with an integrator circuit and connecting the output of one block to the input of another to complete the loop (Haritantis, 1985). Using this approach, ICCII based quadrature oscillator can be implemented as shown in Figure 5.55 and MOS-C realization of the proposed oscillator is shown in Figure 5.56. In this circuit, an ICCII based integrator and first order allpass filter are used. For providing a sinusoidal oscillation, the loop gain of the circuit is set to unity at $s = j\omega$, i.e.

$$\left[\frac{s - 2/R_1C_1}{s + 2/R_1C_1}\right]\left[\frac{2}{sR_2C_2}\right]\Bigg|_{s=j\omega} = 1. \tag{5.55}$$

From Equation (5.55) oscillation condition and frequency can be found respectively as;

$$R_1C_1 = R_2C_2, \tag{5.56}$$

$$\omega_0 = \sqrt{\frac{4}{R_1C_1R_2C_2}}. \tag{5.57}$$

For simplicity, if we choose $R_1 = R_2 = R$ and $C_1 = C_2 = C$, oscillation condition is satisfied and oscillation frequency becomes

$$\omega_0 = \frac{2}{RC}. \tag{5.58}$$

In the simulations, we take W = 4.5 μm and L = 1.5 μm for the transistors realizing the resistors R_1 and R_2. Therefore, the mentioned resistor values are equal to $R \approx 2.8$ kΩ. The capacitor values are taken as $C_1 = C_2 = 41$ pF. Theoretical oscillator frequency is calculated as 2.77 MHz whereas, the simulated one is 2.83 MHz. Resulting output waveforms of the circuit is given in Figure 5.57.

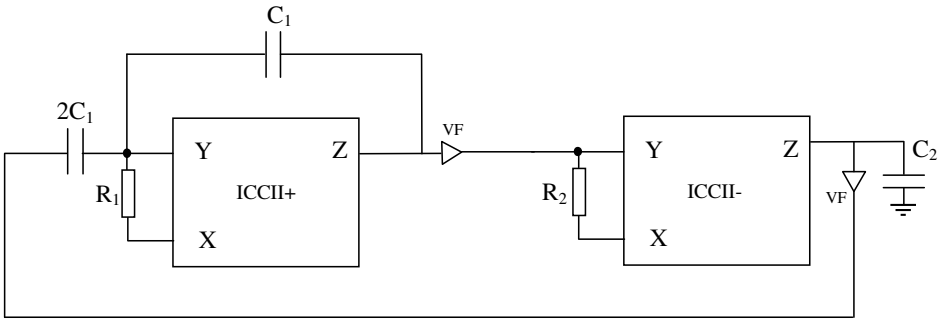

Figure 5.55 MOS-C realization of the oscillator

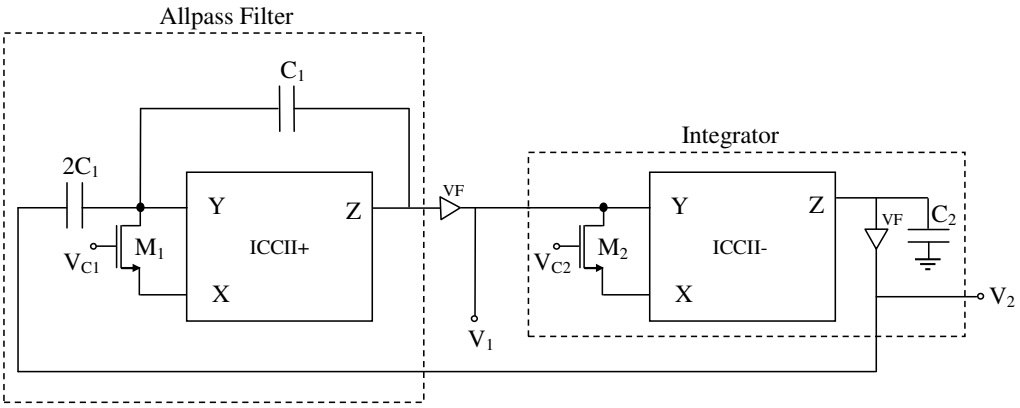

Figure 5.56 MOS-C realization of the oscillator

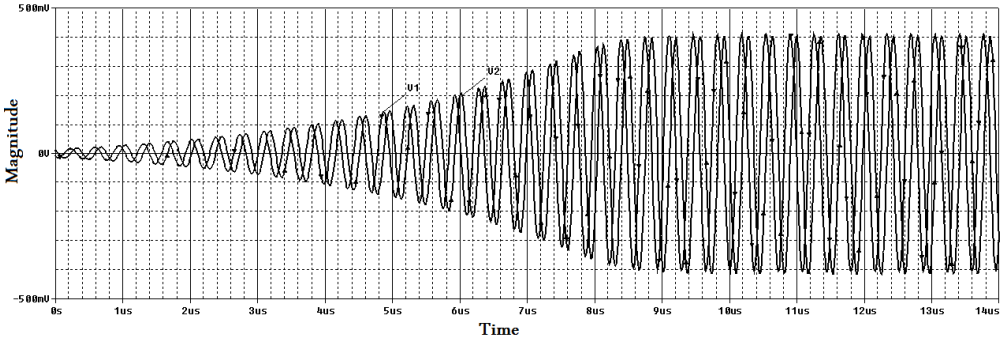

Figure 5.57 Simulated output voltages (V_1 and V_2) of the quadrature oscillator

Figure 5.58 showns the quadrature oscillator output in different time domian.

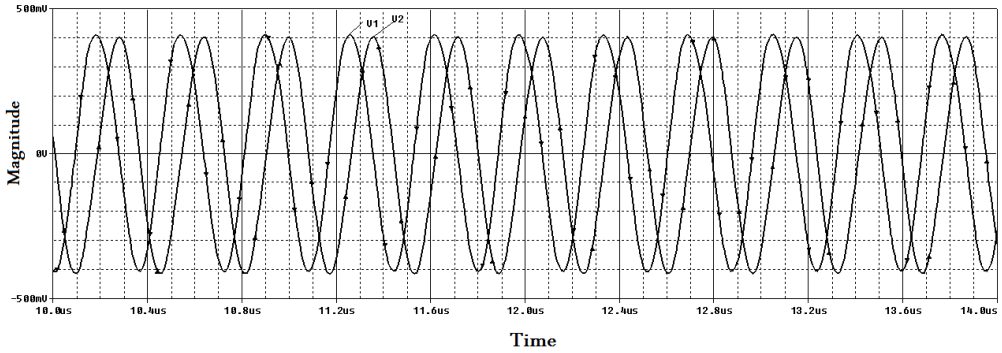

Figure 5.58 Simulated output voltages (V_1 and V_2) of the quadrature oscillator

5.7 Video Filter Application

In this section, a fifth order video band elliptic filter topology as the application example is presented. In video applications, high order elliptic filters are used. The proposed fifth-order lowpass filter is simulated with PSPICE simulation program. The elliptic filter configuration consists of two cascade connected lowpass notch filters which are obtained from the circuit of Figure 5.36 by proper selection of resistors and also a lowpass biquad shown in Figure 5.59. After designing the fifth order video band elliptic filter topology, the MOS-C realization is obtained and used in PSPICE simulation. Block diagram of the fifth order elliptic video filter is given in Figure 5.60.

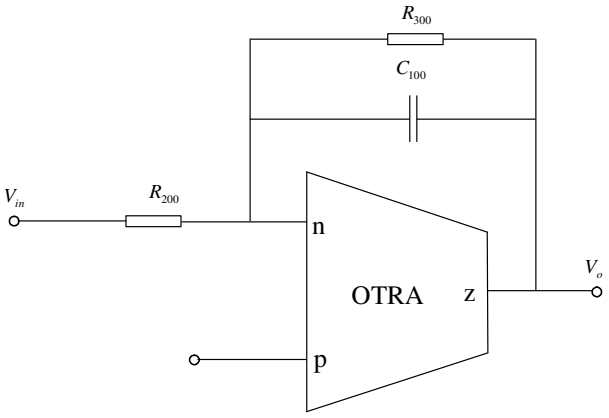

Figure 5.59 The first order Lowpass filter

Video filter is designed to pass the signals of frequencies up to 5 MHz and sharply suppress the signals beyond this frequency.

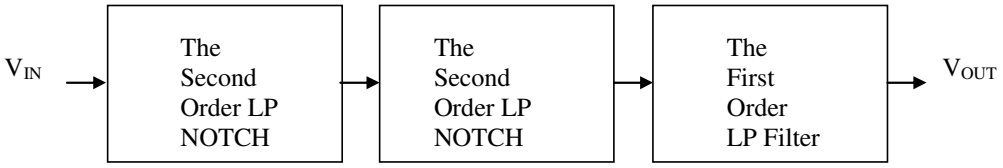

Figure 5.60 Block diagram of proposed fifth order video filter

The resistors are implemented via MOS transistors as mentioned in Chapter 2. The resistor values correspond to R_1=35kΩ, R_2=25kΩ, R_3=5kΩ, R_4=20kΩ, R_5=5kΩ, R_6=5kΩ, R_7=5kΩ, R_8=5kΩ, C_1=4.5pF, C_2=4.5pF (for the first lowpass notch); R_{10}=5.2kΩ, R_{20}=10kΩ, R_{30}=10kΩ, R_{40}=5.2kΩ, R_{50}=4.8kΩ, R_6=5kΩ, R_7=5kΩ, R_8=5kΩ C_{10}=4.5pF, C_{20}=4.5pF (for the second lowpass notch); R_{200}=2.6kΩ, R_{300}=2.4kΩ, C_{100}=21pF (for the last lowpass). The simulated output voltage of the fifth order elliptic lowpass filter is shown in Figure 5.61.

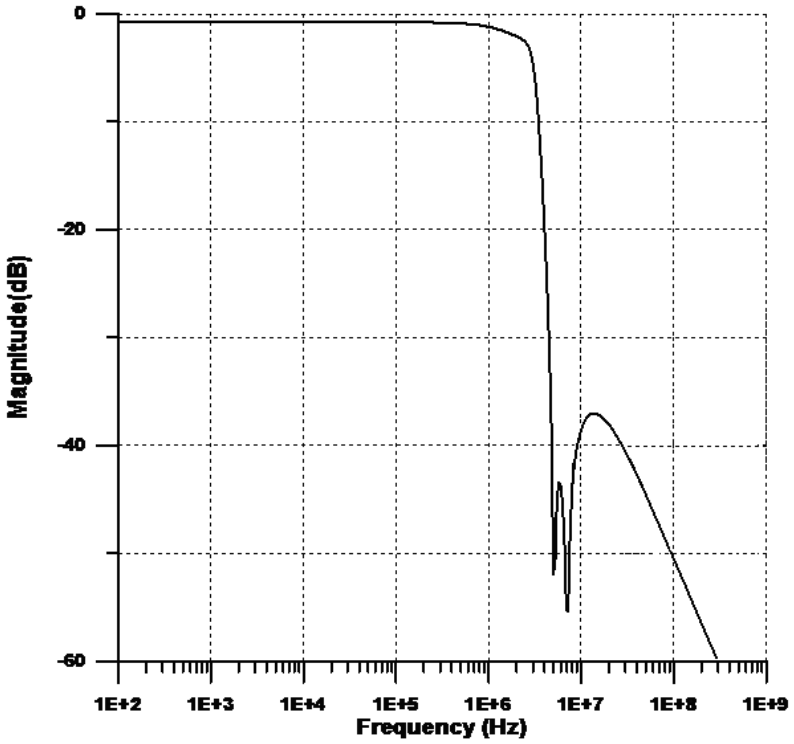

Figure 5.61 Gain response of the proposed filter

CHAPTER SIX
CONCLUSION

6.1 Concluding Remarks

Analog ICs are occupying important place in electronics. The major intended features of these circuits are low power dissipation and much smaller area on the chip. Also, resistors are mostly used passive element in these circuits. Whereas, resistors have disadvantages like power consumption and occupy large area. At the same time, a MOS transistor, which is operating in linear region, acts like a linear resistor. But, the major handicap is nonlinear terms in the MOS transistor current. In the literature lots of techniques are presented to cancel these nonlinear terms. Using these techniques MOS transistors can be use as linear resistor. The resultant resistor value can be changed electronically via the gate voltage of the MOS transistor. Consequently, the circuit consists of only MOS transistors and capacitors. These types of circuits are called MOS-C circuits.

In this thesis, MOS-C realization approach in the analog ICs is investigated. For this purpose, firstly the nonlinearity cancellation techniques in MOS transistors are examined and relevant equations are given. The analyses show that eliminating the body effect coefficient the odd nonlinearities are cancelled completely. And remaining even nonlinearities cancelled according to drain and source voltages. Also appropriate active elements for nonlinearity cancellation techniques are given and the element representations and terminal equations are shown.

Thus, the main points of the MOS-C realization are discussed. With these mentioned nonlinearity cancellation techniques and active elements, first order allpass filters, KHN and Tow Thomas biquads, single amplifier biquad and oscillator circuits are presented. At the same time, ICCII based Tow Thomas and quadrature oscillator is given.

For the application circuit, fifth order elliptic video filter is presented. In all of the above mentioned circuits, the resistors are implemented via MOS transistors and this feature gives them fully integrable property.

Automatic electronic tuning is crucial for fully integrated filters to compensate the drifts of element values and filter performances due to component tolerance, device non-ideality, parasitic effects, temperature, environment and aging. Changing the gate voltage of the MOS transistor, the resistor value can be controlled and so the circuit parameters have electronically tunable feature. The natural frequency, the quality factor and the gain can be changed electronically. The workability of the presented circuits has been verified by PSPICE simulation results.

6.2 Future Work

In this thesis, nonlinearity cancellation techniques in MOS transistor current are given. Some of them have complete cancellation but some of them have not. New nonlinearity cancellation techniques can be improved with complete cancellation. Active elements, which use these cancellation techniques, are limited. New active elements can be improved and using these techniques and active element various filters, oscillators and other circuits can be developed.

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APPENDICES

APPENDIX A

LIST OF SYMBOLS AND ABBREVIATIONS

V_C=Control Voltage

V_T=Threshold Voltage

V_{FB}=Flat Band Voltage

V_B= Substrate Bias Voltage

i_L=Linear Term Of The Current

i_N=Nonlinear Term Of The Current

μ=Effective Mobility

C_{OX}=Oxide Capacitance Per Unit Area

W=Channel Width

L=Channel Lenght

G=Conductance Parameter

γ=Body Effect Coeffiecient

ϕ_B=Surface Inversion Potential

CCI=First Generation Current Conveyor

CCII= Second Generation Current Conveyor

CCIII= Third Generation Current Conveyor

ICCII= Inverting Type Second Generation Current Conveyor

OTRA=Operational Transresistance Amplifier

DVCC=Differential Voltage Current Conveyor

DDCC=Differential Difference Current Conveyor

CFOA=Current Feedback Operational Amplifier

APPENDIX B

1.2 µm AMI SPICE process parameters

```
.MODEL NT NMOS LEVEL=3 PHI=0.700000
+TOX=2.9600E-08 XJ=0.200000U TPG=1
+ VTO=0.5444 DELTA=1.1810E+00 LD=9.0910E-10 KP=7.8792E-05
+ UO=675.4 THETA=1.1400E-01 RSH=9.0910E-02 GAMMA=0.5594
+ NSUB=1.2830E+16 NFS=6.5000E+11 VMAX=1.8380E+05 ETA=9.8850E-02
+ KAPPA=2.2990E-01 CGDO=5.0000E-11 CGSO=5.0000E-11
+ CGBO=3.4989E-10 CJ=2.7735E-04 MJ=5.4186E-01 CJSW=1.3413E-10
+ MJSW=1.0000E-01 PB=9.6971E-01
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is 9.2760E-07

.MODEL PT PMOS LEVEL=3 PHI=0.700000
+TOX=2.9600E-08 XJ=0.200000U TPG=-1
+ VTO=-0.8325 DELTA=2.3680E+00 LD=1.0020E-09 KP=1.8934E-05
+ UO=162.3 THETA=9.8330E-02 RSH=1.1900E+01 GAMMA=0.3195
+ NSUB=4.1860E+15 NFS=5.9070E+11 VMAX=1.3790E+05 ETA=1.3480E-01
+ KAPPA=5.8700E+00 CGDO=5.0000E-11 CGSO=5.0000E-11
+ CGBO=3.5843E-10 CJ=2.9806E-04 MJ=4.6657E-01 CJSW=2.0016E-10
+ MJSW=1.0000E-01 PB=8.0989E-01
* Weff = Wdrawn - Delta_W
```

APPENDIX C

0.5 µm MIETEC SPICE process parameters

```
.MODEL NT NMOS LEVEL=3
+UO=460.5 TOX=1.0E-8 TPG=1 VTO=.62 JS=1.8E-6
+XJ=.15E-6 RS=417 RSH=2.73 LD=0.04E-6 ETA=0
+VMAX=130E3 NSUB=1.71E17 PB=.761 PHI=0.905
+THETA=0.129 GAMMA=0.69 KAPPA=0.1 AF=1
+WD=.11E-6 CJ=76.4E-5 MJ=0.357 CJSW=5.68E-10
+MJSW=.302 CGSO=1.38E-10 CGDO=1.38E-10
+CGBO=3.45E-10 KF=3.07E-28 DELTA=0.42
+NFS=1.2E11

.MODEL PT PMOS LEVEL=3
+UO=100 TOX=1E-8 TPG=1 VTO=-.58 JS=.38E-6
+XJ=0.1E-6 RS=886 RSH=1.81 LD=0.03E-6 ETA=0
+VMAX=113E3 NSUB=2.08E17 PB=.911 PHI=0.905
+THETA=0.120 GAMMA=0.76 KAPPA=2 AF=1
+WD=.14E-6 CJ=85E-5 MJ=0.429 CJSW=4.67E-10
+MJSW=.631 CGSO=1.38E-10 CGDO=1.38E-10
+CGBO=3.45E-10 KF=1.08E-29 DELTA=0.81
+NFS=0.52E11
```

APPENDIX D

0.35 µm TSMC SPICE process parameters

```
.MODEL NT NMOS (LEVEL  =3
+TOX=7.9E-9  NSUB=1E17 GAMMA=0.5827871
+PHI=0.7  VTO=0.5445549 DELTA=0
+UO= 436.256147  ETA=0  THETA =0.1749684
+KP= 2.055786E-4  VMAX =8.309444E4 KAPPA=0.2574081
+RSH =0.0559398  NFS=1E12 TPG =1
+XJ= 3E-7 LD =3.162278E-11  WD=7.046724E-8
+CGDO= 2.82E-10  CGSO =2.82E-10 CGBO=1E-10
+CJ=1E-3 PB =0.9758533  MJ =0.3448504
+CJSW=3.777852E-10 MJSW=0.3508721)

.MODEL PT PMOS (LEVEL =3
+ TOX=7.9E-9  NSUB  =1E17 GAMMA=0.4083894
+ PHI=0.7  VTO=-0.7140674  DELTA =0
+ UO=212.2319801 ETA=9.999762E-4  THETA=0.2020774
+ KP=6.733755E-5 VMAX  =1.181551E5 KAPPA=1.5
+ RSH =30.0712458  NFS   =1E12 TPG=-1
+ XJ=2E-7  LD =5.000001E-13 WD=1.249872E-7
+ CGDO=3.09E-10 CGSO= 3.09E-10 CGBO=1E-10
+ CJ=1.419508E-3 PB=0.8152753  MJ=0.5
+ CJSW=4.813504E-10 MJSW=0.5)
```