FPGA-BASED UWB RADAR SYSTEM DESIGN

A Thesis submitted to the
Graduate School of Natural and Applied Sciences of Dokuz Eylül University
In Partial Fulfillment of the Requirements for the Master of Science in
Electrical and Electronics Engineering

by
Hakan UÇAROĞLU

September, 2009
İZMİR

M.Sc THESIS EXAMINATION RESULT FORM

We have read the thesis entitled **"FPGA–BASED UWB RADAR SYSTEM DESIGN"** completed by **HAKAN UÇAROĞLU** under supervision of **PROF. DR. UĞUR ÇAM** and we certify that in our opinion it is fully adequate, in scope and in quality, as a thesis for the degree of Master of Science.

.....

Prof. Dr. Uğur ÇAM

Supervisor

....

(Jury Member) (Jury Member)

Prof. Dr. Cahit HELVACI

Director

Graduate School of Natural and Applied Sciences

ACKNOWLEDGMENTS

I would like to thank my supervisor Prof. Dr. Uğur Çam for his help and support with both theoratical and practical problems.

A special thanks goes to my family for always being there for me.

Hakan UÇAROĞLU

FPGA-BASED UWB RADAR
SYSTEM DESIGN

ABSTRACT

At the begining of project we aimed to design a radar which has different structure from other radar types. After some observation we decided to design an ultra wide band radar. First of all, transmitting circuit is designed. During this design it was very important to get very narrow pulse signal. The reason of getting narrow pulse is to broaden the frequency band. Then, receiver circuit was designed. We wanted to calculate the distance of movement from the radar because of that also a delay circuit was designed. The aim of delay circuit is to receive just signals from objects which are in movement. After we received echo signal with knowledge of delay time, we could know the distance. To confirm our design, first we used a simple microcontroller. Then, we used FPGA IC to get more reliable and minimized design.

Keywords: Ultra Wide Band (UWB), transmitter, receiver, delay, microcontroller, FPGA (Field Programmable Gate Array)

FPGA TABANLI GENİŞ BANTLI RADAR SİSTEM TASARIMI

ÖZ

Tez başlangıcında proje karar aşamasındayken mevcut radar sistemlerinden farklı çalışan bir radar sistemi tasarlamayı hedefledik. Yaptığımız birkaç araştırmadan sonra geniş bant radar tasarlamaya karar verdik. Bu radar tipi, diğer radar tiplerinden farklı, çünkü çalışma prensibinde taşıyıcı sinyale gereksinim yok. İlk önce basit bir osilatör devresi kullanarak ileti anteninden göndereceğimiz ileti sinyalinin kaynağı olan 500 nano saniyelik peryoda sahip bir kare sinyal ürettik. Daha sonra bu kare sinyali ileti devresinde işleyerek çok dar bir darbe sinyaline çevirdik. Projede mümkün olduğunca dar bir darbe sinyali elde edebilmek önemli çünkü elde ettiğimiz sinyalin darlığı, kullanılacak frekans bandının genişliğini belirleyici bir etken. Daha sonra alıcı devre tasarlandı. Projede amaç hareket algılamak ve kullanıcıyı hareketin varlığı konusunda uyarmak, asıl amaç ise bu hareketin uzaklığını tespit edebilmek. Bu yüzden alıcı devrenin yanında aynı zamanda alıcı devreyi istenildiği zaman aktif edecek bir geciktirici devre tasarlandı. Geciktirici devre, alıcı devreyi aktif ettiği anda alıcı devrenin çıkış sinyalinde değişim var ise bu hareketin varlığını gösterecek. O anda geciktirici devrenin alıcı devreyi, ileti sinyalinin gönderiminden ne kadar süre sonra aktif ettiğimizi de bildiğimiz için, aynı zamanda hareketin uzaklığını da hesaplayabiliyor olacağız.

Tasarlanan devreyi doğrulayabilmemiz için ilk önce basit bir mikro kontroller kullandık. Devre doğrulandıktan sonra ise FPGA kullanarak aynı devreyi daha sadeleştirilmiş ve daha doğru çalışır duruma getirdik .

Anahtar sözcükler: Geniş Bant, İleti Devresi, Alıcı Devresi, Geciktirici Devre, FPGA

CONTENTS

Page

CHAPTER ONE

INTRODUCTION

This thesis project is done to get a radar which has very different operating features from the other known radars. The focus of this thesis is on the transmitting and receiving pulse signals and on commenting the received signal. For transmitting and receving circuits high frequency transistors are used. This design was also built as a demonstrator and the actual hardware is evaluated. The design consist of two parts: first part is high frequency part, the second part is low frequency part. High frequency part consist of transmiting and receiving circuits, low frequency part consist of circuits that comments received signals and microcontroller circuits.

1.1 Types of RADAR Systems

RADAR is an acronym for, “Radio Detection and Ranging.” RADAR uses radio waves to detect and determine the range of a target item. There are two basic radar types: Pulse Transmission and Continuous Wave Radars.

1.1.1 Pulsed Radar

A pulse radar transmits a sequences of short pulses of RF energy. By measuring the time for echoes of these pulses scattered off a target to return to the radar, the range to the target can be estimated by the pulse radar.

The major components of a pulse radar are:

- the transmitter, consisting of an oscillator and a pulse modulator;
- the antenna system, which passes electromagnetic energy from the transmitter to the transmission medium, and receives reflections from the target;
- the receiver, which amplifies the signal received by the pulse radar and detects returns from targets;
- interfaces, including displays and interfaces to other electronic systems.

(PULSE RADAR, Radar Glossary, 2009)

1.1.2 Continuous Wave Radar

Continuous wave radar (CW radar) continually transmits energy in the direction of the target and receives back reflection of the continuous wave. A continuous wave radar can provide velocity information by comparing the differences in the transmitted and received waves and making use of the Doppler effect (CONTINUOUS RADAR, Radar Glossary, 2009).

A disadvantage of continuous wave systems is they can only detect moving targets because targets at rest do not cause Doppler shift. A version of this type uses an amplitude or frequency modulation technique to overcome this problem.

Except these two radar system types there is also one new technology from commercial or civilian application viewpoint, **Ultra Wide Band**. Ultra Wide Band Radar sytstem operation is similar to Pulsed Radar System operation. The difference between these two radar systems is; in Ultra Wide Band Radar systems energy is spread to an extremely wide band of frequencies. But in Pulsed Radar Systems the energy is concentrated at a small range of frequencies. With this new technology, we can add one more radar system to under Radar types topic.

1.1.3 Ultra Wide-Band Radar

When Guglielmo Marconi made radio history by transmitting the Morse code for the letter “S” across the Atlantic ocean on December 12, 1901, little did he know that his brillant idea of using pulses of electromagnetic energy for radio communication would resurface nearly a hundred years later in the frm of ultra-wideband (UWB) technology (Manandhar D., Shibasaki R., 2003).

A very wide bandwidth means better multipath mitigation, interference mitigation by using spread spectrum techniques, improved imagining and ranging accuracy, more users and higher data rate. A lower center frequency for a given bandwidth allows better materials penetration. UWB device transmits millions of very low power radio pulses (impulses), each typically lasting less than a nanosecond

over a very large radio spectrum. UWB system has no carrier. Carrierlessness and very wide bandwidth are two major characteristics of UWB.

UWB signal can be modeled as Gaussian monopulse signal. As we know monopulse with a narrow pulses produces a wide bandwidth signal. The Gaussian function in time domain is;

$$v(t) = \frac{t}{\tau} e^{-\left(\frac{1}{\tau}\right)^2} \tag{1.1}$$

where;

ô is the time decay constant that determines the monocycle's duration

UWB pulses are also modeled by normalized second derivative of the Gaussian monopulses, equation (1.2) is shows this;

$$v(t) = \sqrt{\frac{4}{3\tau\sqrt{\pi}}}\left(1 - \left(\frac{t}{\tau}\right)^2\right) e^{-0.5\times\left(\frac{t}{\tau}\right)^2} \tag{1.2}$$

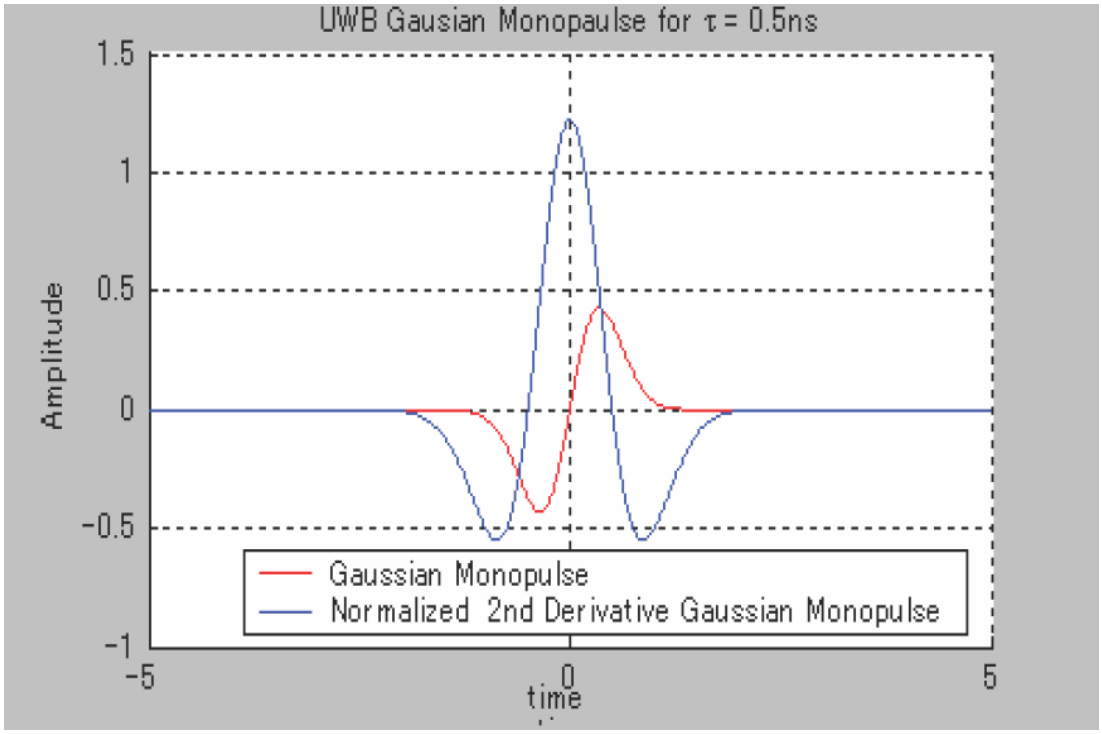

Figure 1.1 Gaussian pulse generated from Equation (1.1) and Equation (1.2)

The pulse itself contains no data. Therefore long sequences of pulses defined by the pulse repetition frequency (PRF) with data modulation are used for data transmission. Generally, in UWB systems, a transmitter emits sequences of pulses that are detected by a corresponding receiver whose front end amplifiers are synchronized and time-gated to the transmitted pulse sequences. Data information that is to be sent is modulated onto certain parameters of the transmitted pulse. These parameters may include the pulse position, amplitude or orientation (Manandhar D., Shibasaki R., 2003).

1.2 History of UltraWideBand (UWB) Radar and Communications

Contributions to the development of a field addressing UWB RF signals commenced in the late 1960's with the pioneering contributions of Harmuth at Catholic University of America, Ross and Robbins at Sperry Rand Corporation, Paul van Etten at the USAF's Rome Air Development Center and in Russia. The Harmuth books and published papers, 1969-1984, placed in the public domain the basic for UWB transmitters and receivers. At aproximately the same time and independently, the Ross and Robbins (R&R) patens, 1972-1987, pioneered the use of UWB signals in a number of application areas, including communications and radar and also using coding schemes. Van Etten's empirical testing of UWB systems resulted in the development of system design and antenna concepts (Van Etten, 1977). In 1974 Morey designed a UWB radar system for penetrating the ground, which was to become a commercial success at Geophysical Survey Systems, Inc. (GSSI). Other subsurface UWB radar designs followed (e.g., Moffat & Puskar, 1976). The development of sample and hold receivers (mainly for oscilloscopes) commercially in the late 1960s, e.g., at Tektronix Inc., was also, unwittingly, to aid the developing UWB field. For example, the Tektronix Time Domain Receiver plug-in, model 7S12, utilized a technique which enabled UWB signal averaging - the sampling circuit is a transmission gate followed by a short-term integrator (Tektronix, 1968). Other advances in the development of the sampling oscilloscope were made at the Hewlett Packard Company. These approaches were imported to UWB designs. Commencing in 1964, both Hewlett Packard and Tektronix produced the first time domain instruments for diagnostics. In the 1960s both Lawrence Livermore National Laboratory (LLNL) and Los Alamos National Laboratory (LANL) performed orginal

research on pulse transmitters, receivers and antennas. Cook & Bernfeld's book (1967) summarized developments in pulse compression, matched filtering and correlation techniques which had begun in 1952 at the Sperry Gyroscope Company. In the 1970s LLNL expanded its laser-based diagnostics research into pulse diagnostics (Barrett, Terence W., 2000).

Thus, by the early 1970s the basic designs for UWB signal systems were available and there remained no major impediment to progress in perfecting such systems. In fact, as is shown below, by 1975 a UWB system – for communications or radar – could be constructed from components purchased from Tektronix. After the 1970s, the only innovations in the UWB field could come from improvements in particular instantiations of subsystems, but not in the overall system concept itself, nor even in the overall subsystems' concepts. The basic components were known, e.g., pulse train generators, pulse train modulators, switching pulse train generators, detection receivers and wideband antennas. Moreover, particular instantiations of the subcomponents and methodologies were also known, e.g., avalanche transistor switches, light responsive switches, use of "subcarriers" in coding pulse trains, leading edge detectors, ring demodulators, monostable multivibrator detectors, integration and averaging matched filters, template signal match detectors, correlation detectors, signal integrators, synchronous detectors and antennas driven by stepped amplitude input (Barrett, Terence W., 2000).

In 1994, T.E. McEwan, then at LLNL, invented the Micropower Impulse Radar (MIR) which provided for the first time a UWB operating at ultralow power, besides being extremely compact and inexpensive (McEwan, 1994, 2000). This was the first UWB radar to operate on only microwatts of battery drain. The methods of reception of this design also permitted for the first time extremely sensitive signal detection. (Barrett, Terence W., 2000).

1.3 Objectives of Following Chapters

In chapter two, initially a block diagram of the design is given. Then, each block in block diagram is explained shortly. In this chapter it is aimed to give foreknowledge to reader about this design.

In chapter three, circuit diagrams of each blocks explained in chapter two are given. Operating principles of each circuits are explained. Outputs of circuits are simulated and these simulation outputs and scope outputs are given. At the end of this chapter scope outputs of thesis are given for no motion, for slower motion, for single motion and for continuous motion.

In chapter four, initially some information are given about FPGA IC and evalution board. The blocks on evalution board are introduced. Then, the software of project is explained by using flow chart. Simulation output and RTL schematic of software are given.

In chapter five, some constraints we have faced during design are showed. To get rid of these constraints alternative ways are explained. Also, some viabe imrovements are given to make the design more efficient.

In chapter six, conclusion of thesis is given.

CHAPTER TWO

DESIGN IDEA

2.1 Block Diagram of UWB System Design

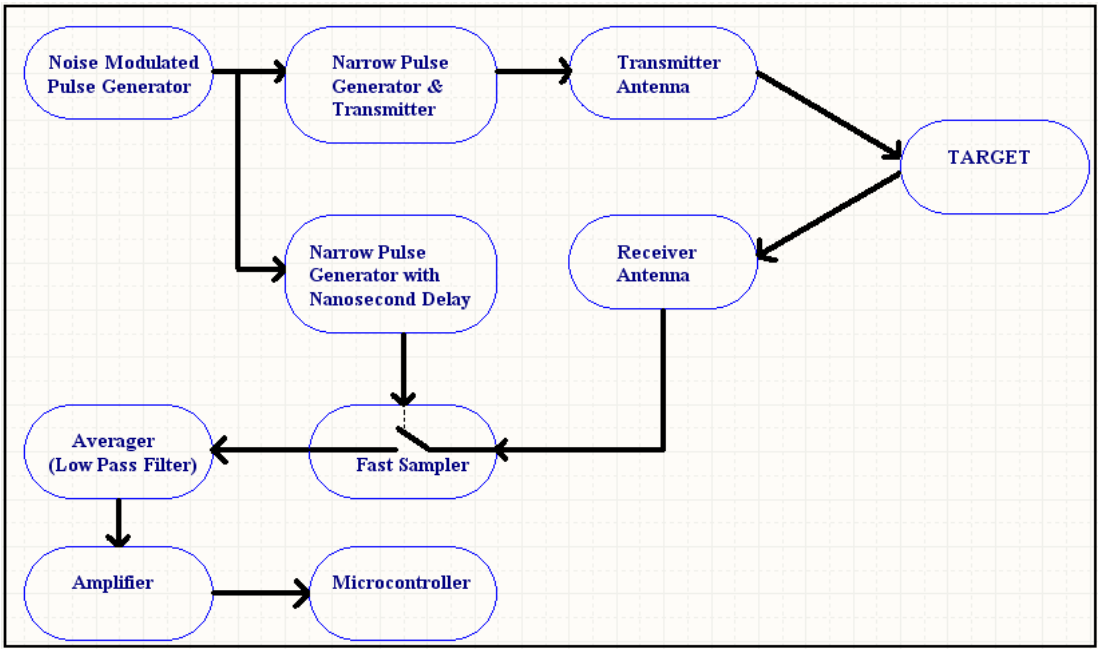

Figure 2.1 Block diagram of ultra wide band system design

Block diagram of our design is shown in Figure 2.1. The block diagram is prepared according to hardware and software requirements . All system is partitioned to understand each block . Now, each block will be explained shortly.

2.1.1 Noise Modulated Pulse Generator

Pulse generator makes a trigger for all system and generates a pulse. This pulse is fed to Narrow pulse generator of transmitter and delay circuits. Generated pulse has determined frequency and duty cycle. To be able to vary the pulse width and duty cycle with great resolution increases the pulse rate, and this gives us a chance to detect faster moving targets.

2.1.2 Narrow Pulse Generator & Transmitter

Source of this block is the generated pulse in Pulse Generator block. By using a RF transistor this pulse is converted to very narrow signal. The aim of generating a narrow pulse signal is the main topic of this thesis. There are a lot of ways to generate a pulse. The shortest pulses so far are on the order of 100 Atto-seconds. One method involves the use of a mismatched transmission line. With one end terminated, when a rising edge is sent into the transmission line, the reflection cancels the input signal. For example, a 100-foot long cable gives a delay of about 300 nS. Another method is to use a step recovery diode. The step recovery diode can give 0.8V pulses in the 100 pS range at a reasonable cost. Another possible method is to use a Limited Space Charge Accumulation Diode. This device (similar to a Gunn diode) can generate pulses on the order of 7 nS with overtones carrying some usable power out to about 1 pS.

In our thesis we used a simple RC differantiator in front of a high frequency transistor. In the next chapter, the operating principle of our trasmitter circuit will be explained deeply. .

2.1.3 Narrow Pulse Generator with Nano Second Delay

This block is approximately same with the previous one, Narrow Pulse Generator & Transmitter. In radar applications moving or stationary objects are detected. Of course there is distance between stationary radar system and stationary or moving target. Tranmitted signal should travel this distance and after it reflected from target echo signals should travel same distance, then this echo signal is emitted by receiver antenna. If we suppose the target is placed to 1 meter distance to radar, the time the tramsmitted signal to get back can be calculated from below formula:

$$t_{echo} = 2 \times \frac{dist}{c} \tag{2.1}$$

where

$\mathbf{t_{echo}}$ is the time for echo signal

dist is the distance between radar and target

c is the speed of light (300000 km/s)

2.1.4 Transmitter Antenna

Tranmitter antenna transmits the created narrow pulse to air. The antenna parameters, dimensions and type of it is very important to send pulses with minimum loss. Antenna type is determined according to the frequency and bandwidth of pulse signal.

2.1.5 Receiver Antenna

Receiver antenna emits the echo signals reflected from target. Since the pulse signal tranmitted loses power during travel from transmitter antenna to target and target to receiver antenna, signals that have very low power are emitted by receiver antenna. So, receiver antenna choice is also very important.

2.1.6 Fast Sampler

Fast sampler works as a mixer. The signals emitted by receiver antenna comes to fast sampler circuit. The aim of fast sampler circuit is to pass echos just coming from targets at desired distance. This means, fast sampler circuit does not pass all coming echos. To realize this characteristic, this circuit should be enabled just after the time needed for tranmitted signal travelling from transmiter antenna to target and from target to receiver antanna. As it is explained in Narrow Pulse Generator with Nano Second Delay section, this time can be calculated with equation 2.1.

2.1.7 Averager (Low Pass Filter)

Fast sampler output signal is a constant dc signal. If there is a movement at desired distance this dc voltage change with small variations. By averager circuit just these small variations are passed, other high frequncy variations are ignored.

2.1.8 Amplifier

Small variations gotten from averager circuit should be amplified to get suitable voltage levels for next section, microcontroller. We need to amplify because these voltage variations are in micro volt levels. Without amplifier sections these variations are meaningless.

2.1.9 Microcontroller

Microcontroller interprets the variation gotten from amplifier section. If there is logical variation, this means there is movement at desired distance, if there is no any variation this means there is no movement. Microcontroller section also supplies the communication between the radar system and computer. The variations can be watched on computer screen by the help of this communication. Microcontroller also supplies a pulse width modulated signal for varicap diode in Narrow Pulse Generator with Nano Secon Delay circuit. This PWM signal determines the dc voltage level that will be applied to varicap diode, and this dc voltage adjusts varicap diode capacitive level. With varying capacitive level, we can adjust the delay time that will be applied to generated narrow pulse signal.

We used PIC16F877 microntroller for this pupose. Because it is easy to communicate with computer and creating PWM signal for varicap diode. In the following sections, you can see that instead of a microcontroller we realized same radar system by using FPGA.

CHAPTER THREE

IMPLEMENTATION AND DETAILS OF CIRCUITs

In this chapter we will give some details about operations of circuits. As explained in Chapter 2, design is a combination of circuits that either have different duty to realize.

3.1 Noise Modulated Pulse Generator Circuit Description

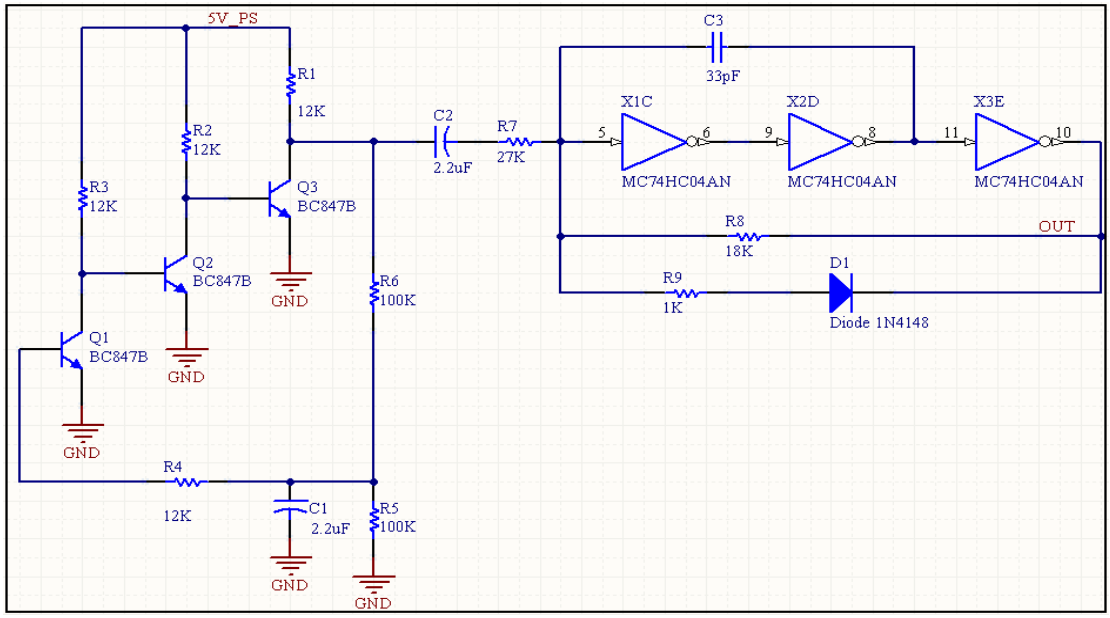

Figure 3.1 Noise modulated pulse generator

The circuit shown in Figure 3.1 shows the noise modulated pulse generator used in a patent from LLNL. The values of the used components were experimentally found according to need for period of generated pulse we need.

The R7 (27KΩ) resistor at the center of the figure can be changed to vary the modulation depth, that is the random variation of pulse repetition period, while mean pulse repetition frequency can be varied changing the value of the C3 (33pF) capacitor or the R8 (18KΩ) resistor in the oscillator. We need a pulse train signal which has 500ns period. So, the circuit component values were choosed according to that. The signal out is at TTL level. Output signal we got from this circuit is shown in Figure 3.2.

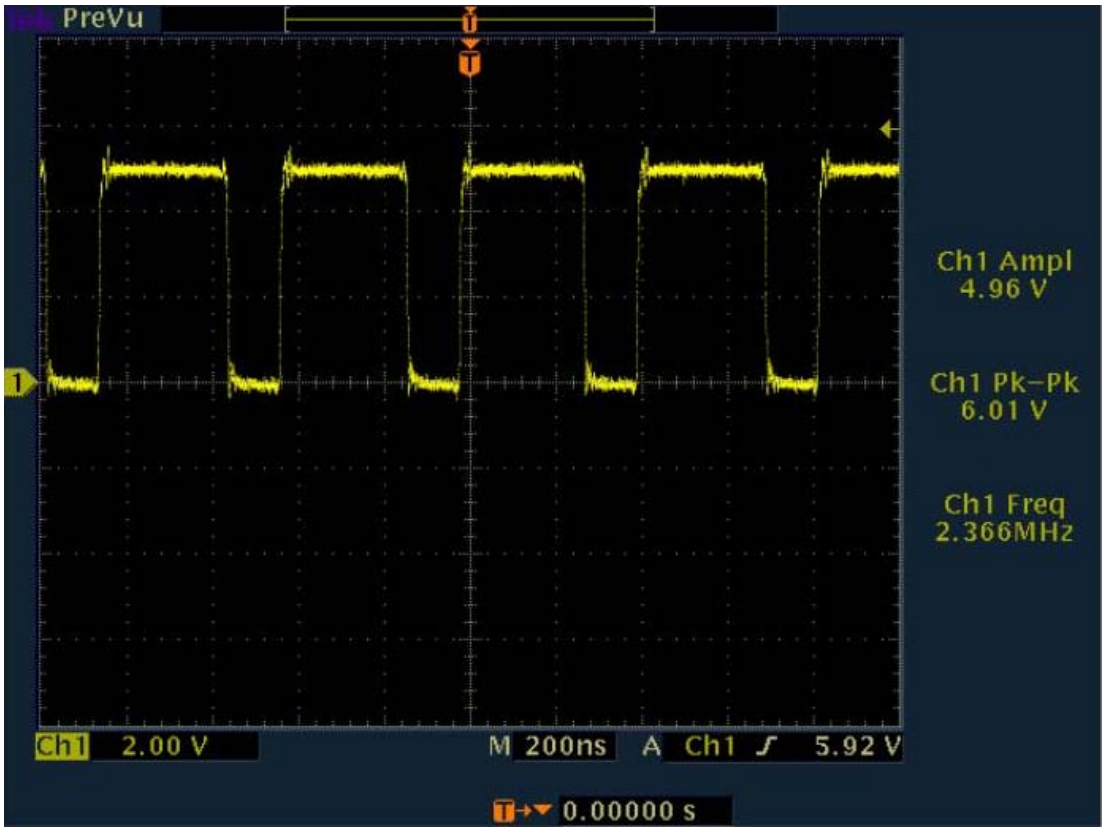

Figure 3.2 Output signal of noise modulated pulse generator

This output signal is the source of transmit signal. As can be seen from figure it has 500ns period. This means the transmit signal will be radiated from transmitting antenna with 500ns period.

3.2 Narrow Pulse Generator & Transmitter Circuit Description

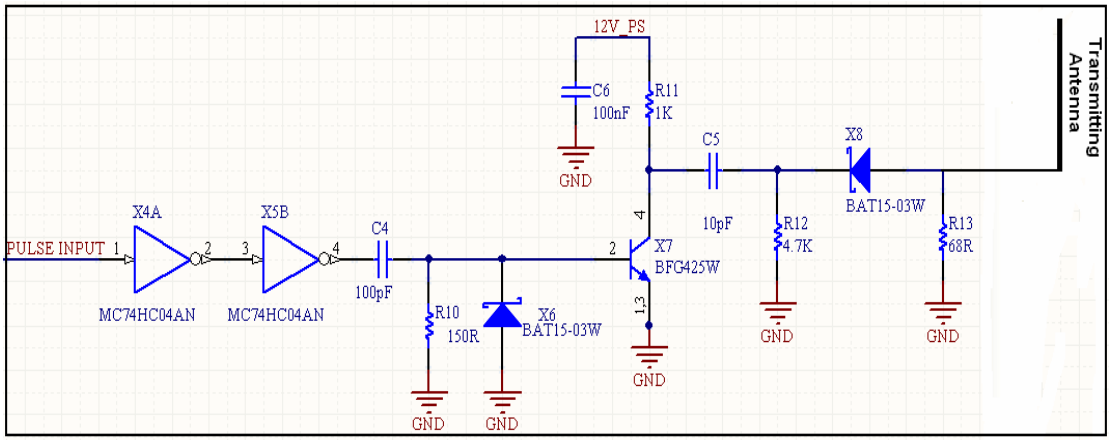

Figure 3.3 Narrow pulse generator and transmitter circuit

The circuit in Figure 3.3 converts the pulse signal gotten from Noise Modulated Pulse Generator to the narrow pulses that will be sent to air by tranmitter antenna. The operating principle of this circuit is very simple. Generated pulse signal first of all enters X4 and X5 (74F04) ICs. These ICs serve three purposes: they enable the transmitter to accept the positive going pulses, buffer the transmit section, and equal out the delay between the transmitter and receiver to allow detection at shorter distances. Output of X5 gives use a signal approximately same with the generated pulse signal by pulse generator. The difference is delay between two signal.

C4 and R10 serve as a differentiator. The aim of this capacitor and resistor circuit is to differentiate the output of X5 and to create a triggering signal for RF transistor (X7).

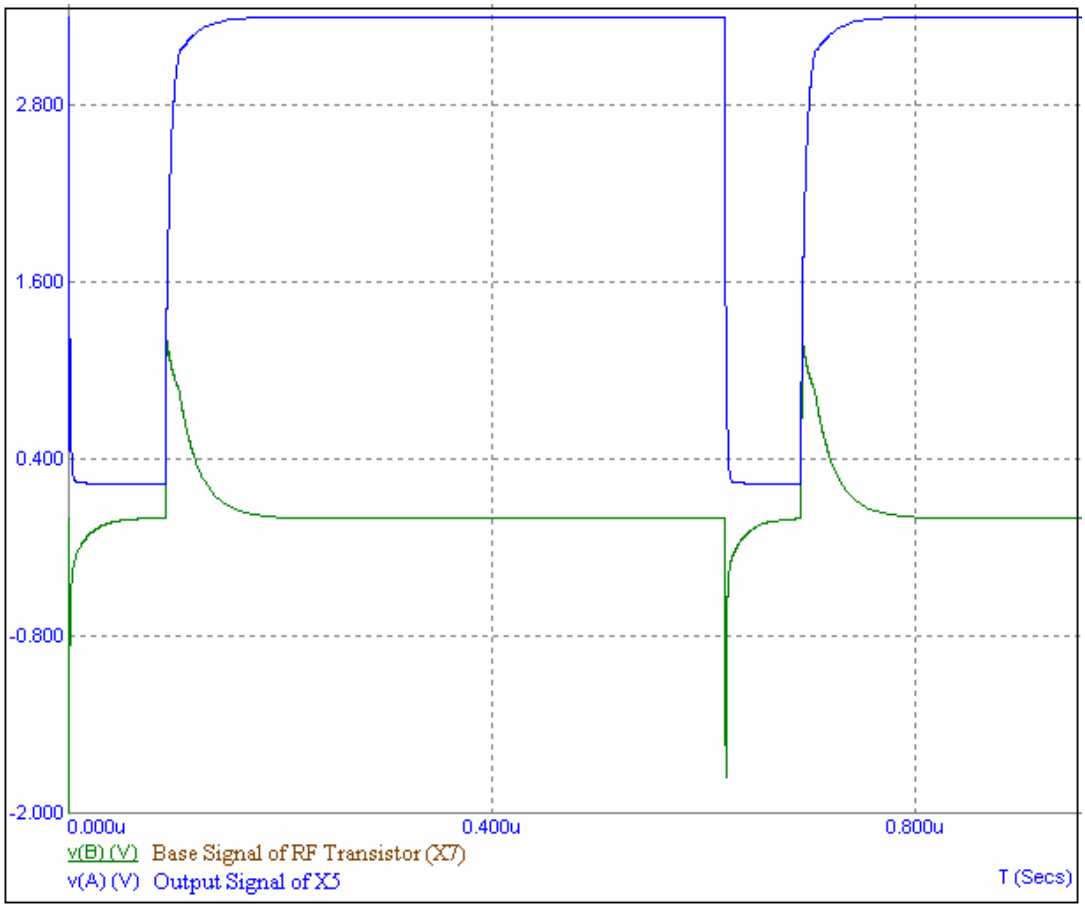

Figure 3.4 Output signal of X5 and input signal of X7

Figure 3.4 shows the output signal of X5 with blue line and input signal of X7 with brown line.

The silicon schottky diode (X6) BAT15-03W has low noise figure and it is a low barrier type diode. It can be used in applications up to 12GHz (Infenion Technologies, 2001). This diode decreases the negative effect of differentiated signal. Because we need just positive side of this signal to disable and enable the RF transistor (X7).

BFG425G (X7) is a RF transistor that has very high power gain and low noise figure. It is generally used in RF applications. Its name is NPN 25GHz wideband transistor (Philips Semiconductors, 1998). There is a small capacitor (C5=10pF) on the collector of the transistor. When it is not conducting, this capacitor charges up to the supply (+12V) at a rate limited by a R11=1 kΩ and R12=4.7 kΩ. The pulse is generated when the transistor goes into conduction and shorts the capacitor C5 to ground. It discharges quickly and generates a pulse.

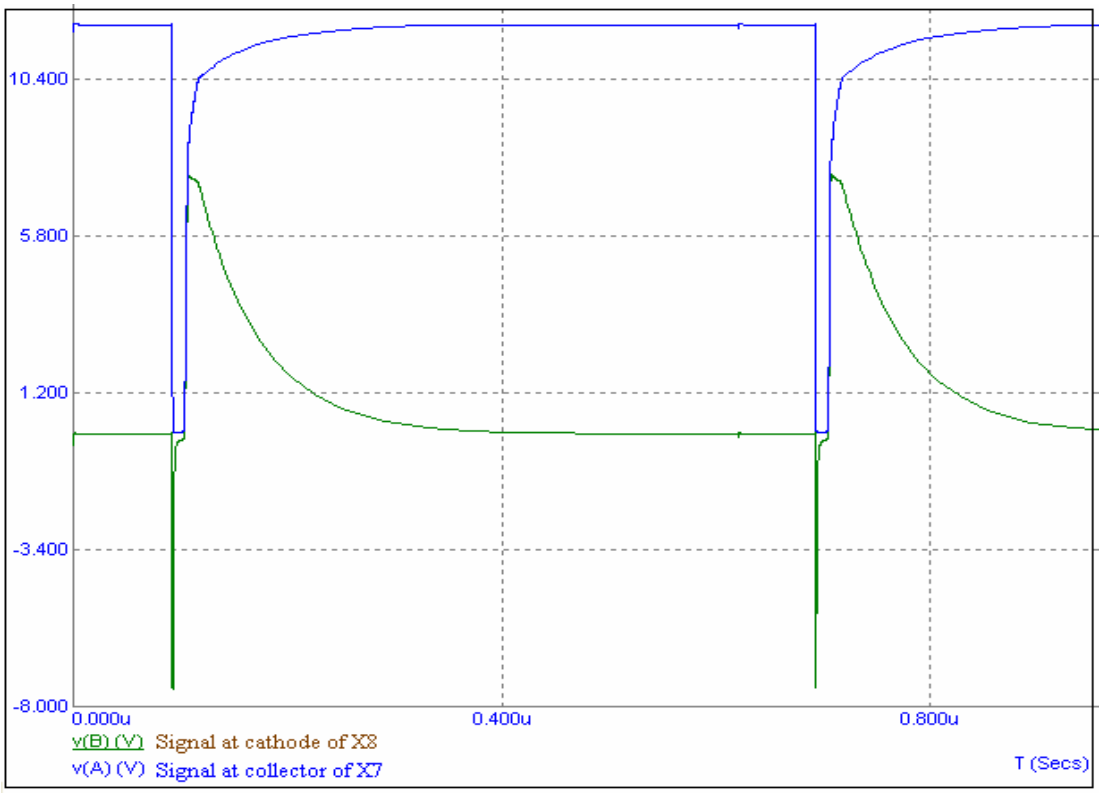

Figure 3.5 Signals at collector of X7 and cathode of X8

When transistor is not in conduction mode, cathode of it is at supply voltage. When it is in conduction mode cathode voltage is 0V. So, while transistor is in cut-off mode, capacitor at collector charges up to supply voltage at a rate limited by R11 and R12. When transistor passes to the conduction mode, the voltage at capacitor discharges suddenly. The negative peaks shown in Figure 3.5 is the result of this operation. These peaks will be our transmit signal after one more operation on it. Negative peak is selected as a tranmit signal because it is very narrow signal and we need such a signal for UWB system application.

Positive side of gotten signal can be removed by using again silicon schottky diode (X8). X8 passes just negative side and we got transmit signal shown in Figure 3.6.

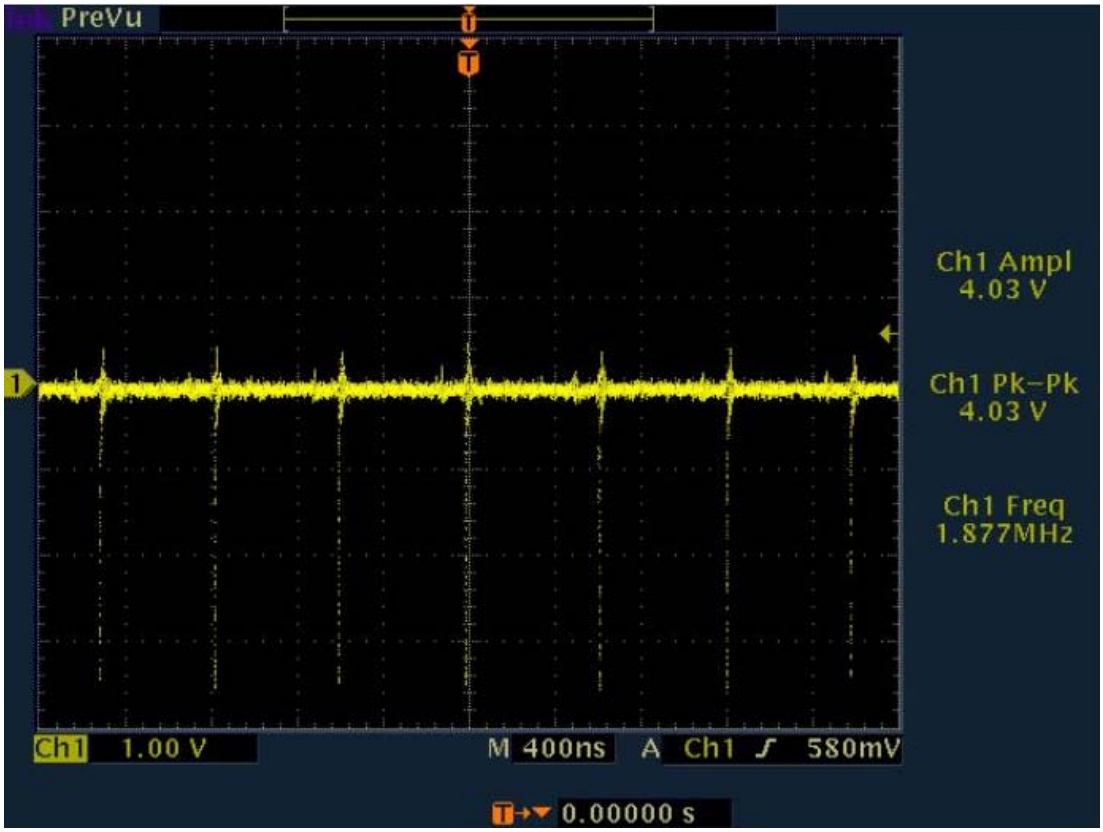

Figure 3.6 Transmit signal train

Tansmit signal has 500ns period same with the pulse signal we got from noise modulated pulse generator. The amplitude of a pulse is approximately 3.5V. One pulse signal can be seen more deeply in Figure 3.7.

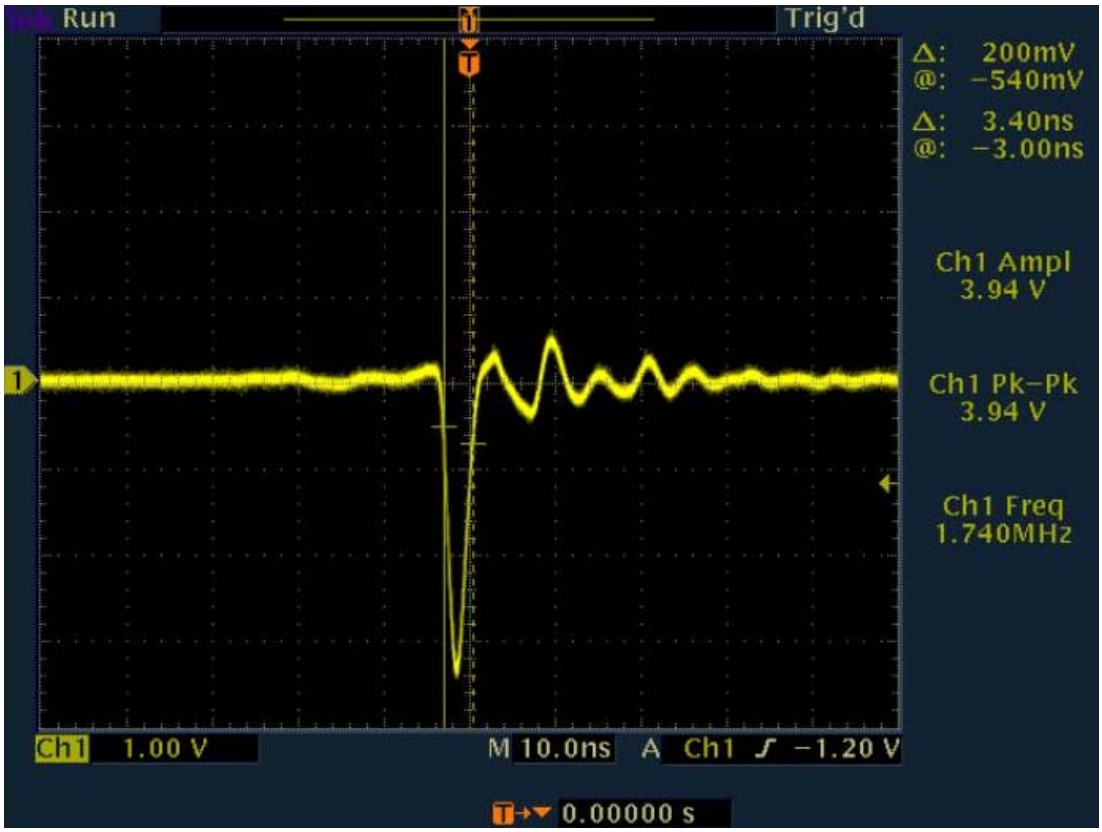

Figure 3.7 One transmitted pulse signal

The pulse width of this signal is 3.4ns. It is better to get more narrow signal. With this circuit that is the best we can get. This signal radiates from tranmitter antenna. As you see there is no carrier signal, no phase information. Just a narrow pulse signal, that is all we need for this UWB radar system.

In UWB radar applicatins tranmitter sends power, not voltage. So, let's try some trivial math to have an idea of the power out from this UWB transmitter. The energy stored in the capacitor C5 (10pF) when this is charged at +9.8V is:

$$E = (1 / 2)*C*V^2 = (1 / 2)*(10*10^{-12})*(9.8^2) = 480*10^{-12}\ J \qquad (3.1)$$

Supposing this energy being completely delivered in a pulse having a width (Pw) of 3.4ns, 141.17 mW power pulse results:

$$W = E / Pw = (480*10^{-12}) / (3.4*10^{-9}) = 141.17 \text{ mW}. \quad (3.2)$$

Considering the duty cycle, taking into account mean pulse repetition period (PRF=500ns), we obtain 1.44 mW.

$$W' = E / PRF = (480*10^{-12}) / (500*10^{-9}) = 0.96 \text{ mW} \quad (3.3)$$

Of course these calculation are realized according 100% efficiency. But this figure is surely very much optimistic. A 50% or less is more realistic estimate giving a final, mere, 500uW mean irradiated power. If we theoratically suppose that this power is spread over a 2000 MHz band, we obtain a 50pW/KHz spectrum usage.

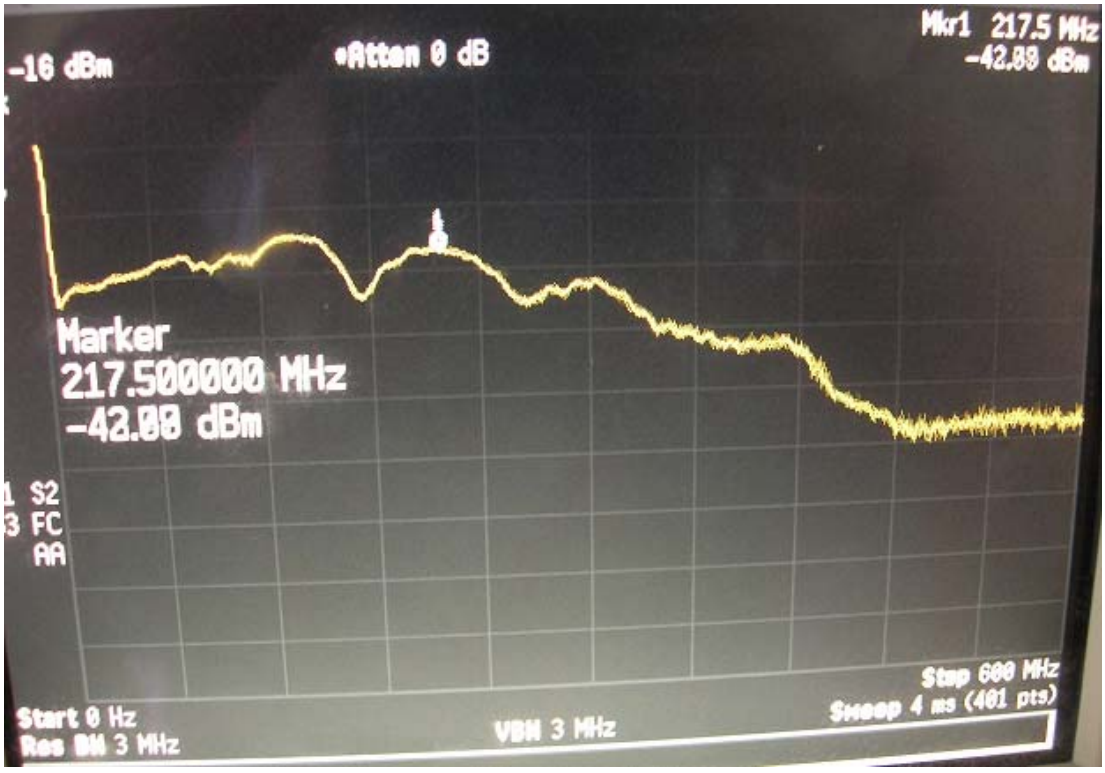

Figure 3.8 Spectrum analyzer output of transmitted signal

3.3 Narrow Pulse Generator with Nanosecond Delay Circuit Description

In previous section 3.2, we described the circuit for generating a narrow pulse. This narrow pulse is used as a transmit signal. The aim of this system is to detect a movement, but more important aim is to know the distance of detected movement. Becasue in radar applications just to know whether there is a movement or not is not enough information. You should also give the distance of movement. Because of that there should be one more circuit design that will trigger the receiver circuit at adaqute time. The time that receiver circuit will be active can be calculated from equation 2.1. For example, a short (~3ns) pulse should be able to go one meter and return in 6.7ns. This can be calculated easily from equation 2.1. This means after transmit signal sent from tranmitter antenna, receiver circuit should be activate after 6.7ns to learn whether there is a movement at 1 meter distance.

To realize this operation, approximately same pulse signal in section 3.2 should be created with delay of determined time before.

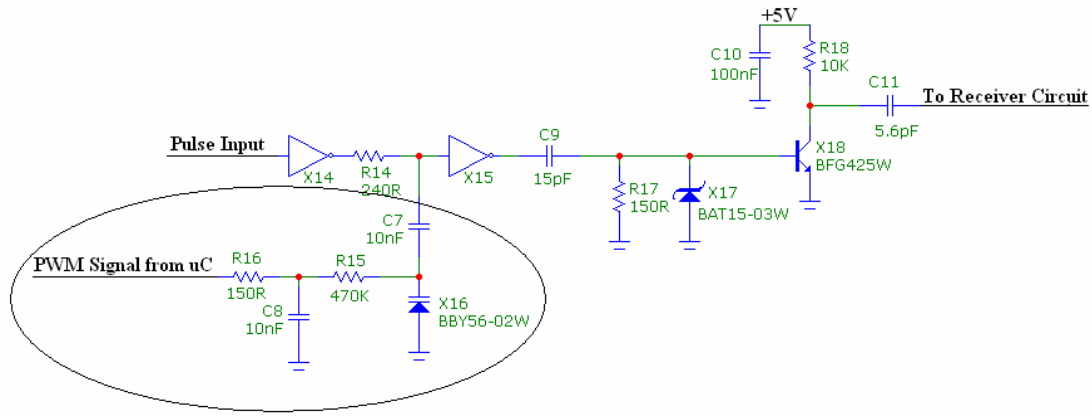

Figure 3.9 Narrow pulse generator with nanosecond delay circuit

As can be seen from Figure 3.9, this circuit is approximately same with transmit pulse signal generator. The only difference is circled part in Figure 3.9. The circled circuit gives desired delay to the pulse signal. This control is supplied by the help of software. X16 is a silicon tuning diode and this diode gives a chance to control delay time with software. The other name of this diode is varicap diode. The most important feature of this diode is, it has variable capacitance value and its capacitance changes according to the dc voltage level applied to cathode of it.

In other words its capacitance value changes according to reverse voltage level of diode. The equation of this capacitance value is;

$$\text{Diode capacitance } C_T = f(V_R) \quad f = 1\text{MHz} \tag{3.4}$$

C_T is the diode capacitance,
f is the operating frequency,
V_R is the reverse voltage.

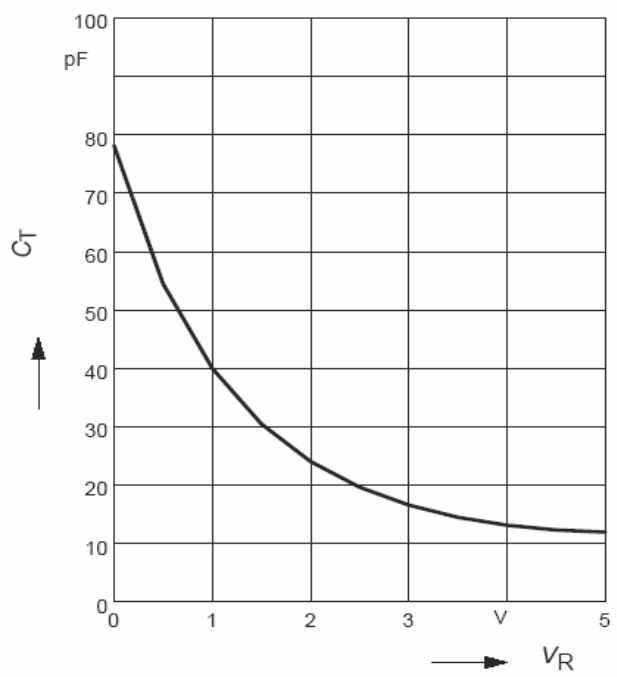

Figure 3.10 Characteristic curve for V_R – C_T relationship

This diode has excellent linearity, low series resistance and very low capacitance spread (Infenion Technologies, BBY56-02W, 2003).

By applying a pulse width modulated signal to cathode of this diode, we could change reverse voltage of it. So, we could get a varying capacitance. With varying capacitance, we could apply desired delay to the pulse signal. We applied PWM signal to cathode of X16 from microcontroller.

To show the affect of varicap diode, the circuit in Figure 3.9 is simulated and we got output signal from output of X15. The result is shown in Figure 3.11.

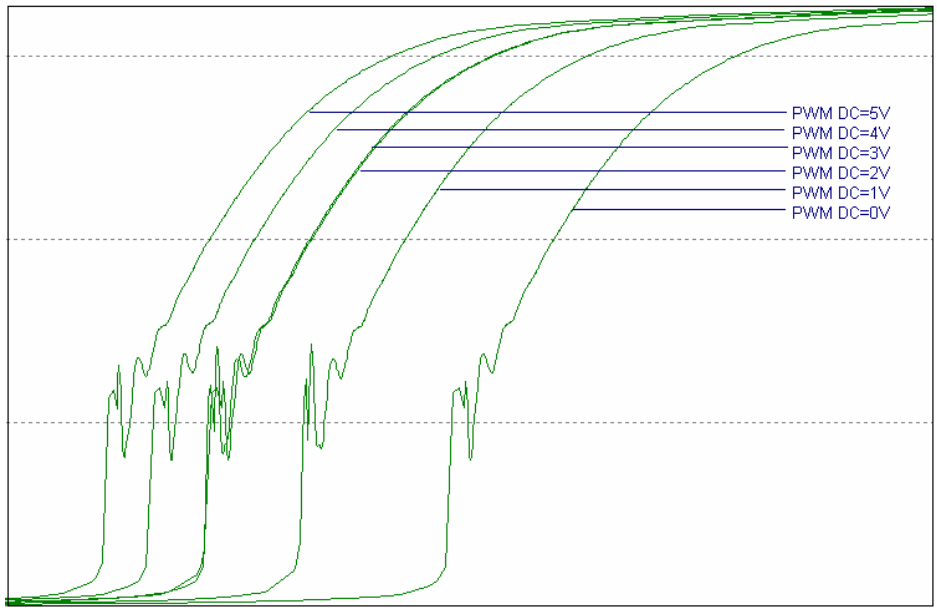

Figure 3.11 Delay time on pulse signal with varying reverse voltage

To show the delay detaily, the raising edges of pulse signals with varying reverse voltage of varicap diode are just showed. Simply, what we did is to vary the capacitance value of RC circuit, which is created by R14 and combination of C7, X16. R14 and C7 has constant values but the capacitance of X16 can be varied.

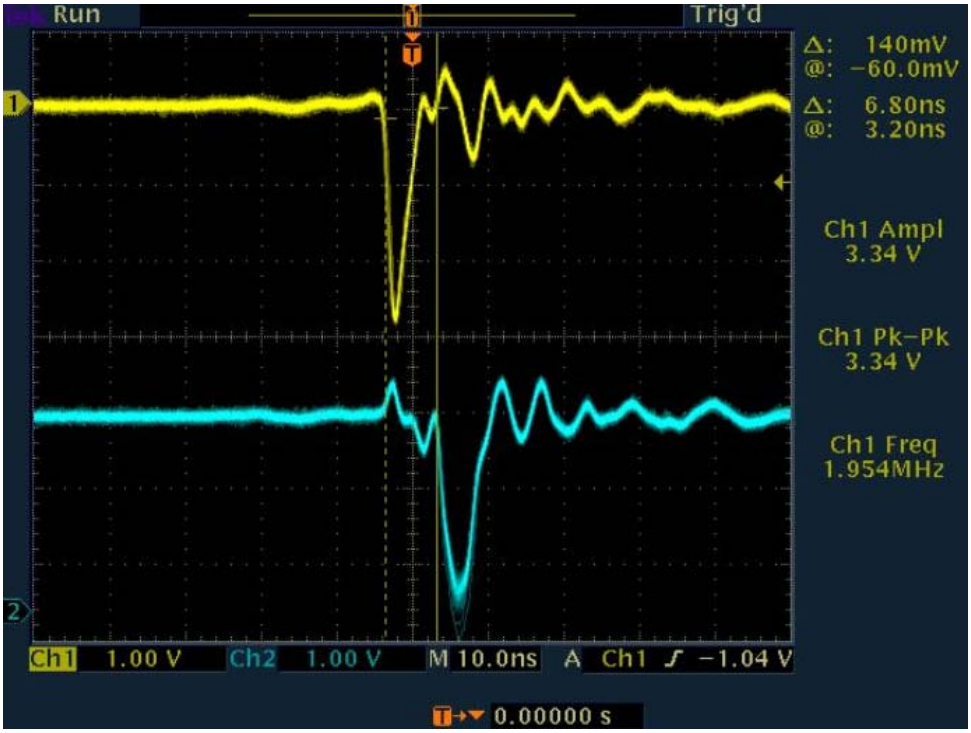

Figure 3.12 Transmit signal versus delayed signal

In Figure 3.12 both transmit and delayed signals are shown. Scope channel 1 is connected to transmit signal, scope channel 2 is connected to delayed signal. The time difference between these two signals are adjusted to 6.8ns. Narrow pulse is sent to air by transmitter antenna and after 6.8ns the receiver is activated. This means that the movements at distance 1 meter are detected with this configuration.

3.4 Fast Sampler & Intergrator Circuit Description

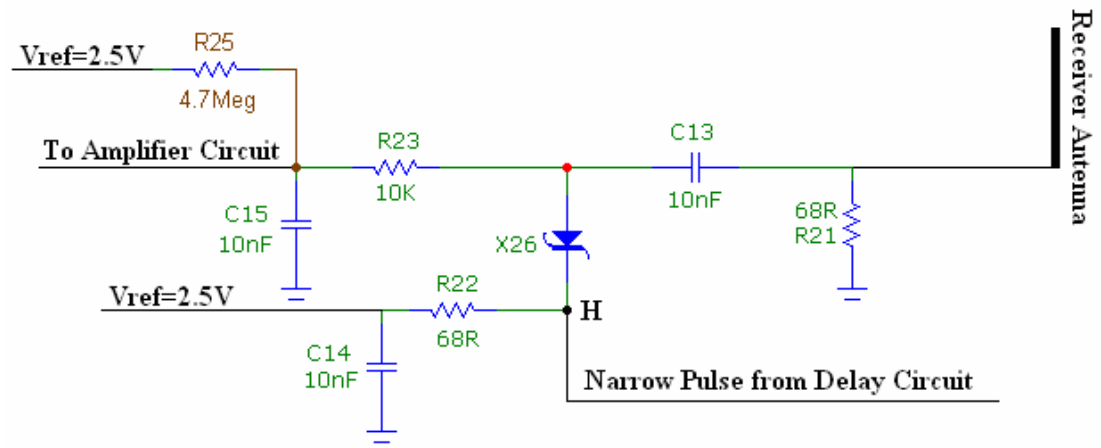

Figure 3.13 Fast sampler and integrator circuit

The transmitted signal travels from the antenna and an attenuated echo returns to the antenna system. If the target is not at the expected distance, the system ignores it. If the target is at the correct distance, the return signal is detected by the diode gate and averaged by the integrator section.

As a signal is impressed onto the receiver antenna, it appears on the antennas and thus the 68Ω resistor. When a valid echo appears and the sampling diode (X26) is pulled low by the delayed pulse at point “H”, the diode conducts and the signal is dumped into the input capacitor. When the pulse releases the cathode of the gate diode, the signal appears at the signal input. This increases the signal-to-noise ratio by recording the voltage only when the signal is present, and ignoring time periods when there is no signal and only noise.

It is known that signal-to-noise ratio improves with the square root of the number of averaged pulses. By considering the mean number of received echoes during a time epoch equal to the time constant of the low pass filter we get a 30 dB

improvement in the signal-to-noise ratio figure before any active amplification of the signal. The time constant of the averager is:

$$\tau = 2\pi RC = 2 \cdot \pi \cdot 10^{4} \cdot 10^{-8} = 628\pi s \tag{3.5}$$

So the number of received echoes during a time epoch equal to the time constant of the averager is:

$$P_n = \frac{\tau}{\overline{PRP}} = \frac{628 \cdot 10^{-6}}{500 \cdot 10^{-9}} = 1256 \tag{3.6}$$

It follows an increase of the signal-to-noise ratio of:

$$S/N = 20\log\left(\sqrt{P_n}\right) = 20\log\left(\sqrt{1256}\right) = +31\,\mathrm{dB} \tag{3.7}$$

628us time constant in the receiver limits the target detectable moving frequency to about 1200 Hz, that is a maximum target speed is defined above which the UWB radar is no more able to detect it.

3.5 Amplifier Circuit Description

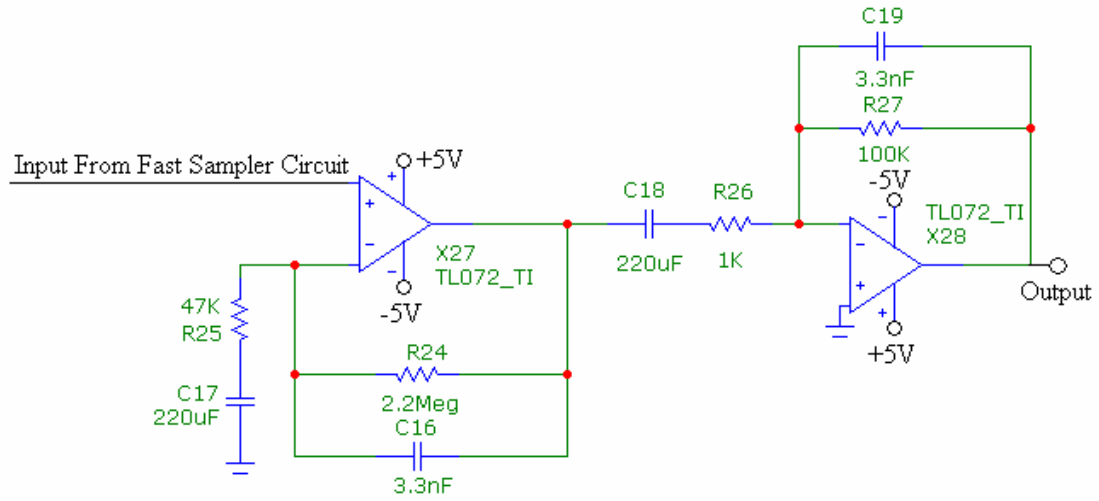

Figure 3.14 Amplifier circuit

In the amplifier section we used TL072 JFET input operational amplifier (Texas Intruments, TL072, 1996). The signal comes from integrator which is at the output of fast sampler circuit, and this signal is in the range of volt. But the variations on this signal is in the range of micro volts. These variations say us whether there is a movement at the desired distance or not. So these variations should be amplified to interpret the coming signal.

Second amplifier X28 is used as a active first order band pass filter. A human movement is approximately 16Hz. So the amplifier circuit should not pass all the frequencies. Because steady echos can come from all around the environment. This means that anything not moving goes unnoticed by the radar. With component values in Figure 3.13, we realized a simulation and we gave a pulse signal which has 1uV amplitude. The result is shown in Figure 3.15.

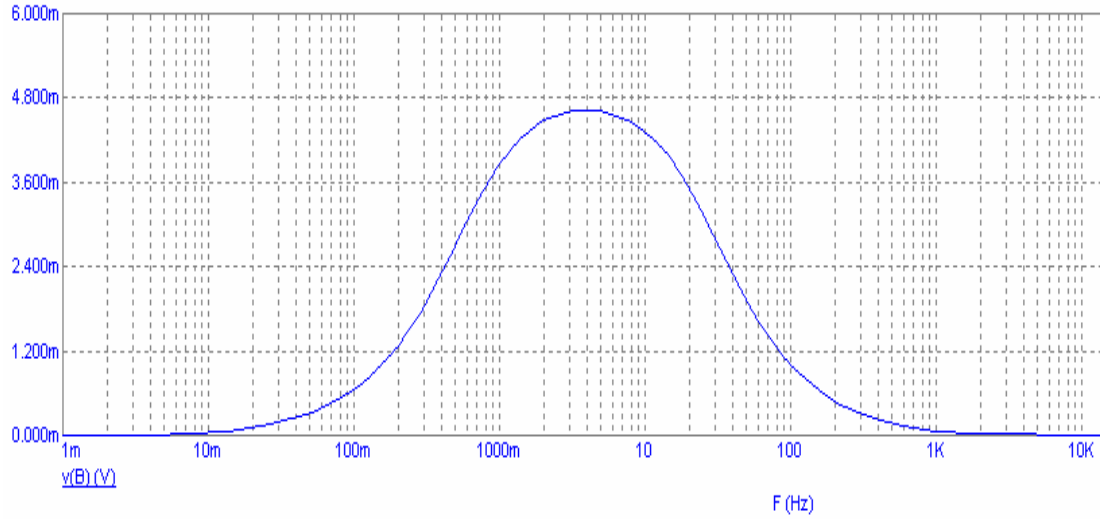

Figure 3.15 Characteristic curve of band pass filter in amplifier circuit

The gain is eqaul to –R27/R26. This means we got gain of 100. If there is no movement at the desired distance, the output signal of amplifier section is approximately a constant dc voltage. If there is a movement, then output signal swings between -5V and +5V.

3.6 The Output Graphs of Project

The output graphs are gotten when there is no any movement and there is a movement at the desired distance. We attached a scope probe to the output of amplifier circuit. Then we settled the delay signal according to measurement to detect the movement at 5 meters.

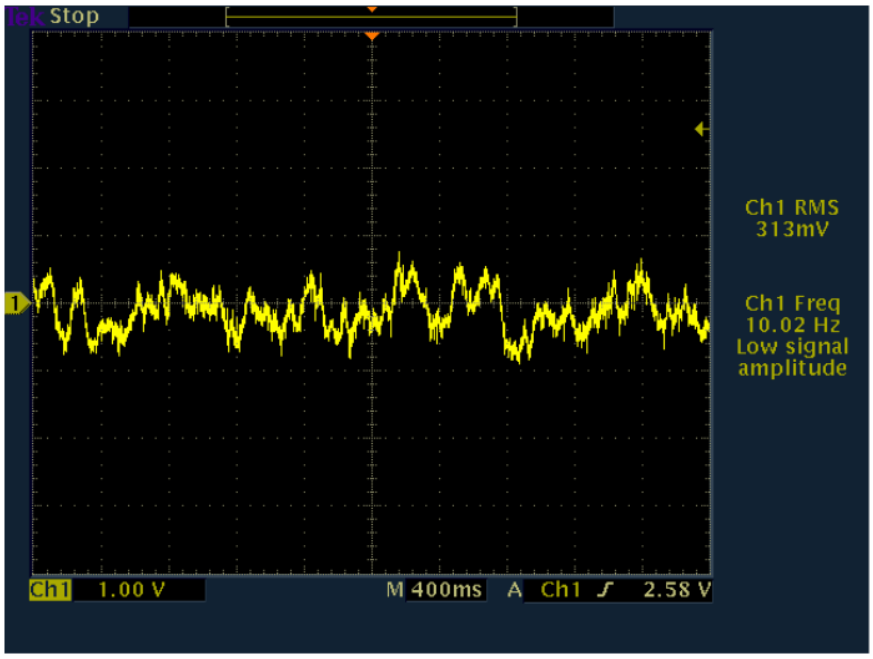

Figure 3.16 Output of amplifier circuit with no motion

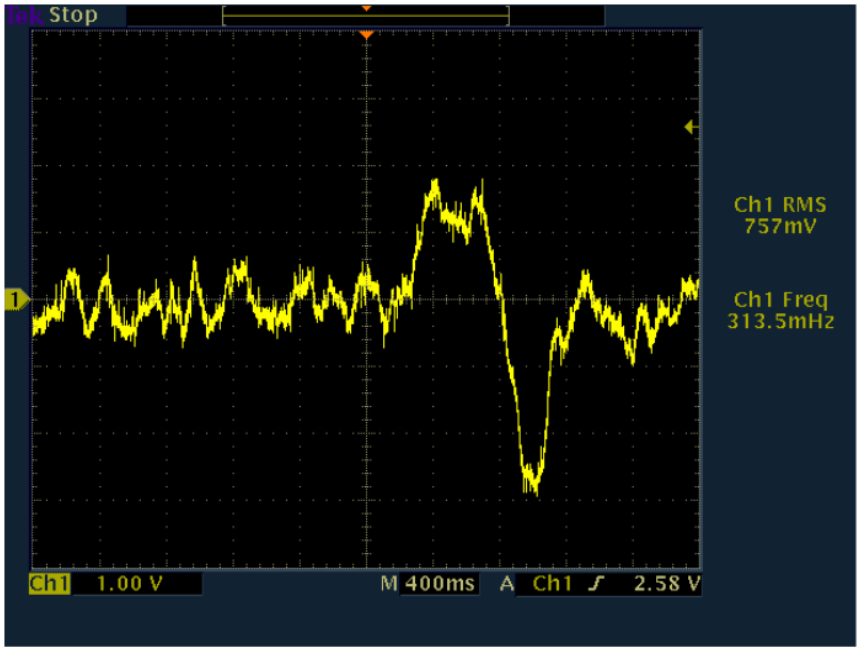

Figure 3.17 Output of amplifier circuit with single motion

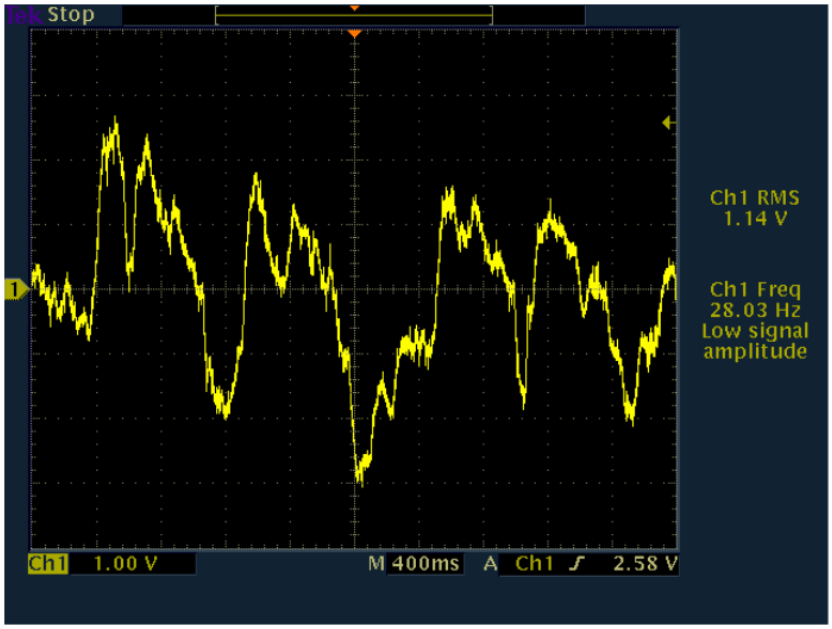

Figure 3.18 Output of amplifier circuit with continuous motion

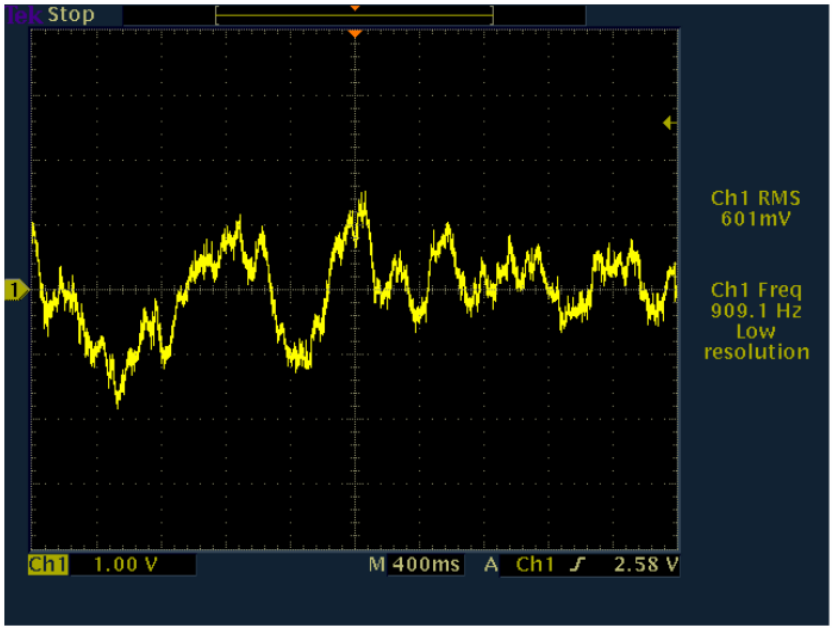

Figure 3.19 Output of amplifier circuit with slower motion

CHAPTER FOUR

IMPLEMENTATION OF FPGA IC TO RADAR DESIGN

In previous chapter the working principles of radar design is explained. The key point of design is to get proper delayed signal, because delayed signal gives us information about distance of object. In first design, explained in previous chapters, delayed signal is gotten by the help of a varicap diode in which capacitance value can be varied by the dc voltage applied to cathode of it. The delay time we can apply to a signal is limitted because the capacitance of diode can be varied just from 10pF to 80pF and this means we can get delay time between 1ns to 15ns. From equation 2.1, we need 6.8ns delay time to detect object just 1 meter far away. From this known, for 2 meter we need 13.6ns delay time. So, we can say that with varicap diode design we can detect objects at maximum 2.5 meters far away.

Because of this timing constraints we decided to control delay timing with software. To realize this purpose, microcontroller could be used but FPGA is more logical to use and to use an FPGA IC was first target of this project.

We used Xilinx Spartan-3E Sample Pack board for this project. This board has FPGA IC which belongs to Spartan-3E family. As we said above, the only feature that we used is to be able control delay time with software. In varicap diode solution we used output of Noise Modulated Pulse Generator circuit for both transmit and delay circuits. With FPGA IC solution we used two pulse signals, one for transmit circuit and other for delay circuit.

4.1 Xilinx Spartan-3E Sample Pack Board

We didn't choose the FPGA IC according to my needs, we selected to use a Sample Pack which was already exist in company I work. We used Xilinx SPARTAN-3E FPGA Sample Pack. A photograph of this Sample Pack can be seen in Figure 4.1.

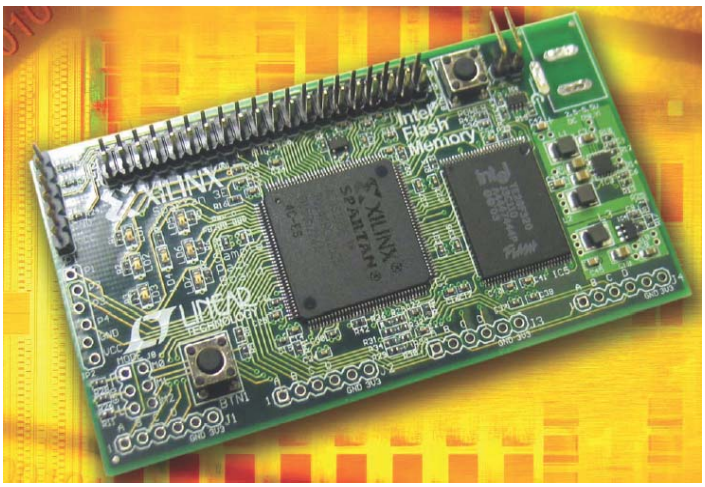

Figure 4.1 Xilinx Spartan-3E sample pack

This Sample Pack is a demonstration platform intended to become familiar with the new features and avalibility of the SPARTAN-3E FPGA familiy. Figure 4.2 shows the SPARTAN-3E Sample Pack board block diagram, which includes the following components and features:

- 100,000 gate Xilinx Spartan-3E XC3S100E FPGA in a 144-Thin Quad Flat Pack package
  - 2,160 logic cell equivalents
  - Four 18K-bit block RAMs (72Kbits)
  - Four 18x18 pipelined hardware multipliers
  - Two Digital Clock Managers (DCMs)
- 32Mbit Intel StrataFlash
- A 40-pin expansion connection port to gain access to the Spartan-3E FPGA
- Four 6-pin expansion connector ports to extend and enhance the Spartan-3E

- 7 Light Emitting Diodes (LEDs)
- 50Mhz Crystal Oscillator Clock Source
- Power Regulators

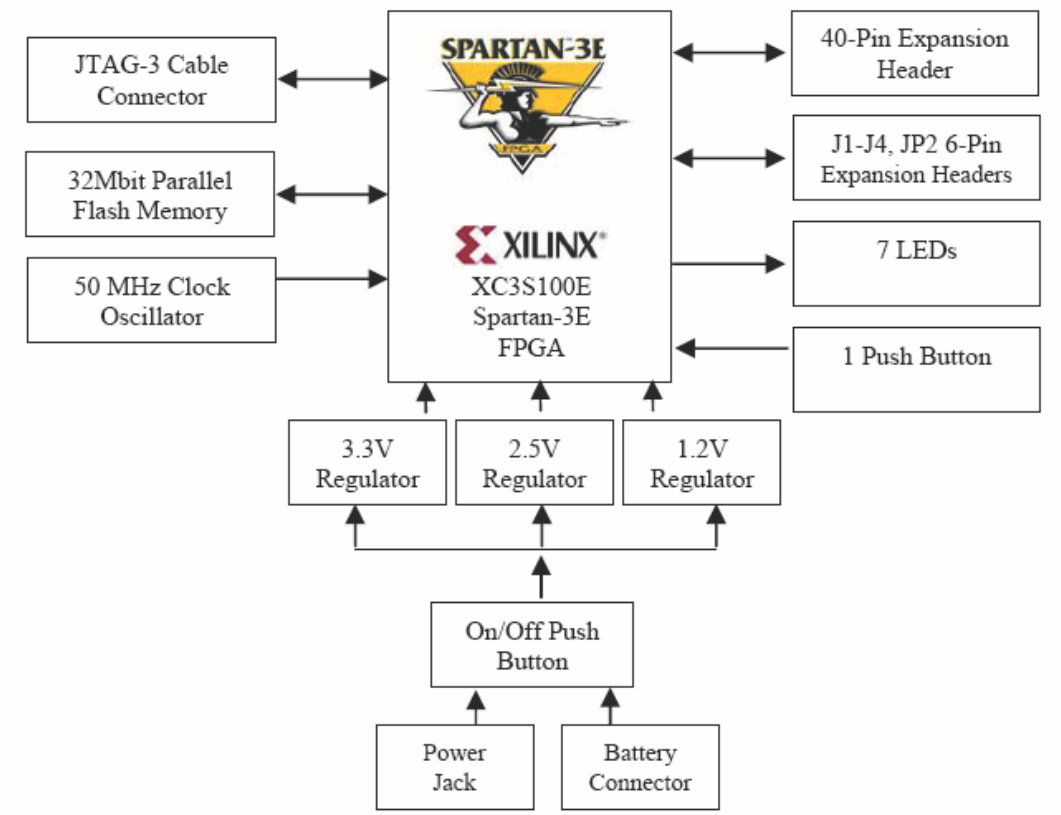

Figure 4.2 Xilinx Spartan-3E sample pack board block diagram

The Spartan-3E Sample Pack board has 32Mbit of parallel NOR flash used to configure the Spartan-3E FPGA in Byte-Peripheral Interface (BPI) mode. Additionally, the Intel StrataFlash can be used store execuatble software code, user data, multiple FPGA configurations and copy protection methods. The StrataFlash is setup for x8 read / write operation and optionally x16 read operations from the Intel StrataFlash.

4.2 Information About FPGA

Before the advent of programmable logic, custom logic circuits were built at the board level using standard components, or at the gate level in expensive application-specific (custom) integrated circuits. The FPGA is an integrated circuit that contains many (64 to over 10,000) identical logic cells that can be viewed as standard components. Each logic cell can independently take on any one of a limited set of personalities. The individual cells are interconnected by a matrix of wires and programmable switches. A user's design is implemented by specifying the simple logic function for each cell and selectively closing the switches in the interconnect matrix. The array of logic cells and interconnect form a fabric of basic building blocks for logic circuits. Complex designs are created by combining these basic blocks to create the desired circuit (Andraka Consulting Group, 2007).

The logic cell architecture varies between different device families. Generally speaking, each logic cell combines a few binary inputs (typically between 3 and 10) to one or two outputs according to a boolean logic function specified in the user program . In most families, the user also has the option of registering the combinatorial output of the cell, so that clocked logic can be easily implemented. The cell's combinatorial logic may be physically implemented as a small look-up table memory (LUT) or as a set of multiplexers and gates. LUT devices tend to be a bit more flexible and provide more inputs per cell than multiplexer cells at the expense of propagation delay (Andraka Consulting Group, 2007).

Field Programmable means that the FPGA's function is defined by a user's program rather than by the manufacturer of the device. A typical integrated circuit performs a particular function defined at the time of manufacture. In contrast, the FPGA's function is defined by a program written by someone other than the device manufacturer. Depending on the particular device, the program is either 'burned' in permanently or semi-permanently as part of a board assembly process, or is loaded from an external memory each time the device is powered up. This user programmability gives the user access to complex integrated designs without the

high engineering costs associated with application specific integrated circuits (Andraka Consulting Group, 2007).

Individually defining the many switch connections and cell logic functions would be a daunting task. Fortunately, this task is handled by special software. The software translates a user's schematic diagrams or textual hardware description language code then places and routes the translated design. Most of the software packages have hooks to allow the user to influence implementation, placement and routing to obtain better performance and utilization of the device. Libraries of more complex function macros (eg. adders) further simplify the design process by providing common circuits that are already optimized for speed or area (Andraka Consulting Group, 2007).

4.3 Modification of Design with Usage of FPGA IC

The FPGA IC is used to be able control delay time with software. With this control we don't need extra circuit for delay purpose. Because of that we deleted the circuit with varicap diode. With this configuration, narrow pulse generator (transmitter circuit) is same but narrow pulse generator with nanosecond delay circuit is changed.

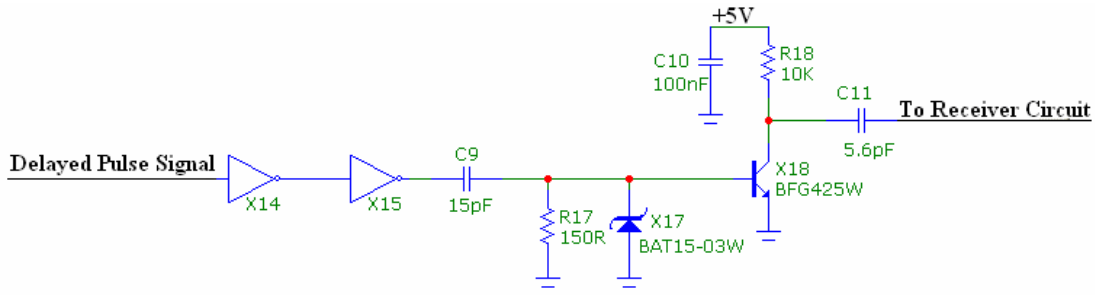

Figure 4.3 New delay line circuit

If we compare Figure 3.9 and Figure 4.3, we can see the difference easily. The circuit with varicap diode is deleted and the input to this circuit is already a delayed Pulse signal.

We used two GPIO of FPGA IC for transmit signal and delayed version of transmit signal. We renamed the delayed signal as “DELAY” and we renamed transmit signal as “TRANSMIT”.

The output signals of amplifier circuit are given in Figures 3.15 to 3.18 at no motion, single motion and continuous motion conditions. As can be seen from these figures, with motion output signal swings between -5V and +5V. These scope outputs says us a lot of things but for user these outputs are meaningless. Because, to detect whether there is a motion or not with scope outputs is an expensive way for such an applications. So, it is more useful to give a visual output to user.

Because of that we used a simple LED for this application. We know that if there is no motion, the output of amplifier circuit swings between -1V and +1V. If there is motion, output signal exceeds +1V and gets lower than -1V. We used a Limit Comparator to give a visual output with LED. This limit comparator circuit is shown in Figure 4.4.

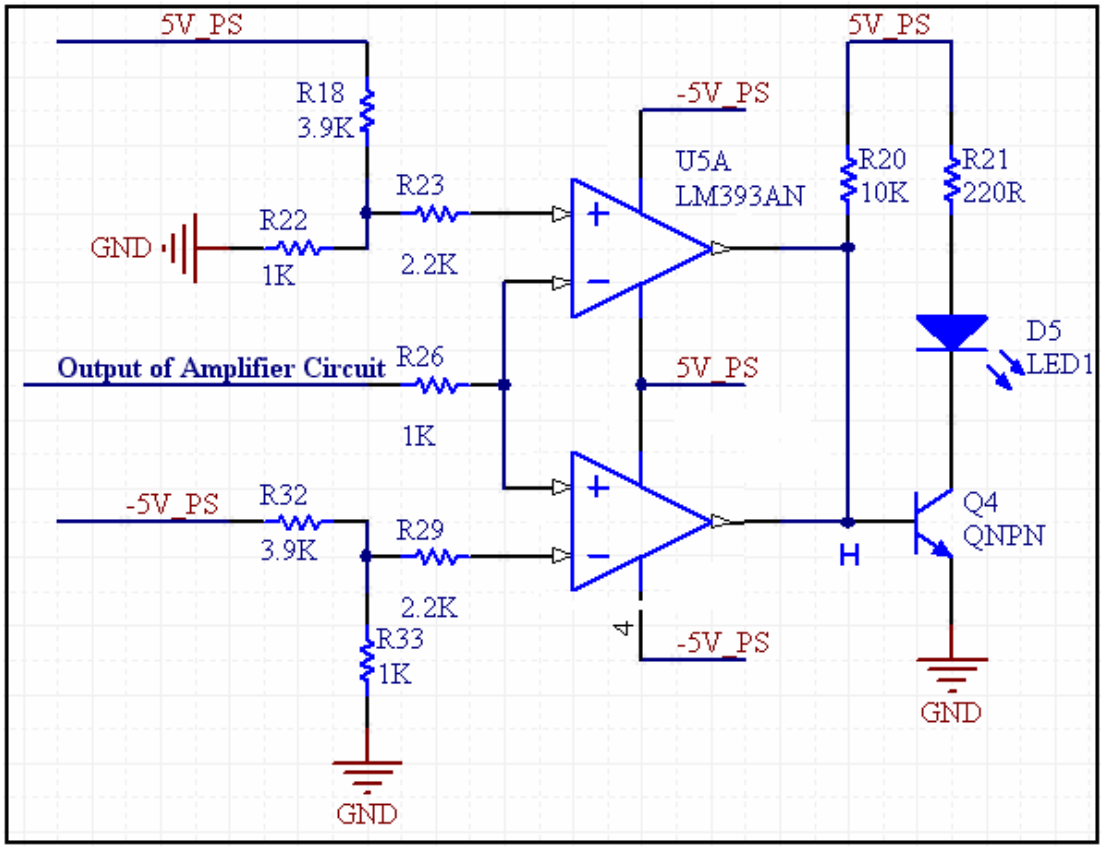

Figure 4.4 Limit comparator circuit

In limit comparator circuit LM393 dual operational amplifier comparator IC is used. To simulate this circuit we applied a sinusoidal signal which swing between -5V and +5V as an output of amplifier circuit. The output signal at point “H” and input signal are shown in Figure 4.5. From this simulation output it can be easily seen that if the input signal is between -1V and +1V the output signal at point “H” is HIGH for transistor Q4. If the input signal is out of range (-1V and +1V) then the output signal at point “H” is LOW for transistor Q4. This causes the LED to light on when the input signal is between -1V and +1V, and light off when the input signal is out of range (-1V and +1V). In other words the LED (D5) is light on when there is no motion at desired distance and it is light off when there is motion at desired distance.

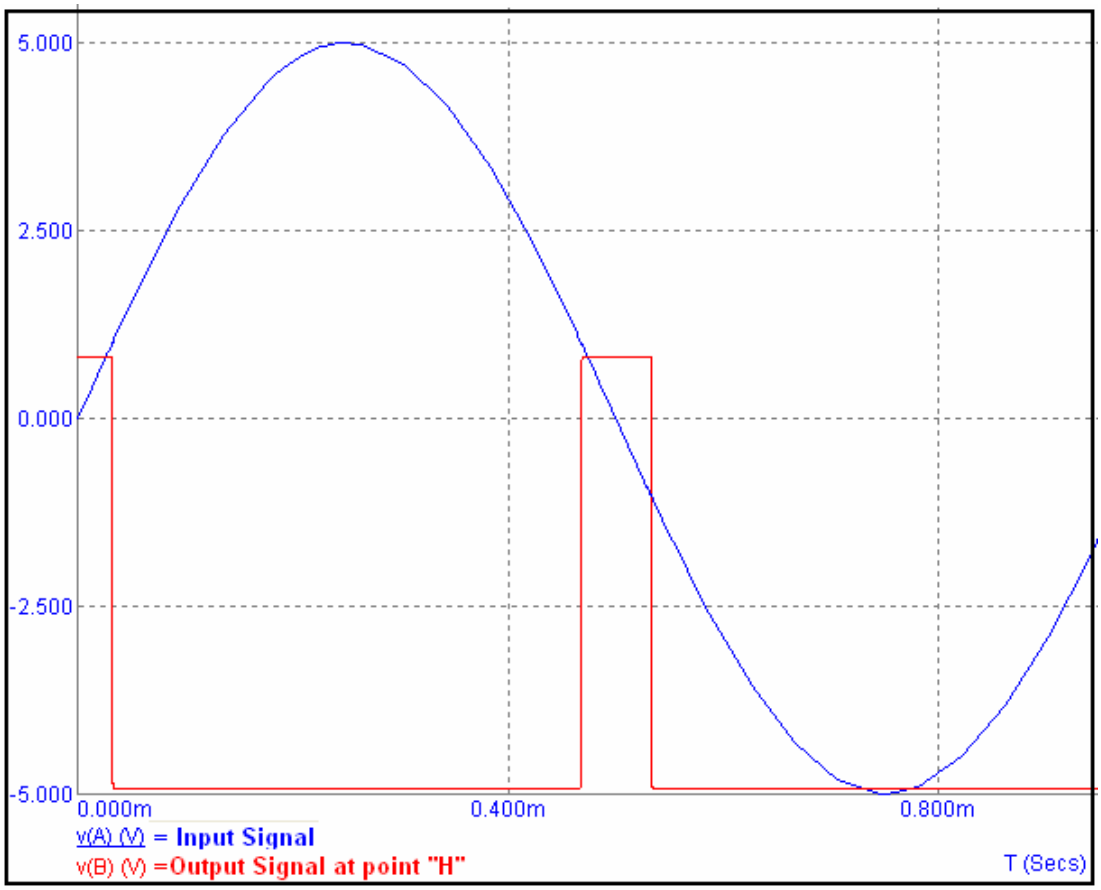

Figure 4.5 Simulation output of limit comparator circuit

4.4 Xilinx ISE 10.1 Program and Simulation Outputs

"TRANSMIT" signal is a pulse train which has 630ns period. "DELAY" signal is same with TRANSMIT, the only difference is DELAY signal is drived after user specified time from TRANSMIT signal.

Verilog hardware modeling language is used for FPGA IC programming. In Verilog to supply this delay time to a specific signal is very simple. The code for this purpose is;

```
assign #TIME DELAY=TRANSMIT;
```

In this code TIME is the delay time that we want to apply to signal. DELAY is the pulse train that will drive the circuit which creates enable signal for receiver circuit. TRANSMIT signal is the pulse train that will drive the circuit which creates the transmit signal.

The software was written in Xilinx ISE 10.1 program. The simulation results are sown in Figure 4.6.

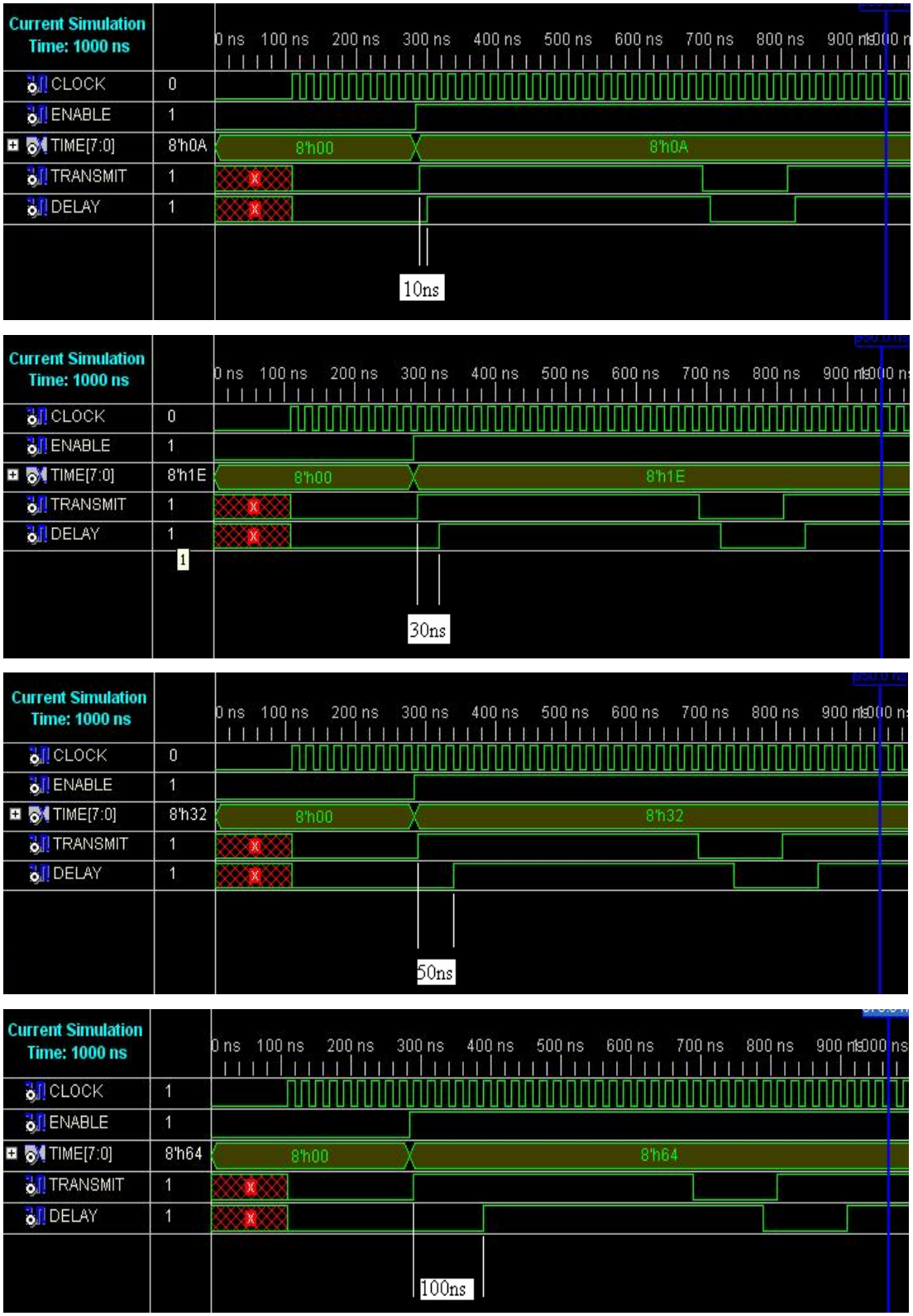

Figure 4.6 Simulation outputs of TRANSMIT and DELAY signals

In Figure 4.6 TIME signal determines the delay time that will be applied to DELAY signal. The value for TIME signal is hexadecimal format of delay time. TRANSMIT and DELAY signals are same, the only difference is delay between them.

TRANSMIT and DELAY signals are constructed by using Sample Pack board reference CLOCK source. The clock input to FPGA IC is 50MHz. This means its period is 20ns. By using a counter for all rising edges of clock signal, we got these two pulse train. TRANSMIT signal's period is 580ns. It is high during 400ns and low during 180ns. In program we count the rising edges, since the period of clock is 20ns there is 20ns between two rising edges and counter increases at every rising edges. If counter value is 20 (this means 20*20ns=400ns) the TRANSMIT signal toggles from HIGH to LOW. It continues to count and if it counts 9 (9*20ns=180ns) then it toggles LOW to HIGH again. At he end of count, counter value is again 0.

4.5 RTL Schematics of Verilog Module

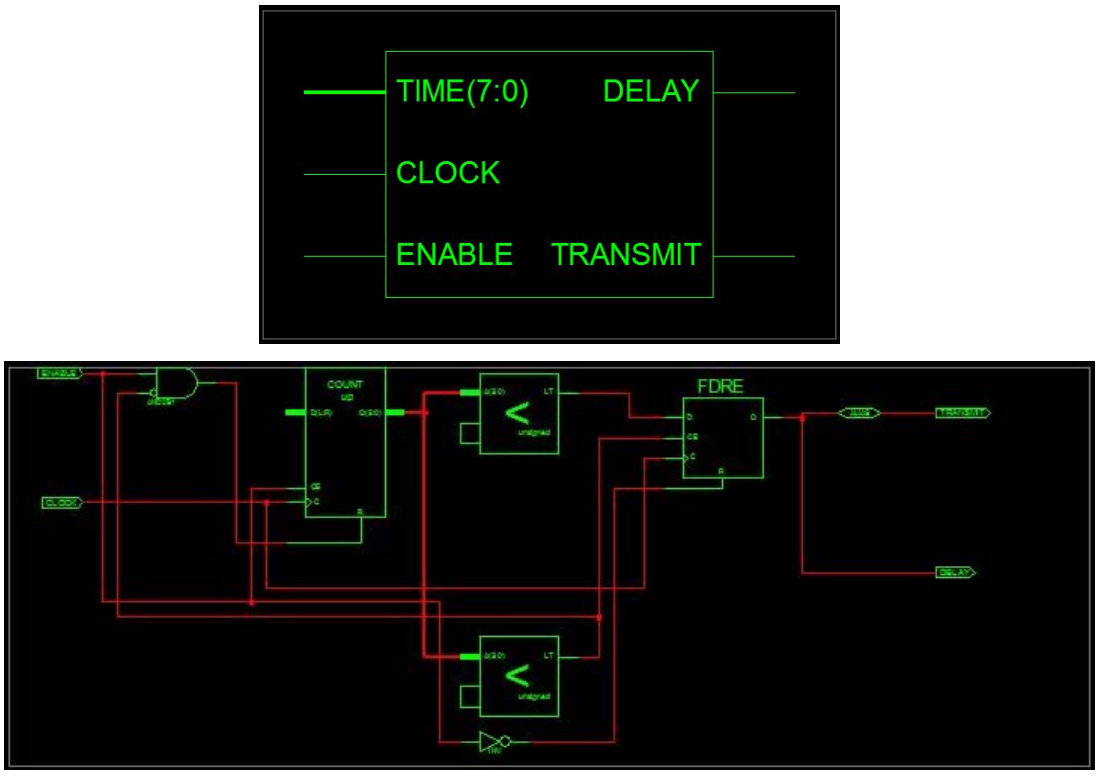

Figure 4.7 RTL schematics of verilog module

4.6 Flowchart of Verilog Software

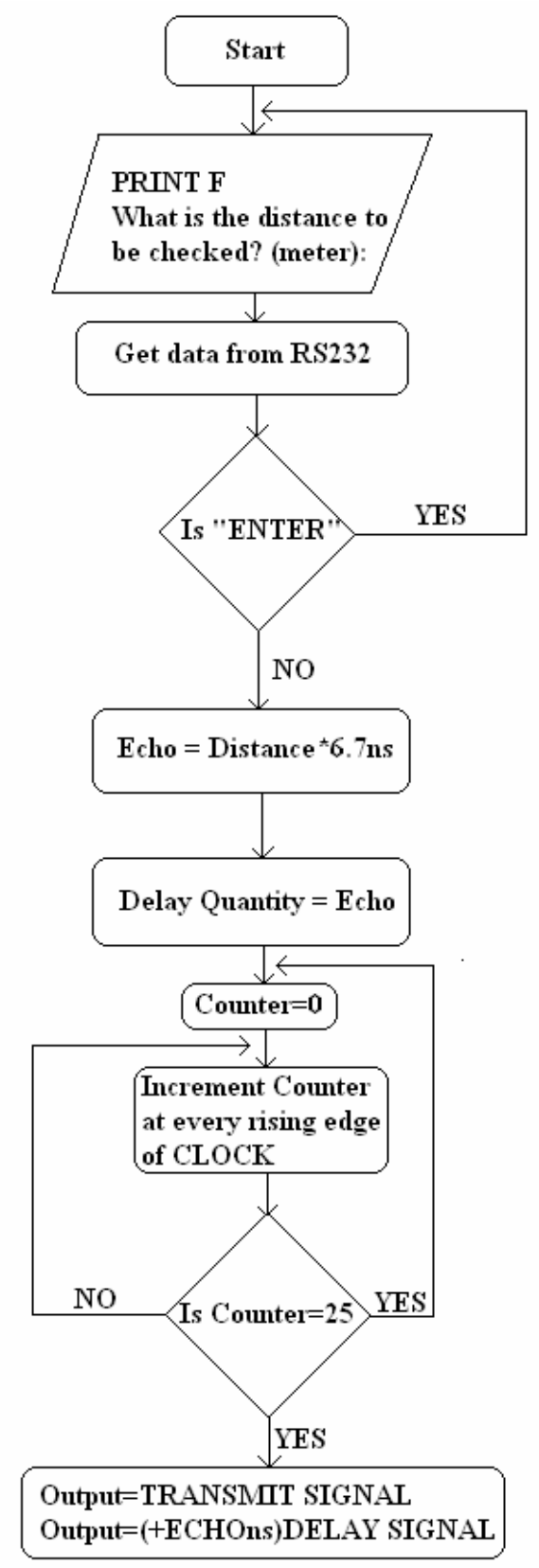

Figure 4.8 Flow chart of program

4.7 A Photograph of Hardware of Project

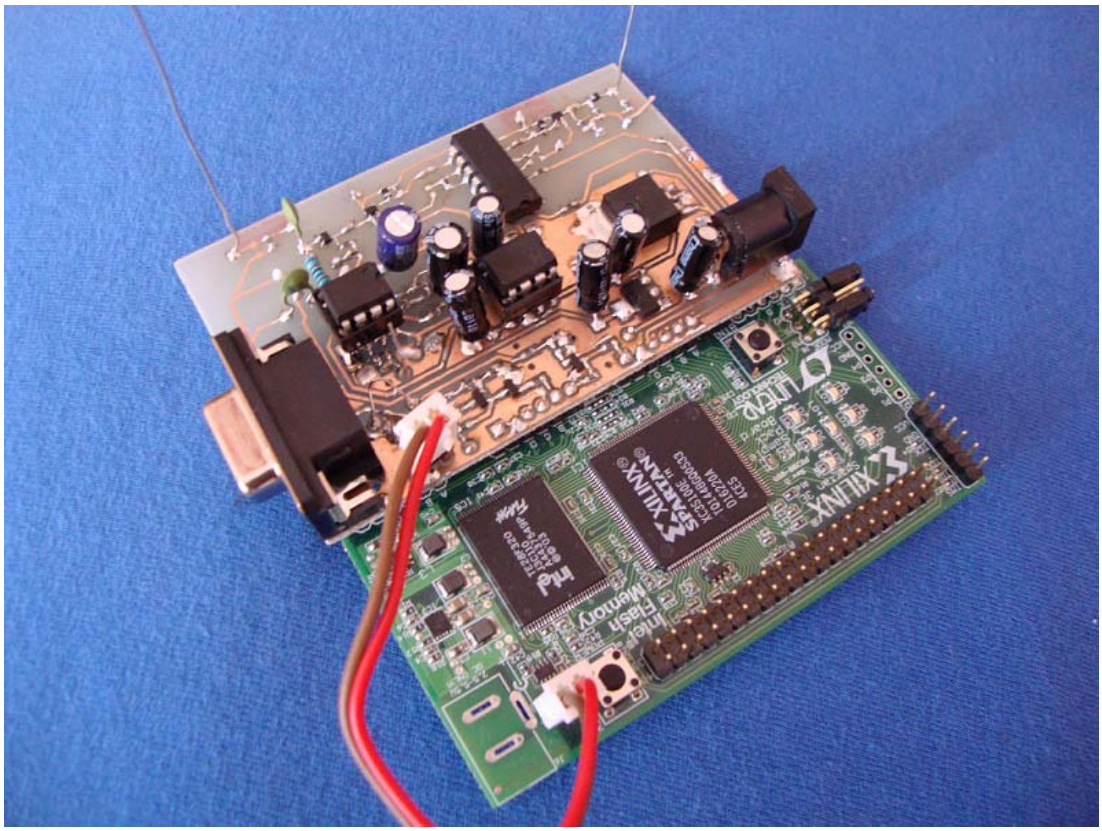

Figure 4.9 A photograph of hardware of project

The hardware of project is constructed by using two hardware. One of the hardware contains FPGA IC and its components. This PCB was ready and it is sent by Xilinx as an evaluation board. The other PCB is designed by us. This PCB contains the sections that are explained in Chapter 3. These two PCBs are connected according to needs of our design and one completed hardware is created.

CHAPTER FIVE

CONSTRAINTS AND VIABLE NEEDS

In this design, there are two important constraints; one, distance can be checked, two, speed of target can be checked. These contraints are related to the components used in design.

5.1 Speed of Target

The transmitted signal travels from the antenna and an attenuated echo returns to the receiver antenna system. If the target is not at the expected distance, the system ignores it. If the target is at the correct distance, the return signal is detected by the diode gate and averaged by the integrator.

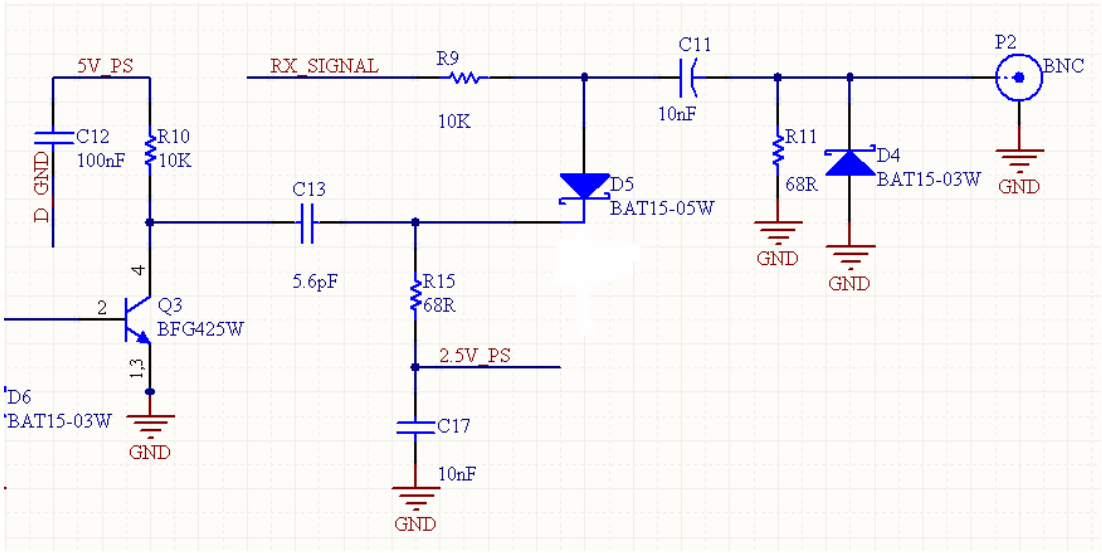

Figure 5.1 Receiver circuit

In Chapter 3, I also pointed out that the time constant of the averager can be calculated from the equation 5.1.

$$\tau = 2\pi RC = 2*\pi*10^{4}*10^{-8} = 628\ \mu s \qquad \text{(Eq. 5.1)}$$

628 μs time constant in the receiver limits the target detectable moving frequency to about 1200Hz, that is a maximum target speed is defined above which the UWB radar is no more able to detect it.

5.2 Distance of Target

As explained in previous chapters, the detectable distance depends on the maximum delay time we can apply to the enable signal of receiver circuit. Since the period of transmitted signal is 500ns and since this signal is high during 300ns of this period, the maximum delay we can apply to enable signal is 300ns. If we want to apply more delay, then, we can not detect anything. For a pulse signal to travel from transmitter antenna and come back to receiver antenna takes about 6.7ns. So, from this contraint the maximum ditance can be checked is 300ns / 6.7ns = 44 meter. But this is not only constraint that effects the maximum distance can be checked. The power of transmitted and received signals is also very important determinant for distance. Attenuation of pulse signal also depends on the environment that it travels in. Since we are working in laboratory, environment signal path is air. Main determinants are humidity and temperature of air. At my working environments, the maximum distance that can be detectable is approximately 9-10 meters.

5.3 Detecting Moving vs. Stationary Objects

The realized UWB radar in this thesis can detect just moving objects, it can not detect the stationary objects. The reason of this lack can be explianed by using Figure 3.13.

In Figure 3.13, the fast sampler is operated using schottky diode (X26) which is placed in the conduction mode by applying a short pulse at the cathode. In this way the 10nF on the antenna line charge with, and integrate the received echoes by using R23 and C15. Integrate means, R23 and C15 takes the average of received echoes. If there is a change at the value of this average, this means there is an object in movement at the desired distance.

Suppose that we adjust the delayed enable signal for detecting an object 2 meters far away. If this is a stationary object, the echoes coming back is accepted by receiver circuit. Becuase, the object is at 2 meters and the delay is adjusted according to 2 meter. But these coming and passed echo signals can not create a variation at averaged voltage level, because echo signals from a stationary objects come continuously and this creates a constant voltage input for amplifier section. For object detection the system need a varying average voltage for amplifier section, this variation is amplified and interpreted as a movement. Because, the variation on average voltage level can be supplied just from objects which are in movement.

5.4 The Reasons of Using an UWB Radar For Motion Detection

Motion detection realized in this thesis project can be aslo achieved by using other two radar types, pulse transmission and continuous wave radars.

At the first glance it seems that to use continues wave radar for this thesis is more suitable. Because the aim of the thesis is to detect motion. As we know Doppler Effect can be used for detection of movement is the best solution. But for the short range the continuous wave radars are not such much succesful. Doppler effect is based on the detection of frequency changes of returned echos. For short ranges this frequency variation is very little. So, very sensitive receiver circuit should be designed. Also, a continuous wave radar is bulky because it requires two antennas. Continuous wave radars also needs a carrier signal and adjustment of carrier frequency. While designing a continuous wave radars it is very imporant to take care of about empedance matching, very suitable antenna usage. All these lacks are reasons why a continuous wave radar is not used in this thesis.

A pulsed radar system sends out a pulse containing a signal of a known frequency. The time that it takes for the echo to return is used to compute the distance from the radar site to the target. Pulsed radar systems can be constructed with a single antenna where the antenna switched between transmit and receive signal paths. For better resolution on range measurements the pulse signals are sometimes frequency or

amplitude modulated. Common parameters for the pulsed radar systems include: pulse width, pulse shape, pulse repetition frequency, average power, and carrier frquency. Wider pulse widths give a longer range. However, if the pulse width is too large, closer targets will reflect the leading edge before the system has finished limiting the minimum detection range. In a similar manner, the pulse shape can affect the accuracy, resolution, and range extends. If the rising edge of the pulse is skewed, the timing accuracy of the return pulse will be changed. A change in the trailing edge would harm the resolution by widening the pulse. Distortion of the leading and trailing edges also makes the pulse wider, worsening the minimum range. High pulse repetition frequencies allow the system to detect targets at shorter ranges since the system is less likely to be in transmit mode when the pulse returns from its shorter trip. Thse same higher rates also increase the detection probability by allowing the system to do more averaging. As we can see from these limitiations, there are lots of parameters should be adjusted for correct detection. These limitations causes a bulky design.

Both continuous wave and pulsed systems benefit by adding more power to get better range. Since continuous wave systems have a lower peak power for a given average, they gain an advantage. Both systems also have to make tradeoffs such as carrier frequencies. A higher frequency allows smaller equipment, but lower frequencies better penetrate the atmosphere.

UWB radar systems are similar to pulsed systems. Unlike pulsed systems that concentrate their energy at a small range of frequencies. UWB radars try their best to spread this energy to an extremely wide band of frequencies. For short range movements UWB radars are best to use. The system is not bulky as much as other two radar types. There is no carrier signal, no need for empedance matching and no need to use special antennas for short ranges. The only thing is to send narrow pulse train and to detect whether there is echo from desired distance.

5.5 Alternative Methods for Getting Narrower Transmitter Signal

Most conventional radar systems operate in a relative narrow frequency band; they use harmonic (sinusoidal) signals as carrier oscillations to transmit the information. The reason for that is rather simple: a sinusoidal is an eigenoscillation of LC-contour, which is the simplest and, so, the most widely used electrical oscillation system. The resonance features of such a system make possible frequency selection of the large number of information channels operating in the common environment (space, guiding and optical communication lines). So, the frequency selection is now the main method to divide these channels, most radars now in use are narrow band systems with frequency band much less than the carrier frequency. The theory and practice of current radar systems are based of this specific feature.

But as known, it is a frequency band that determines the information content of radar systems, as the volume of information transmitted per a time unit is directly proportional to a frequency band. To raise the information capability of a radar system, the widening of its frequency band is needed. The only alternative approach is an increase in information transmission time.

In connection with fast informatization of society and continuous increase of information streams, this problem becomes more and more actual both for radio communication and radars. Actuality of this problem determined rapid development in the last years the technologies using ultra wide band (UWB) signals (UWB Russian Group, 2009).

In my design, to get UWB pulse train I used the circuit shown in Figure 3.3. The part of circuit that the narrow pulse signal is created is shown in Figure 5.2.

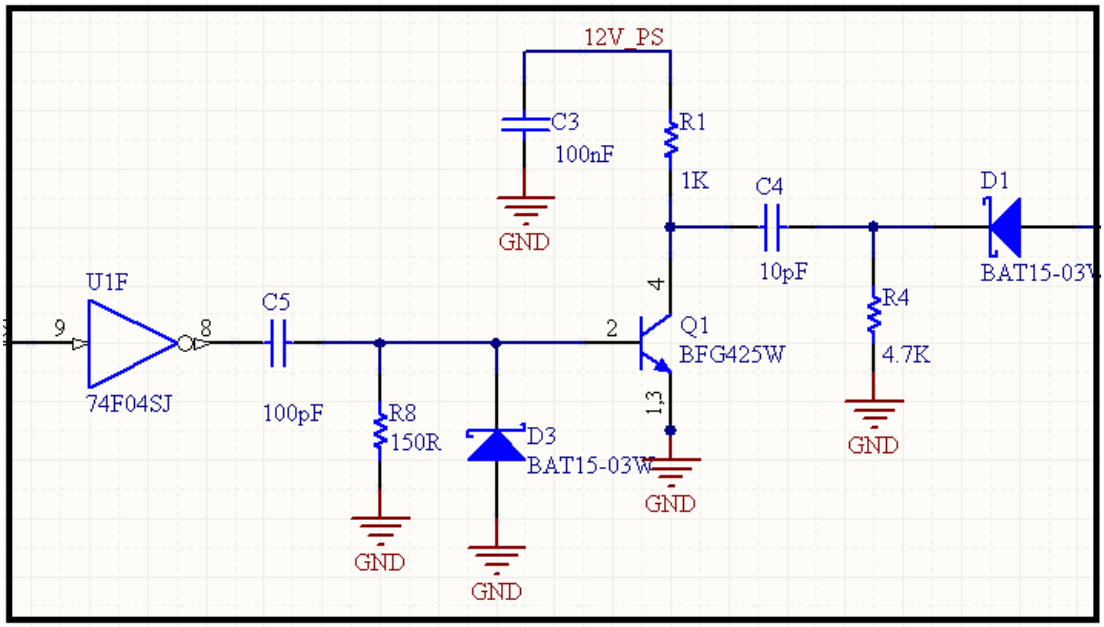

Figure 5.2 Narrow pulse generator part of transmitter circuit

The capacitor C4 is on the collector of the RF transistor. When the transistor is not conducting, this capacitor charges up to the supply at a rate limited by a R1 and R4 resistors. The pulse is generated when the transistor goes into conduction and shorts the capacitor to gorund. It discharges quickly and generates a pulse. Discharging time of capacitor C4 depends on its capacitance value and resistance value from collector to emitter of Q1. Time constant for C4 equals to $\tau = C*R_{CE}$. In this design with the component values in Figure 5.2, the pulse width is approximately 3.4ns. This is the narrower pulse that we can get with this design.

5.5.1 Using Step Recovery Diode For UWB Applications

Pulse generator is an essential component for UWB radar systems. In general, the pulse produced by the pulse generator has the features of monocycle, short width and high amplitude. The spectrum of this kind of pulse is much abundant. So the pulse has the performance of strong penetrability and anti-jamming, which is suitable for short-range communication, through-wall radar, exploring land radar, etc. SRD (Step Recovery Diode) is widely used in pulse generator. SRD is a kind of strongly nonlinear device. The operation process of pulse production is very complicated.

SRD is a p – i – n diode with thin i layer, which is an energy storage element. A large amount of charged is stored in i layer during forward conduction period while a dynamic equilibrium is maintained between injection and recombination of carriers. When SRD is stimulated from forward pulse to backward pulse, the forward current of SRD will not turn off immediately, but will turn off when carriers in i layer are exhausted. SRD can be modeled as the parallel connection of a dynamic capacitor and a pn diode. The equivalent circuit of SRD including all factors is shown in Figure 5.3. C_p, L_s, R_s, $C_j(V)$ and D_1 represent package capacitance, lead inductance, series resistance, dynamic capacitance and pn diode respectively.

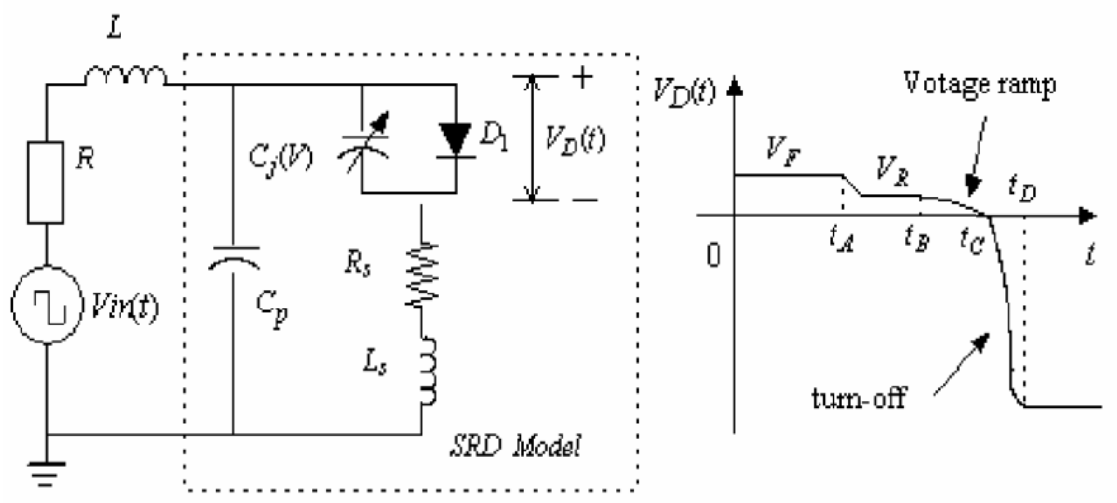

Figure 5.3 SRD model scheme and the operation process

The operation process of SRD from forward conduction to backward turn-off can be divided into five stages, shown in Figure 5.3.

First Stage; In the first stage (before t_A), the forward current SRD is maintained constantly and the dynamic equilibrium is formed between injection and recombination of carriers. The voltage through SRD is V_F. The charge stored in i layer is represented as $Q_A = I_{F\tau}$. In this stage SRD can be modeled as the parallel connection of a large capacitor and a pn diode.

Second Stage; In the second stage (between t_A and t_B), Vin(t) steps from V^+ to V^- and the current is opposite. But SRD is still in conduction state because there is no space charge region in i layer. The charge in i layer is drawn out gradually and becomes less and less. In this process the voltage through SRD is slightly changed

and the dynamic capacitance gets smaller and smaller according to he relationship $Q=C_j(V_R)V_R$. Thus, in this stage SRD can be modeled as the parallel connection of a pn diode and a capacitor with the capacitance getting smaller and smaller.

Third Stage; in the third stage (between t_B and t_C), the space charge region appears at t_B. The space charge region becomes wider and wider with the charge in i layer being drawn out gradually. At t_C, the charge in i layer is exhausted and SRD gets into the turn-off period. The nonlinear transition is mainly completed in this stage in which the dynamic capacitor transits from large capacitance to small capacitance, and the transition process is very complicated. Thus, in this stage SRD can be modeled as the parallel connection of a pn diode and a capacitor with the capacitance getting smaller and smaller. The width of space charge region is given by

$$W = 2d - \left(\frac{8DQ}{I_R}\right)^{1/2} \tag{5.2}$$

Here, 2d, D, Q and I_R are the width of i layer, the ambipolar diffusion constant $D=20cm^2/V.s$, charge in i layer and current respectively. The voltage through SRD is then

$$V = \frac{W^2 I_R}{4\varepsilon v A} = \frac{I_R}{\varepsilon v A}\left(d^2 - 2d\left(\frac{2DQ}{I_R}\right)^{1/2} + \frac{2DQ}{I_R}\right) \tag{5.3}$$

Here, ν and ε are the velocity of electron and hole, working area of SRD and dielectric constant of i layer respectively. The ratio that the third item is divided by the second item in second formula is $m = (2DQ)^{1/2} / (2d(I_R)^{1/2})$. In this the charge in i layer is little. If suppose $Q = 10^{-13}C$, I_R = 100mA, d = 1 um, it can get that m = 0.03. So the third item is much smaller than the second item. The third item can be ignored compared with the second item. After simplified the charge in i layer is

$$Q(V) = \frac{I_R}{8Dd^2}\left(d^4 - \frac{2\varepsilon v A d^2}{I_R}V + \left(\frac{\varepsilon v A}{I_R}\right)^2 V^2\right) \quad (\phi > V > 0) \tag{5.4}$$

By one order differential on above formula, the dynamic capacitance can be obtained

$$C_j(V) = \frac{dQ}{dV_{SCL}} = \frac{\varepsilon v A}{4Dd^2}\left(\left(\frac{\varepsilon v A}{I_R}V - d^2\right)\right) \quad (\phi > V > 0) \tag{5.5}$$

This formula indicates that the relationship between the dynamic capacitance and the voltage through SRD is linear.

Fourth Stage; In the fourth stage (between t_C and t_D), the SRD turn off and the charge is exhausted. SRD is charged by source. The opposite voltage through SRD is larger and larger and the dynamic capacitance is smaller and smaller. The i layer has little effect on SRD performance so that the function of SRD is similar as a pn varactor diode. The dynamic capacitance is

$$C_j(V) = C_{j0}/\sqrt{1 - V/\phi}. \tag{5.6}$$

Here, Ø = 0.7V. C_{j0} is the dynamic capacitance at V = 0.

Fifth Stage; In the fifth stage (before t_D), SRD turns off
(IEICE Electronics Express, 2006).

SRD diodes are designed to have a very abrupt switching time from their forward bias state to their reverse bias state, making them very popular devices for pulse generators.

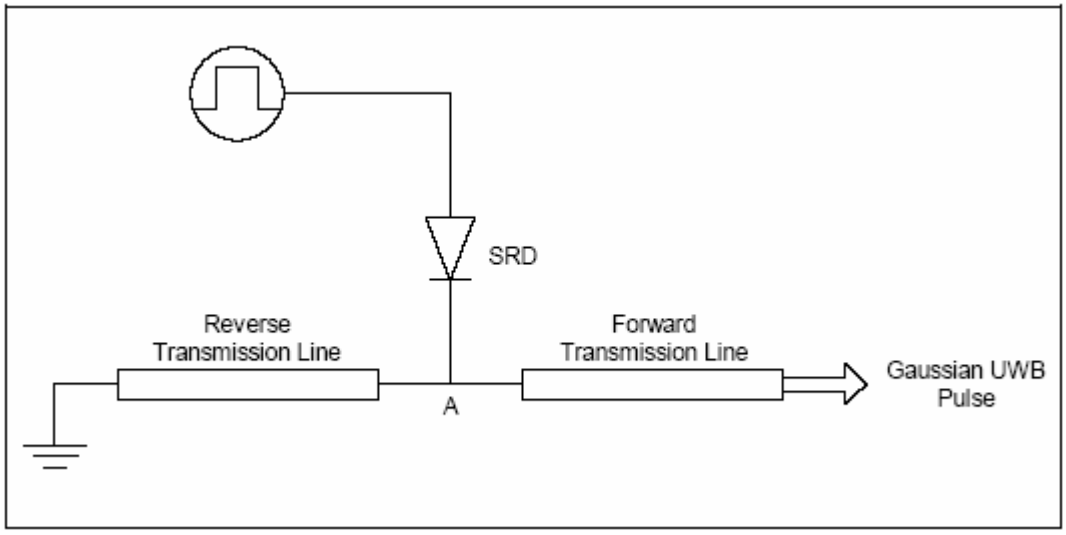

Figure 5.4 SRD pulse generator example

One common SRD Gaussian pulse generator configuration is shown in Figure 5.4. the ramp-like pulse produced by the SRD splits at point A, traveling down the reverse transmission line and also propagating down the forward transmission line.

The ramp-like pulse moving down the reverse transmission line reflects from the stub and is converted into an opposite polarity ramp-like time delayed pulse due to the negative reflection coefficient of the short circuit. At the forward transmission line, the two pulses recombine to form a Gaussian pulse shape. Using the same configuration shown in Figure 5.4, the SRD can be replaced by a tunnel diode and produce the same pulse shape (Orndorff A.M., 2004).

The width of the pulse is determined by the length of the short circuited transmission line and is analytically computed using: (Orndorff A.M., 2004).

$$\tau = \frac{2L_{TL}}{v_p} \tag{5.7}$$

where:

L_{TL} is length of the reverse transmission line (meters)

Vp is the phase velocity along the reverse transmission line (meters/second)

The phase velocity along a microstrip transmission line (used since implementation will be done on a printed circuit board) is found using:

$$v_p = \frac{c}{\sqrt{\varepsilon_e}} \tag{5.8}$$

where:

c is the speed of light (meters/second)

ε_e is the effective permittivity constant of the microstrip

The effective permittivity constant is the equivalent homogeneous medium replacing the air and microstrip substrate. This variable is calculated using: [12]

$$\varepsilon_e = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\left(\frac{1}{\sqrt{1 + 12d/w}}\right) \tag{5.9}$$

where:

ε_r is the relative permittivity constant of the microstrip substrate

d is the thickness of the microstrip substrate

w is the width of the microstrip transmission line (meters)

To give an example using the formulas above, typical FR4 PCB material has a relative permittivity constant of 4.6, uses 7.2 mil substrate thickness, and utilizes 12 mil trace widths for RF transmission lines. The effective permittivity and phase velocity can then be calculated using Equations (5.7) and (5.8), respectively. For a transmission line length of 1 inch, after converting to metric, the resulting pulse width is 315 picoseconds (Orndorff A.M., 2004).

CHAPTER SIX

CONCLUSION

In this thesis, an ultra wide band radar with FPGA control is designed. At the begining of the thesis a transmit signal was created, it was very important to get a narrower pulse signal. So, after some observation and experiments I decided to use an RF transistor to charge and discharge a capacitor. Discharging of this capacitor created the desired pulse signal. The created pulse width was not suitable for radar applications but it was suitable to meet with ultra wide band radar techniques.

After transmit signal is created receiver circuit is designed. For receiver circuit, it was again important to design a simple but efficient circuit. So, a simple sample-gate circuit is designed. The aim of thesis was not only to detect a movement, also to detect the distance of movement was very important. Becuase of that, receiver circuit should not pass all the returned echo signals, it should pass echos only coming from distance determined before. So, an enable signal for receiver circuit is created. This enable signal is approximately same with transmit signal, so, same circuit is used for also enable signal. Since it takes some time for transmit signal to go to target ans come back to receiver circuit, receiver circuit should be enabled after transmit signal is sent. To achieve this delay, a simple varicap diode is used. The capacitance of this varicap diode changes with dc voltage applied to its cathode pin. I applied a PWM signal to control this dc voltage with software. With a serial resistance and a varying capacitance of varicap diode, RC circuit, desired delayed signal is created. For these controls I used a PIC microcontroller.

The source signal for transmit and enable signal circuits a simple oscillator circuit was designed. After some experiments, I saw that with delay quntity gotten with varicap diode is not enough, I could only detect maximum 2 meters. So, I decided to use an FPGA IC for both source signal of transmitter and enable circuits and for delay applied to enable signal. With FPGA IC I don’t need to use an external varicap

diode like component. I could apply a pulse signal to its one GPIO and I could apply desired time delay to this signal and to output delayed signal from another GPIO pin.

The voltage variations on receiver circuit in movement condition at the desired distance are in micro-mili volt ranges. So, these variations are amplified and low-pass filtered. At he output of this amplifier circuit, a signal which swings between -5V and +5V is gotten with movement of target.

Since this output voltage is not meaningful for user, we added limit comparator circuit to design. Limit comparator circuit makes a LED to light on or off according to whether there is a movement or not. With LED configuration we supplied a visual result for user.

With this project we proved that a radar system can be designed without using an RF signal which hasn’t got a carrier signal. We learned key points of ultra wide band design, for example the width of tranmitted signal should be as possible as narrow to be able to use broden frequency spectrum. Broden frequency spectrum means carrying more information. Ultra wide band designs are not used just only for radar applications, they can also be used in communication area.

REFERENCES

Andraka Consulting Group, Inc. (March 16, 2007). *FPGA Basics,* Retrieved August 21, 2009, from http://www.andraka.com/whatisan.htm

Barrett, Terence W. (2000). *History of UltraWideBand (UWB) Radar & Communications: Pioneers and Innovators.* Retrieved January 28, 2009, from http://www.ntia.doc.gov/osmhome/uwbtestplan/barret_history_(piersw-figs).pdf

Argos Press Pty Ltd. (2004). *Information on Continuous Wave Radar (CW Radar),* Retrieved June 14,2009, from http://www.argospress.com/Resources/radar/continwavradar.htm

Infenion Technologies. (July 12, 2001). *BAT15-03W,* Retrieved July 5, 2009, from http://datasheet.digchip.com/216/216-12702-0-BAT15-03W.pdf

Infenion Technologies. (Jan 10, 2003). *BBY56-02W,* Retrieved August 21, 2009 from http://datasheet.digchip.com/216/216-12780-0-BBY56-02.pdf

IEICE Electronics Express. (December 25, 2006). *A new CAD model of step recovery diode and generation of UWB signals,* Retrieved August 21, 2009, from http://www.jstage.jst.go.jp/article/elex/3/24/534/_pdf

Manandhar D., Shibasaki R., (July 17, 2003). *Ultra Wide Band (UWB) – introduction and signal modeling,* Retrieved June 14, 2009, from http://shiba.iis.utokyo.ac.jp/member/dinesh/research/Paper/ACRS2003/UWBdo.pdf

Argos Press Pty Ltd. (2004). *Information on Pulse Radar,* Retrieved June 14, 2009 from http://www.argospress.com/Resources/radar/pulradar.htm

Orndorff A. M. (May 20, 2004). *Tranciever Design for Ultra-Wide Band Communications,* Retrieved August 20, 2009 from http://scholor.lib.vt.edu/theses/available/etd-05242004-141034/unrestricted/Thesis.pdf

Philips Semiconductors. (March 11, 1998). *BFG425G,* Retrieved July 5, 2009 from http://datasheet.digchip.com/364/364-23609-0-BFG425W.pdf

Texas Instruments. (1996). *TL071, TL071A, TL071B, TL072, TL072A, TL072B, TL074, TL074A, TL074B, LOW-NOISE JFET-INPUT OPERATIONAL AMPLIFIERS,* Retrieved July 5, 2009, from http://datasheet.digchip.com/477/477-26126-0-TL071.pdf

UWB Russion Group. (2009). *About Technology – What is UWB,* Retrieved August 21, 2009 from http://www.uwbgroup.ru/eng/uwb/whatis/html