DOKUZ EYLUL UNIVERSITY
GRADUATE SCHOOL OF NATURAL AND APPLIED SCIENCES

DESIGNING LOCAL DIMMING ALGORITHM FOR HIGH CONTRAST RATIO AND LOW POWER CONSUMPTION FOR LED BACKLIGHT LCD TV SETS

by
Yusuf ÖZTÜRK

October, 2009
İZMİR

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A Thesis submitted to the,
Graduate School of Natural and Applied Sciences of Dokuz Eylul University In Partial Fulfilment of the Requirements for the Degree Master of Science in Electric and Electronic Engineering, Electric and Electronic Engineering Program.

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M.Sc THESIS EXAMINATION RESULT FORM

We have read the thesis entitled **"DESIGNING LOCAL DIMMING ALGORITHM FOR HIGH CONTRAST RATIO AND LOW POWER CONSUMPTION FOR LED BACKLIGHT LCD TV SETS"** completed by **YUSUF ÖZTÜRK** under supervision of **ASST. PROF. DR. ÖZGE ŞAHİN** and we certify that in our opinion it is fully adequate, in scope and in quality, as a thesis for the degree of Master of Science.

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ABSTRACT

Backlight level of LCD TV with LED backlight unit can be dimmed locally depending on the input video. This feature saves power and increases contrast ratio. Dimming is applied by three ways; zero-dimensional dimming, one-dimensional dimming and two-dimensional dimming. Most popular and effective dimming type is two-dimensional dimming. There are many algorithms to achieve two-dimensional dimming and this thesis brings a novel approach to this issue. The algorithm developed at this study is realized on FPGA chipset and is applied successfully. Algorithm is implemented on 42" full high definition with LED backlight panels and TV sets which have full high definition output. Application uses low voltage differential signalling of TV mainboards and never manipulates image data.

To see the results of the algorithm, three different measurements are taken from the system. Power consumption and contrast ratio are measured for five different images on cold cathode fluorescent lamp backlight, LED backlight and LED backlight with local dimming panels. Measured values have revealed that the algorithm is applied successfully. In terms of contrast ratio, improvement is very high on black-weighted images than white-weighted images. Measurements have emerged that power consumption depends on the white level of the image. It is approved that LED backlight panels, with local dimming or not, are better than cold cathode fluorescent lamp backlight panels in terms of both power consumption and contrast ratio.

Keywords: Local dimming, LED backlight panel, Dimming algorithm, Contrast ratio, Power consumption.

LED ARKA IŞIKLI TELEVİZYON ÜNİTELERİ İÇİN GÜÇ TÜKETİMİNİ AZALTICI VE KOTRAST ORANINI ARTRICI YEREL KISMA ALGORİTMASI GELİŞTİRİLMESİ

ÖZ

Sıvı Kristal Ekran Televizyonun arka ışık seviyesini yerel olarak giriş video sinyaline göre kısma işlemi yapılabilir. Bu, güç tüketimini azalmak ve kontrast oranını arttırmaktadır. Boyutsuz, bir boyutlu ve iki boyutlu olmak üzere üç farklı tür kısma işlemi alternatifi mevcuttur. LED arka ışıklı paneller için en çok tercih edileni iki boyutlu kısma işlemidir. İki boyutlu kısma işlemi için çeşitli algoritmalar geliştirilmiştir. Bu tezde de iki boyutlu yerel kısma işlemi için algoritma tasarlanmıştır. Tasarlanan algoritma alan programlamalı kapı dizisi üzerinde gerçekleştirilmiş ve başarıyla uygulanmıştır. Algoritma, tam yüksek çözünürlüklü LED arka ışıklı 42 inç panel kullanılarak gerçeklenmiş ve tam yüksek çözünürlüklü tüm platformlarda çalışabilecek şekilde tasarlanmıştır. Uygulama, anakartların düşük gerilim fark sinyalleri kullanılarak, orijinal sinyaller değiştirilmeden gerçeklenmiştir.

Algoritmanın sonuçlarını görmek için 3 farklı sistem için ölçüm alınmıştır. Soğuk katot floresan lamba arka aydınlatmalı, LED arka aydınlatmalı ve yerel ayarlanabilen LED arka aydınlamalı panellerde 5 farklı resim için güç tüketimi ve kontrast oranları ölçülmüştür. Ölçüm değerleri algoritmanın başarılı bir şekilde uygulandığını ortaya koymuştur. Kontrast oranı olarak siyah ağırlıklı resimlerde kontrast oranı çok yüksek çıkarken beyaz ağırlıklı resimlerde kontrast oranı bakımından iyileşme çok yüksek olmamıştır. Güç tüketiminin ise beyaz seviyesine göre değiştiği ölçüm sonuçlarından ortaya çıkmıştır. LED arka aydınlatmalı panellerin yerel kısma olmaksızın soğuk katot floresant lamba arka aydınlatmalı panellere göre hem kontrast oranı hem de güç tüketimi açısından avantajlı olduğu gösterilmiştir.

Anahtar Sözcükler: Yerel Ayarlama, LED Arka Işıklı panel, Kısma algoritması, Kontrast oranı, güç tüketimi.

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CHAPTER ONE

INTRODUCTION

Today, LCDs are the most common display technology for small (mobile), medium (monitor), and large (TV) display sizes. The image quality equals or exceeds that of a conventional CRT on many front-of-screen parameters, such as color, brightness, and resolution. In terms of contrast and viewing angle, however, an LCD's performance is rather poor. This is caused by the leakage of light from the backlight through the panel when it is in the black state. (Langendijk et al., 2008)

For a dark image, the contrast can be improved significantly by dimming the backlight and simultaneously increasing the drive values to the panel accordingly. (Langendijk et al., 2008)

The process of changing backlight globally, this is called 0D dimming. In this way, backlight should always provide adequate light to depict a scene, because of that, increasing contrast ratio by this method is not effective.

Increasing CR can be accomplished by changing backlights according to the video content. De Greef et al., (2006) presented a lamp-based approach in which each HCFL lamp could be driven independently. This method gives chance to modulate backlight vertically, called 1D dimming.

After developments of LED backlight LCD panels, two dimensional dimming as known 2D dimming come up. Backlight parts of this kind of panels have matrix structure and are addressable individually.

As a result of 2D dimming, dynamic contrast ratios of these sets are very high. Dynamic contrast ratio is division of brightness of full white and brightness of full black. It is known that individual LED backlight blocks are capable of turning off. So

this ratio goes to infinite and cannot be measured. In practical, when full black pattern applied to TV, there exists an offset value for measuring and avoid of artifacts. Dynamic contrast ratio does not mean anything to user.

Static contrast ratio gives information about the scene. As distinct from its name, the ratio cannot be static, changes dynamically according to the scene. In this paper, an algorithm developed and applied for increasing static contrast ratio.

In literature, there are similar studies on this issue. Shiga et al., (2008), work on power savings by changing backlight unit via controlling TV signal at and Langendijk et al., (2008) works on increasing contrast gain and power saving with local dimming. Conclusion of these studies, local dimming saves power and increase contrast ratio and there must be a local dimming algorithm to prove this facts. This thesis aim is to develop a local dimming algorithm and show that power saving and difference at contrast ratio. At these studies, LED backlight panel is not used. One of the differences of this thesis is using LED backlight panel.

The thesis contains 6 chapters. First chapter is introduction. The aim of the thesis is explained in this chapter generally.

In second chapter, detailed explanations of display technologies and backlight technologies can be read. Every type of displays and backlights are explained from historical development to how it works.

FPGA basics are mentioned in chapter three. Basic information, architectures, historical development and why FPGA is chosen are shown at this chapter.

Technical explanations which are used in the thesis are given in chapter four. This chapter contains application part of the thesis. Software design section located at this chapter also. This section tells how the software will be applied. Algorithm schematics can be seen at chapter four.

At chapter five the measurement results take part. The measurement tools and patterns will be shown. For each pattern there are two different measurements will be performed at three setups. One of them is full HD 100Hz LCD TV with local dimming, other one is as same as first one except local dimming, the last setup is Full High Definition (HD) 100Hz Liquid Crystal Display TV with Cold Cathode Fluorescent Lamp (CCFL) backlight.

Chapter six is conclusion part of thesis. According to the results, the achievement of the algorithm will be discussed at this chapter.

CHAPTER TWO

DISPLAY AND BACKLIGHT TECHNOLOGIES

Display technology has a critical role explaining how information is transmitted. It is better to describe something by a picture than a thousand words, therefore display technology simplifies information sharing. Cathode Ray Tube (CRT) technology has dominated the display industry from 1922 until the late 20th century. However, new trends such as the desire for mobile electronics have increased demand for displays that rival and surpass CRTs in areas such as picture quality, size, and power consumption. One of the latest devices likely to replace CRTs is Liquid Crystal Displays (LCD) depending on their lightweight, low power consumption and design compactness. LCDs allowed devices such as digital watches, cell phones, laptops, and any small screened electronics to be possible. Although LCDs were initially created for handheld and portable devices, they have expanded into areas previously monopolized by CRTs such as computer monitors and televisions. Other contenders for leadership in display technology are Organic LEDs, DLP technology, Plasma Displays, Field Emission Displays, and Electronic Paper. Organic LEDs, being composed of light emitting polymers, can emit their own light to offer thin and power-saving displays. Using many microscopic mirrors, DLP technology can generate large bright projections on screens with up to 35 trillion colors. Plasma Displays generate excellent quality images on very large screens. Field Emission Displays can produce high resolution images like CRTs without the bulky appearance. The makers of Electronic Paper are trying to replace print by developing displays with many paper-like properties. (Gurski & Quach, 2005, p.3)

2.1 Cathode Ray Tube (CRT)

The earliest version of the CRT was invented by the German physicist Ferdinand Braun in 1897 and is also known as the 'Braun tube'. (Discover in Medicines Co., 2009) It was a cold-cathode diode, a modification of the Crookes tube with a phosphor-coated screen. The first version to use a hot cathode was developed by John B. Johnson (who gave his name to the term Johnson noise) and Harry Weiner Weinhart of Western Electric, and became a commercial product in 1922.

The cathode rays are now known to be a beam of electrons emitted from a heated cathode inside a vacuum tube and accelerated by a potential difference between this cathode and an anode. The screen is covered with a crystalline phosphorescent coating (doped with transition metals or rare earth elements), which emits visible light when excited by high-energy electrons. The beam (or beams, in color CRTs) is deflected either by a magnetic or an electric field to move the bright dot(s) to the required position on the screen. External electromagnets deflect the beams magnetically, while internal plates placed near to and alongside the beam deflect it electrostatically. (Electrostatic deflection is used only for single-beam tubes.)

In television sets and computer monitors the entire front area of the tube is scanned repetitively and systematically in a fixed pattern called a *raster*. A raster is a rectangular array of closely-spaced parallel lines, scanned one at a time, from left to right (and, ever so slightly, "downhill", because the beam is moving steadily down while drawing the image frame). An image is produced by modulating the intensity of each of the three electron beams, one for each primary color (red, green, and blue) with a received video signal (or another signal derived from it). In all CRT TV receivers except some very early models (The earliest commercial TV receivers used electrostatic deflection, even by the end of the 1940s, many of them relying on the famous 7JP4), the beam is deflected by magnetic deflection, a varying magnetic field generated by coils (the deflection yoke), driven by electronic circuits, around the neck of the tube.

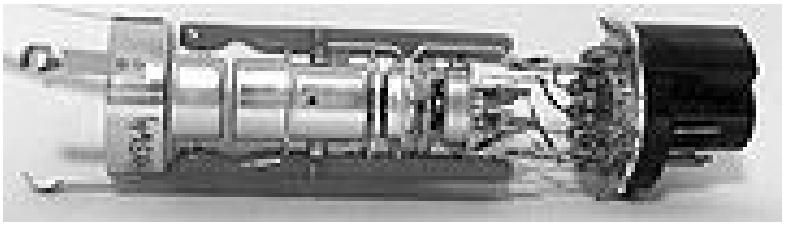


Figure 2.1 Electron gun. (Wikimedia Foundation Inc. , 2004)

The source of the electron beam is the electron gun, which produces a stream of electrons through thermionic emission, and focuses it into a thin beam. Electron gun can be seen at Figure 2.1. Earlier, black-and-white TV CRTs used magnetic focusing, but electrostatic focus has totally superseded focus coils. The gun is located in the narrow, cylindrical neck at the extreme rear of a CRT and has electrical connecting pins, usually arranged in a circular configuration, extending from its end. These pins provide external connections to the cathode, to various grid elements in the gun used to focus and modulate the beam, and, in electrostatic deflection CRTs, to the deflection plates. Since the CRT is a hot-cathode device, these pins also provide connections to one or more filament heaters within the electron gun. When a CRT is operating, the heaters can often be seen glowing orange through the glass walls of the CRT neck. The need for these heaters to 'warm up' causes a delay between the time that a CRT is first turned on, and the time that a display becomes visible. In older tubes, this could take fifteen seconds or more; modern CRT displays have fast-starting circuits which produce an image within about two seconds, using either briefly increased heater current or elevated cathode voltage. Once the CRT has warmed up, the heaters stay on continuously. The electrodes are often covered with a black layer, a patented process used by all major CRT manufacturers to improve electron density. (Wikimedia Foundation Inc. , 2004)

The electron gun accelerates not only electrons but also ions present in the imperfect vacuum (some of which result from outgassing of the internal tube components). The ions, being much heavier than electrons, are deflected much less by the magnetic or electrostatic fields used to position the electron beam. Ions striking the screen damage it; to prevent this the electron gun can be positioned slightly off the axis of the tube so that the ions strike the inside of the CRT neck instead of the screen. Permanent magnets (the *ion trap*) deflect the lighter electrons so that they strike the screen. Some very old TV sets without an ion trap show

browning of the center of the screen, known as ion burn. The aluminum coating used in later CRTs eliminated the need for ion traps; they are no longer used.

When electrons strike the poorly-conductive phosphor layer on the glass CRT, it becomes electrically charged, and tends to repel electrons, reducing brightness (this effect is known as "sticking"). To prevent this, the interior side of the phosphor layer can be covered with a layer of aluminum connected to the conductive layer inside the tube, which disposes of this charge. It has the additional advantages of increasing brightness by reflecting, towards the viewer, the light emitted towards the back of the tube. The aluminum layer also protects the phosphors from ion bombardment.

CRTs were embraced as output devices very early in the development of digital computers. There close cousins, vacuum tubes, were some of the first switching elements used to build computers. Today, the CRT is the last remaining vacuum tube in most systems (Even the flashing lights are solid-state LEDs). Structure of CRT display can be seen at Figure 2.2.

Most likely, oscilloscopes were some of the first computer graphics displays. The results of computations could be used to directly drive the vertical and horizontal displacement plates in order to draw lines on the CRT's face. By varying the current to the heating filament the output of the electron beam could also be controlled. This allowed the intensity of the lines to vary from bright to completely dark.

Color CRT's are more complicated than the simple monochrome models summarized above. The phosphors on the face of a color CRT are laid out in a precise geometric pattern. There are two primary variations, the *stripe* pattern of in-line tubes shown on the left, and the *delta* pattern of delta tubes as shown on the right.

Within the neck of the CRT there are three electron guns, one each for red, green, and blue (the actual beams are all the same color-- *invisible*). There is also a special metal plate just behind the phosphor cover front face, called a *shadow mask*. This mask is aligned so that it simultaneously allows each electron beam to see only the phosphors of its assigned color and blocks the phosphor of the remaining two colors.

Despite the rapid rise of display solutions based on various flat screen technologies, CRT displays are still in the market and new products are being launched. Arguably, CRT technology continues to offer a superior quality of picture and higher contrast ratios than FPDs and at highly competitive costs (although see the discussion of total cost of ownership when power consumption is considered) and it is likely that CRT will continue to dominate the very low end of the TV market for some time. They are also challenging the 'thinness' issue. Samsung recently announced plans to produce a CRT 32-inch TV display with a depth that is half that of existing solutions. (Discover in Medicines Co., 2007)

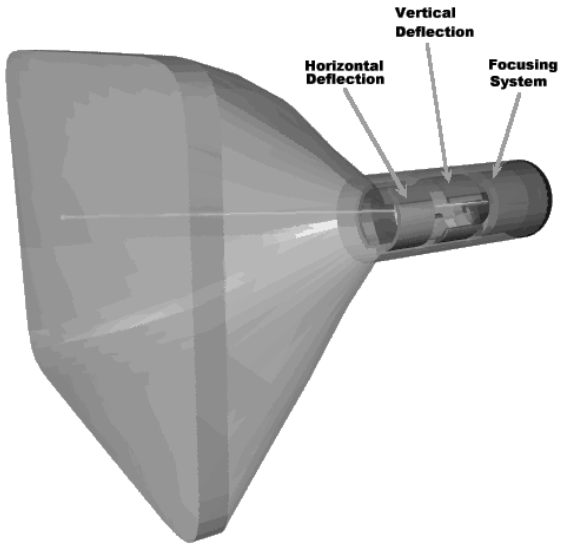


Figure 2.2 Structure of CRT

2.2 Plasma Display Panel (PDP)

By definition, plasma is a state of matter (gas) where atoms are ionized by adding energy - in this case electrical energy by applying a voltage between two electrodes and which eventually leads to the flow of an electric current. In the process, positive and negative charged particles move fast towards the respectively opposite charged electrodes.

The photon is that elementary particle responsible for all electromagnetic phenomena; it carries electromagnetic radiation - from gamma to radio. If it falls within the light spectrum, visible or otherwise - it is called a light photon.

The released light photons are in effect ultraviolet photons - meaning that the emitted radiation is invisible to the human eye. Ultraviolet light photons can be used to produce visible light by exciting phosphor atoms. Phosphors are substances that give off visible light photons when their atoms are hit by ultraviolet photons. The collision causes electrons to jump to a higher energy level - which energy is then released in the form of a visible light photon when the electron returns to its normal energy level. Different phosphor formulations yield different colors of light. (Wikimedia Foundation Inc. , 2005)

A plasma display panel (PDP) is a type of flat panel display common to large TV displays (32 inches or larger). Many tiny cells between two panels of glass hold an inert mixture of noble gases. The gas in the cells is electrically turned into plasma which then excites phosphors to emit light. Plasma displays should not be confused with LCDs, another lightweight flat screen display using different technology.

Plasma displays are bright (1000 lux or higher for the module), have a wide color gamut, and can be produced in fairly large sizes, up to 381 cm (150 inches) diagonally. They have a very low-luminance "dark-room" black level compared to the lighter grey of the unilluminated parts of an LCD screen. The display panel is

only about 6 cm (2.5 inches) thick, while the total thickness, including electronics, is less than 10 cm (4 inches). Plasma displays use as much power per square meter as a CRT or an AMLCD television. Power consumption varies greatly with picture content, with bright scenes drawing significantly more power than darker ones, as is also true of CRTs. Nominal power rating is typically 400 watts for a 50-inch (127 cm) screen. Post-2006 models consume 220 to 310 watts for a 50-inch (127 cm) display when set to cinema mode. Most screens are set to 'shop' mode by default, which draws at least twice the power (around 500-700 watts) of a 'home' setting of less extreme brightness.

The lifetime of the latest generation of plasma displays is estimated at 100,000 hours of actual display time, or 27 years at 10 hours per day. This is the estimated time over which maximum picture brightness degrades to half the original value, not catastrophic failure.

Plasma displays also have their drawbacks. They are often criticized for reflecting more ambient light than LCD displays. The screen is made from glass, which reflects more light than the material used to make an LCD screen, which creates a glare. Although companies, such as Panasonic, coat their newer plasma screens with an anti-glare filter. Plasma panels currently cannot be made in screen sizes smaller than 32". Although few companies have been able to make plasma EDTVs this small, even fewer have made 32" plasma HDTVs. The 32" screen size is also "going extinct". Plasma displays are also considered bulky and thick (usually six inches in depth) compared to their LCD counterparts. Panasonic aims to solve the thickness issue by releasing the Viera Z1 series, which are only one inch thick. Plasma displays also tend to consume more electricity than LCD displays. Panasonic, once again aims to solve this dilemma by using Neo-PDP screens for their 2009 series of Vieras. Panasonic states that the PDPs will consume half the power to achieve the same overall brightness.

Competing displays include the CRT, OLED, AMLCD, DLP, SED-TV, and field emission flat panel displays. Advantages of plasma display technology are that a large, very thin screen can be produced, and that the image is very bright and has a

wide viewing angle. The viewing angle characteristics of plasma displays and flat-face CRTs are essentially the same, topping all LCD displays, which have a reduced viewing angle in at least one direction. Plasma TVs also do not exhibit an image blur common in many LCD TVs.

The xenon, neon, and argon gas in a plasma television is contained in hundreds of thousands of tiny cells positioned between two plates of glass. Long electrodes are also put together between the glass plates, in front of and behind the cells. The address electrodes sit behind the cells, along the rear glass plate. The transparent display electrodes, which are surrounded by an insulating dielectric material and covered by a magnesium oxide protective layer, are mounted in front of the cell, along the front glass plate. Control circuitry charges the electrodes that cross paths at a cell, creating a voltage difference between front and back and causing the gas to ionize and form plasma. As the gas ions rush to the electrodes and collide, photons are emitted.

In a monochrome plasma panel, the ionizing state can be maintained by applying a low-level voltage between all the horizontal and vertical electrodes – even after the ionizing voltage is removed. To erase a cell all voltage is removed from a pair of electrodes. This type of panel has inherent memory and does not use phosphors. A small amount of nitrogen is added to the neon to increase hysteresis.

In color panels, the back of each cell is coated with a phosphor. The ultraviolet photons emitted by the plasma excite these phosphors to give off colored light. The operation of each cell is thus comparable to that of a fluorescent lamp.

Every pixel is made up of three separate sub-pixel cells, each with different colored phosphors. One sub-pixel has a red light phosphor, one sub-pixel has a green light phosphor and one sub-pixel has a blue light phosphor. These colors blend together to create the overall color of the pixel, the same as a "triad" of a shadow-mask CRT or color LCD. By varying the pulses of current flowing through the different cells thousands of times per second, the control system can increase or decrease the intensity of each subpixel color to create billions of different combinations of red, green and blue. In this way, the control system can produce

most of the visible colors. Plasma displays use the same phosphors as CRTs, which accounts for the extremely accurate color reproduction when viewing television or computer video images (which use an RGB color system designed for CRT display technology.) Structure of plasma panel is shown at Figure 2.3.

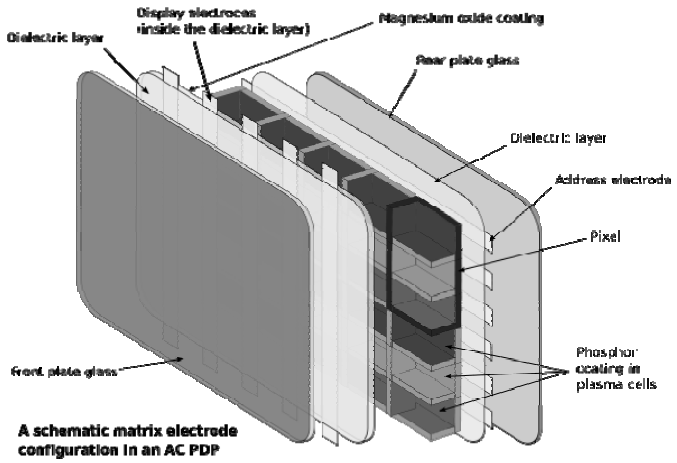


Figure 2.3 Structure of plasma panel (Wikimedia Foundation Inc. , 2005)

2.3 Liquid Crystal Display LCD

Liquid crystals were discovered in 1888, but their potential application in display technology was not realized until 1968 when researchers from the RCA's David Sarnoff Research Center developed the first liquid crystal display. Since then, LCDs have revolutionized the small screen and portable electronic market offering an alternative to CRTs and making devices like calculators, cell phones, PDAs, and laptops possible. As LCD designs advance, they will remain a popular part of home entertainment systems and continue to dominate handheld electronics.

2.3.1 Liquid Crystals

An Austrian botanist by the name of Friedrich Reinitzer was the first person to perform research on liquid crystals. In 1888 he conducted an experiment involving a material known as cholesterly benzoate. In his experiment Reinitzer observed changes in a solid sample of cholesterly benzoate as he increased the applied temperature. He noticed that as the temperature increased the solid sample became a hazy liquid and then changed into a transparent liquid. A physics professor named Otto Lehmann having learned of Reinitzer's discovery conducted his own research confirming that the substance seem to have two distinct melting points; his research led him in 1889 to coin the term 'liquid crystal'.

Liquid crystals are substances that exhibit properties of both solids and liquids; they are an intermediate phase of matter. Liquid crystals can be classified into three different groups, nematic, smectic, and cholestric depending on the level of order in their molecular structure. Liquid crystals in the nematic group are most commonly used in LCD production because of their physical properties and wide temperature range. In the nematic phase, liquid crystal molecules are oriented on average along a particular direction. By applying an electric or magnetic field, the orientation of the molecules can be manipulated in a predictable manner; this mechanism provides the basis for LCDs. (Gurski & Quach, 2005)

2.3.2 Liquid Crystal Display Basics

Simple LCDs consist of a liquid crystal cell, conductive electrodes and a set of polarizing lenses. The structure for a simple LCD is shown in the diagram below at Figure 2.4.

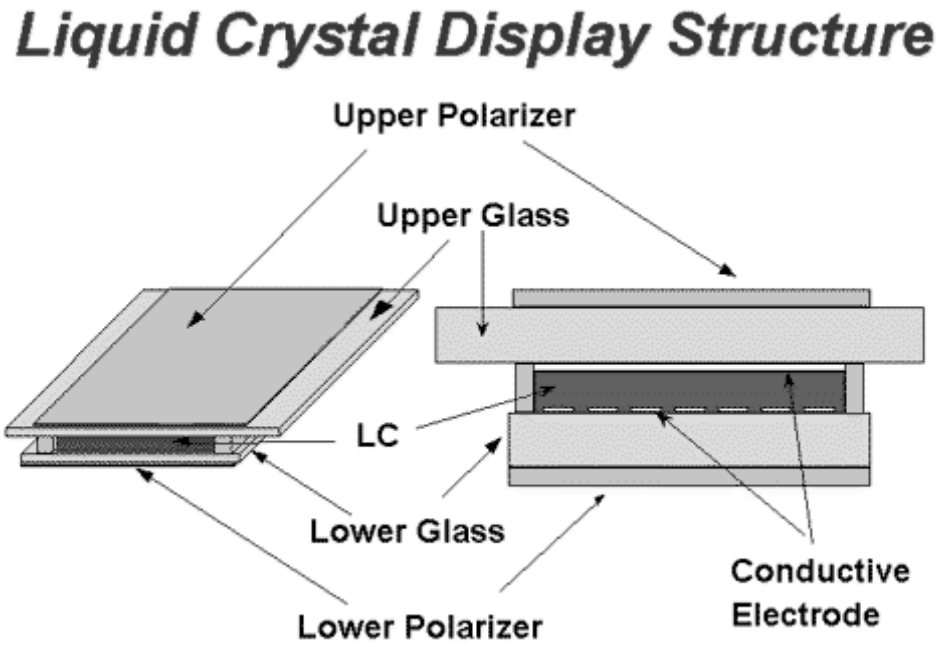


Figure 2.4 Basic diagram of an LCD. (Gurski & Quach, 2005)

2.3.2.1 The Liquid Crystal Cell

To use liquid crystals in display technology, the ability to control how their molecules are naturally arranged is needed. In their natural state, liquid crystal molecules in the nematic phase are loosely ordered with their long axes parallel; to change this arrangement they are placed onto a finely grooved surface. When they come into contact with a finely grooved surface also called the alignment layer, the molecules line up parallel along the grooves.

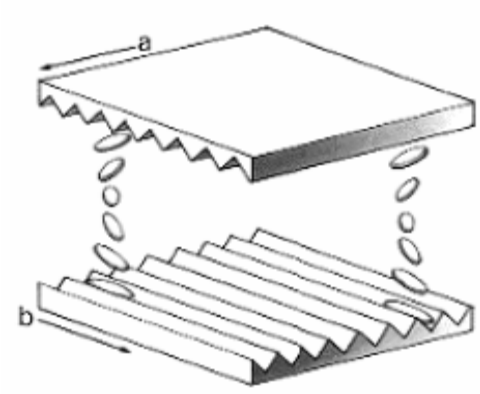


Figure 2.5 Molecules near each plate line up in respected directions. (Morris, 1993)

Figure 2.5 shows the directions of molecules. Light sent through the twisted liquid crystal structure curls following the molecular arrangement and figured at Figure 2.6. By changing the orientation of the liquid crystals, light propagating through is also changes to follow.

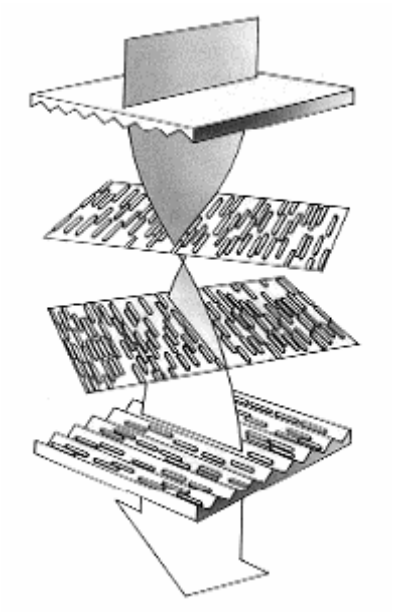


Figure 2.6 Light rotates following the molecular arrangement. (Morris, 1993)

Conductive electrodes are used to apply voltage to the liquid crystal cell as shown at Figure 2.7. When a voltage is applied the molecules straighten out aligning parallel to the applied electric field; this also allows propagating light to pass directly through.

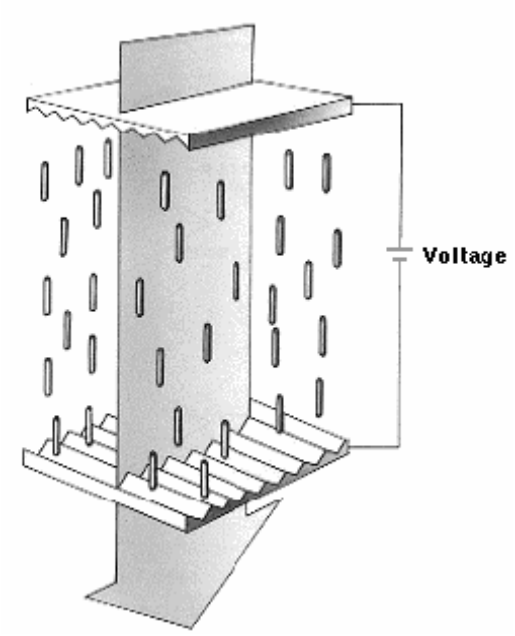
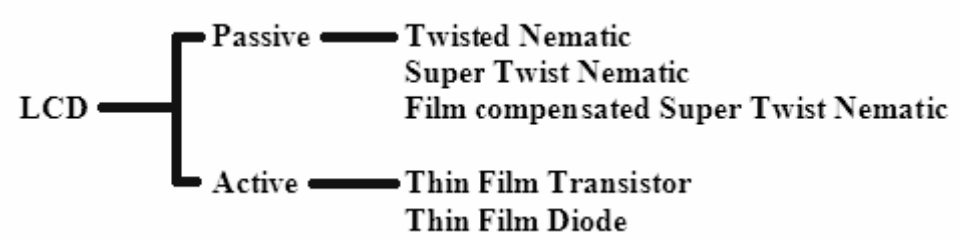


Figure 2.7 Liquid crystal molecules follow an applied electric field. (Morris, 1993)

2.3.4 Liquid Crystal Display Types

LCDs are broken up into two main groups: passive displays and active displays. Passive and active refer to the circuits that are responsible for activating pixels.



Passive LCDs use electrical components that do not supply their own energy to turn ‘on’ or ‘off’ desired pixels. A passive matrix LCD is made up of a set of multiplexed (a method of reducing the number of I/O lines needed) transparent electrodes. The electrodes are made of a conductive film, usually indium-tin oxide or ITO and are placed above and below the liquid crystal layer in a row/column formation (see Figure 2.8). The rows and columns are then connected to integrated circuits, which control when and where charge is delivered. To address a pixel the

column containing the pixel is sent a charge; the corresponding row is connected to ground. When sufficient voltage is placed across the pixel, the liquid crystal molecules align parallel to the electric field.

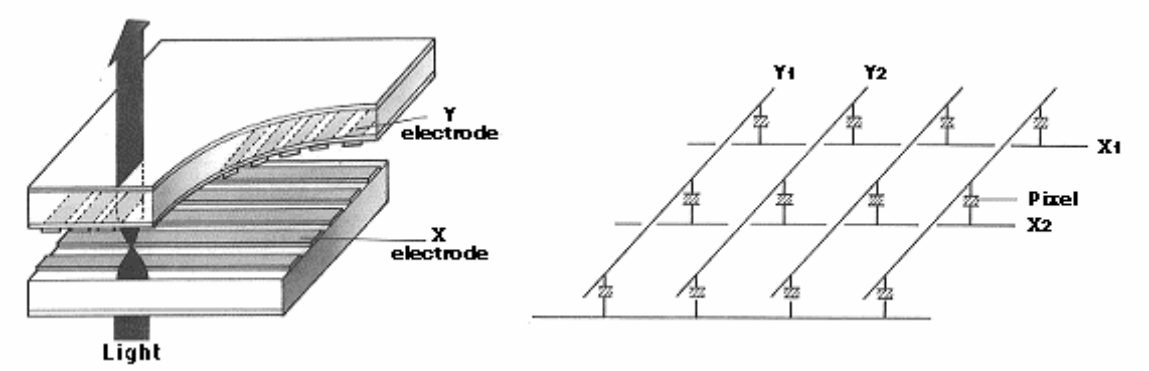


Figure 2.8 Structural and circuit level diagrams of a passive matrix. (Gurski & Quach, 2005)

Multiplexed passive screens were the solution to creating larger LCDs. In a ten by ten array of pixels one hundred separate connections would be needed to be able to address all of them. If the lines were multiplexed then only 20 connections would be needed (one for each row and column). In general the number of connections needed for non-multiplexed lines is M x N where 'M' and 'N' are the number of rows and columns in an array. When multiplexing is used, the number of connections is M+N. To activate pixels in a multiplexed array carefully timed voltage pulses are sent to corresponding rows and columns. Pulses are coordinated so that they reach the right pixel at the right time without activating unwanted pixels. Timing, duration and amplitude of pulses are controlled by driver circuitry external to the passive matrix. The diagram of LCD with color filter is shown at Figure 2.9.

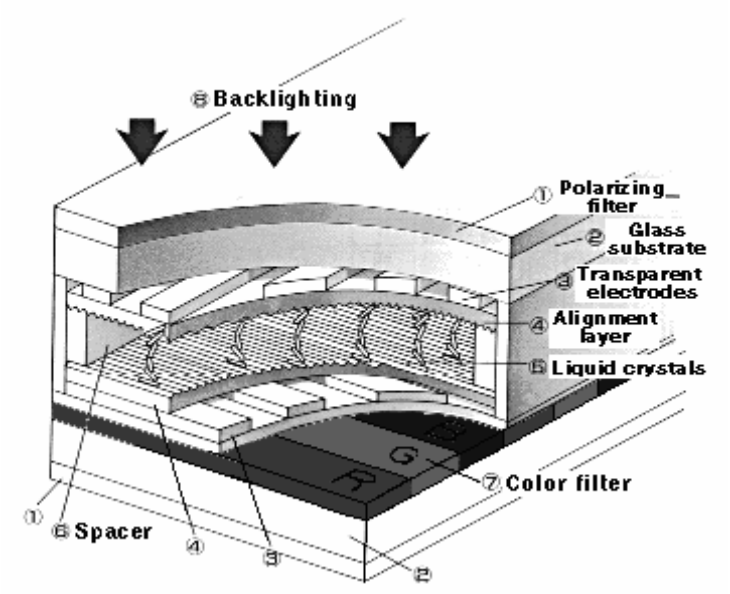


Figure 2.9 Diagram of LCD with color filters added. (Gurski & Quach, 2005)

Active liquid crystal displays have a similar construction to the passive implementation. Just like a passive display, active LCDs use a semi transparent conductive grid to supply charge to the liquid crystal layer. The important difference is that the active displays have a transistor built into each pixel. This thin film transistor (TFT) acts like a switch precisely controlling the voltage each pixel receives. As shown in the diagram below the basic structure of an active matrix LCD or a TFT display is a common electrode placed above the liquid crystal matrix. Below the liquid crystal is a conductive grid connected to each pixel through a TFT. Inside each pixel the structure is as follows, the gate of each TFT is connected to the row electrode, the drain to the column electrode, and the source to the liquid crystal. To activate the display voltage is applied to each row electrode line by line. To turn on a pixel the gate lines have to be activated; this closes the switch and allows charge from the drain to flow to the source setting up an electric field between the source and the common electrode above. The column electrodes connected to the drain carry the data voltages (which pixels to activate and to what shade) and are synchronized to the gate pulses. Connected to the source of each TFT in parallel with the liquid crystal is a small capacitor. When a pulse is sent to the gate, charge flows from the drain to the source where the capacitor charges to the desired level. The purpose of the capacitor is to keep voltage applied to the liquid crystal molecules until the next

refresh cycle. Capacitors are sized large enough to keep a constant voltage on activate pixels, over the entire refresh cycle. Structure diagram and circuit diagram is shown at Figure 2.10.

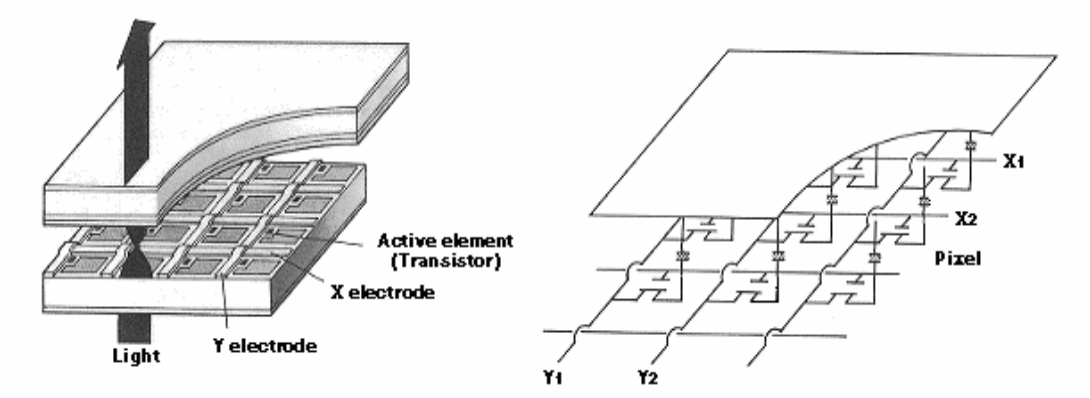


Figure 2.10 Structural and circuit level diagrams of an active matrix. (Gurski & Quach, 2005)

LCD technology had been in development for almost forty years, and will continue into the near future. Each day new ways are devised to improve the brightness, contrast, and overall picture quality of LCDs. New materials are under research in order to give TFT screens faster refresh times, and to lower power usage. LCDs are making progress, but must continue to improve if they are to remain competitive against other emerging display technology.

2.4 Organic Light Emitting Diodes (OLEDs)

One of the next trends in display technology is Organic Light Emitting Diodes (OLEDs). Polymer Light Emitting Diodes (PLEDs), Small Molecule Light Emitting Diodes (SMOLEDS) and dendrimer technology are all variations of OLEDs. With all variations being made by electroluminescent substances (substances that emit light when excited by an electric current), OLED displays are brighter, offer more contrast, consume less power, and offer large viewing angles – all areas where LCDs fall short.

2.4.1 Fundamentals of OLEDs

OLEDs are composed of light-emitting organic material sandwiched between two conducting plates, one of n-type material and one of p-type material. The molecular structure in n-type material, although electrically neutral, has an extra electron that is relatively free to move around the material. In p-type material the opposite is true. The lack of an electron creates a hole that is free to move about. The creation of the extra electron or the hole comes about because of the mismatch of valence electrons in the molecular structure of the p or n-type material. Applying a voltage between the two plates causes holes to be injected from the p-type substrate and electrons to be injected from the n-type substrate. When an Electron fills in a hole, it drops from a higher energy level to a lower one; consequently, this difference in energy is released as a photon of light (light particle). The wavelength of the light generated is dependant on the energy gaps of the emitting material. In order to produce visible light, these energy gaps have to be within 1.5 to 3.5 electron volts (eV). For example, a photon of 3.1 eV has a wavelength of 400 nm which is visible as a violet light. Therefore, the colors emitted are dependant on the molecular composition of the organic emissive material chosen for the OLED.

2.4.2 Structure and Types of OLEDs

OLEDs were first developed by Eastman Kodak in 1987. Their method of producing OLEDs was known as the Small Molecular method. Based on the Small Molecular method, PLEDs and dendrimers were later developed. While their structures remained approximately the same, the organic material was different.

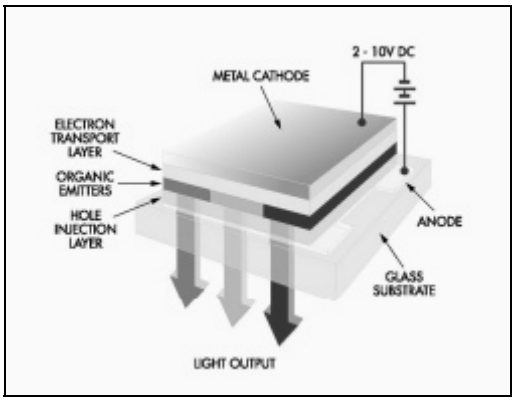


Figure 2.17 OLED structure. (Antoniadis, 2004)

The structure of a basic SMOLED contains multiple layers of organic material. (See Figure 2.14) Depending on the organic chemicals that are used to generate the display, different manufacturing techniques can be used. The p-type layer, known as the anode, is made from a high work function material such as indium tin oxide (ITO) – known for its conductive and transparent properties. The next layer is an organic material which aids in the transportation of holes known as normal-propyl-bromide (NPB). Following this layer is one which aids in the transport of electrons; tris-8-ydroxyquinoline aluminum (alq3) is generally used to form it. Lastly, the n-type layer, known as the cathode, is made from a low work-function material such as MgAg (magnesium silver) to produce the electrons. In order to improve efficiency, a luminescent layer is normally added in between the two layers of organic material, and is generally composed of a mixture of alq3 and C540 (a carbon derivative). C540 is responsible for the added fluorescence. SMOLEDs require a complicated process of vacuum vapor deposition, where the deposition method involves sublimating the material in a vacuum. This process allows for a more accurate and better controlled application of these layers onto the display substrate; however, vapor vacuum deposition is also very complex, and as a result, this renders to higher manufacturing costs. Therefore, SMOLEDs are more suited for smaller displays such as cell phones, camera displays, etc. where they can produce excellent color displays with a long lifetime.

2.4.4 OLED Benefits

Because of the OLEDs' thin structure and excellent display qualities, it is ideal for use in flat-panel displays. OLEDs have many advantages compared to LCD technology – today's leader in this area. OLEDs are emissive displays (meaning they generate their own light), and as a result require no backlighting. Another significant advantage is OLED displays have extremely high switching speeds and as a result can handle high refresh rates required for full-motion video. OLEDs also have a large viewing angle as a result of its self-luminous effect.

2.5 Digital Light Processing (DLP)

DLP technology is a system that uses an optical semiconductor developed by Dr. Larry Hornbeck of Texas Instruments in 1987. This device, known as a Digital Micromirror Device (DMD chip), is essentially a very precise light switch that can digitally modulate light through the use of 2 million hinge-mounted microscopic mirrors arranged in a rectangular array; each of these micromirrors are less than 10 microns (approximately one-fifth the width of a human hair). Combined with a digital video or graphic signal, a light source, and a projection lens, the mirrors of the DMD chip can reflect an all-digital image onto any surface. A DLP Chip and color display process is shown at Figure 2.15.

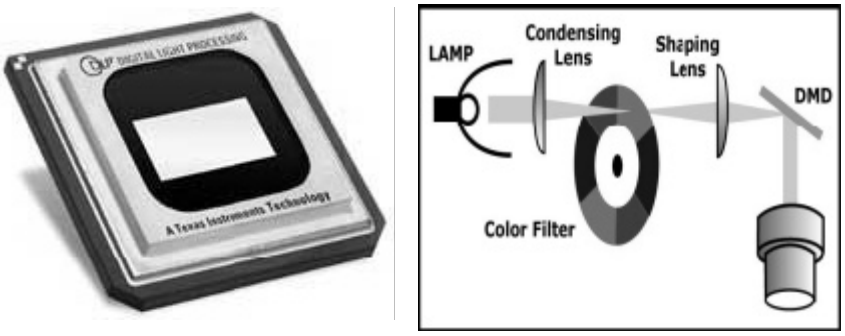


Figure 2.15 DMD chip and DLP color display process (Antoniadis, 2004

2.5.1 DLP Structure

By mounting these micromirrors on tiny hinges, they are able to tilt either toward the light source where they are noted as being “on” or away from the light source where they are noted as being “off”. Consequently, depending on the state of these mirrors, a light or a dark pixel is projected onto the screen. The mirrors are instructed to switch on or off several thousand times per second by a digital signal entering the semiconductor. A lighter shade of grey is produced when a mirror is switched on more frequently than off; whereby a darker shade of grey is produced when a mirror is switched off more frequently than on. Using this method, DMD chips can generate up to 1024 shades of grey and consequently produce a highly detailed greyscale image.

2.5.2 DLP in Color

In most DLP systems, a color wheel is placed between the light source and the mirrored panel. As the color wheel spins, it causes the white light generated by the light source to filter into red, green, and blue light to fall on the DMD mirrors. When the on/off states of each mirror are coordinated with the flashes of colored light, the DLP system can generate approximately 16 million colors. For example, a purple pixel is created by switching on the mirror only when red or blue light is falling on it. Our eyes then combine these primary colors to see the intended purple.

2.5.3 DLP Uses

Projectors, TVs, and home theatre systems are currently based on DLP systems that use a single DMD chip. Larger venues like cinemas tend to use DLP systems that use three DMD chips. The difference being the white light generated by the light source is passed first through a prism and is then filtered into red, green, and blue.

Each DMD chip is then dedicated to each primary color and the reflected light is then combined and passed through the projector lens to a screen. The result is a system that can produce up to 35 trillion colors for the ultimate movie experience.

As mentioned previously, DLPs are currently limited to projection technology and have not been developed for smaller screen displays such as monitors and cell phones.

2.6 Field Emission Displays (FEDs)

Field emission displays (FEDs) function much like CRT technology. Instead of using one electron gun to emit electrons at the screen, FEDs use millions of smaller ones. The result is a display that can be as thin as an LCD, reproduce CRT-quality images, and be as large as a plasma display. Initial attempts in making emissive, flat-panel displays using metal tipped cathodes occurred nearly 20 years ago, however, with reliability, longevity, and manufacturing issues, these types of FEDs do not seem commercially viable.

2.6.1 Field Emission Fundamentals

The foundation of Field Emission technology is the extraction of electrons from a material using the "tunneling" effect. Tunneling describes the phenomenon of electrons being able to behave likes waves as well as like particles. Within a conductor, free electrons are generally mobile within a certain degree. What prevents these electrons from simply escaping the bounds of conductors is a potential energy barrier. In order to surpass this potential energy barrier, electrons must be provided with enough energy. However, with the tunneling effect, (see Figure 2.16) if a high enough electric field is applied outside the conductor, the strength of the potential energy barrier will be reduced, and consequently it will get to the point where an electron wave can extend itself across the barrier.

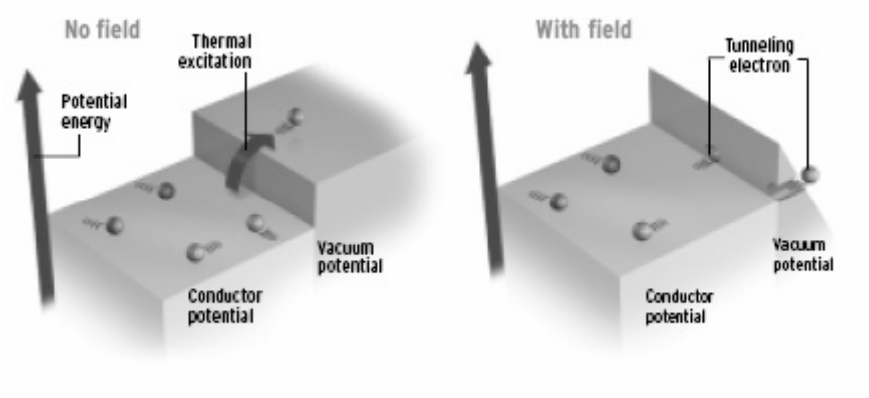


Figure 2.16 The tunneling effect (Guarski & Quach, 2005)

The emitted current, or moving electrons, depends on the electric field strength, the emitting surface, and the work function. In order for field emission to function, the electric field has to be extremely high: up to 3 x 107 V/cm. This value, though large, is accessible by the fact that field amplification increases with a decreasing curvature radius indicating that the pointier the object, the more charge it will have at its tip, and hence the larger the electric field. As a result, if such a material can be found, a moderate voltage will cause the tunneling effect, and hence allow electrons to escape into free space without the heating of the cathode like the traditional Cathode Ray Tube (CRT) technology.

2.6.2 Traditional FED Structure

The basic structure of the first FED was comprised of millions of vacuum tubes, called microtips. Each tube was red, green, or blue and together, formed one pixel. These microtips were sharp cathode points made from molybdenum from which electrons, under a voltage difference, would be emitted towards a positively charged anode where red, blue, and green phosphors were struck, and as a result emit light through the glass display. Unlike CRTs, color was displayed sequentially, meaning the display processed all the green information first, then refreshed the screen with red information, and finally blue.

The advantages of the traditional FED included the fact that they only produced light when the pixels were "on", and as a result power consumption was dependent on the display content. A FED also generated light from the front of the pixel, providing an excellent viewing angle of 160 degrees both vertically and horizontally. These FEDs also had a high product yield as thousands of electron emitters were in place for each pixel; they suffered no brightness loss even if 20% of the emitters failed. Though this technology seemingly could have been a huge contender in the flat panel business, it was plagued with many problems due to the extreme electrical environment of the display. One problem being the metal molybdenum, used to make the microtips, would become so heated that local melting would result and consequently deform its sharp tips needed to form the electric field used for electron emission. Another problem caused by the electrical environment was the hot cathodes would react with the residual gases in the vacuum consequently reducing the field emission even more.

2.7 Backlight Technologies

A key component in the deployment of Liquid Crystal Display (LCD) technology for outdoor applications is the integration of a high bright backlight (or light source) behind the LCD glass. There are several different LCD backlight technologies being

employed in the outdoor digital signage market today; Cold Cathode Fluorescent Lamp (CCFL), External Electrode Fluorescent Lamp (EEFL), Hot Cathode Fluorescent Lamp (HCFL), Light Emitting Diode (LED), and Flat Fluorescent Lamp (FFL). There are advantages and disadvantages for each technology as it pertains to outdoor environments where displays are typically subject to direct sunlight across a wide range of temperature and humidity conditions. In order to perform well in these environments, the backlight must meet certain minimum criteria for outdoor use that include brightness, reliability, efficiency, thermal packaging, and color reproduction. In LCD panels, the majority of power consumption in the product comes from the backlight source. With today's energy costs skyrocketing, the efficiency and longevity of the backlight plays a critical role in the cost of operation, and ultimately in the total cost of ownership. This white paper provides a comparison of the current backlight technologies available today for outdoor display applications and provides insight into Delphi's long term backlight technology development roadmap.

2.7.1 Cold Cathode Fluorescent Lamp (CCFL)

Cold Cathode Fluorescent Lamps (CCFL), (other abbreviations include CFL (Cold Florescent Lamp) and CCFT (Cold Cathode Fluorescent Tube)) are the most commonly used form of LCD backlighting at present. This is due to exceptional brightness and full spectral output. A CCFL is a thin (outer diameters as small as 1.6mm) glass tube with an internal vacuum. A pressurized Neon/Argon mix sealed within the fluorescent tube is excited by a high AC voltage with a striking voltage > 1000 V and a sustained voltage of 100 ~ 300 VAC (please check individual data sheets as appropriate). A DC/AC inverter is required to generate these high alternating voltages. The electrons within the gas become highly energized and when they strike the fluorescent material coated on the inner surface of the tube cause the fluorescent material to fluoresce and emit white light. The CCFL is normally used with a light-guide to illuminate a surface area (Figure 2.17).

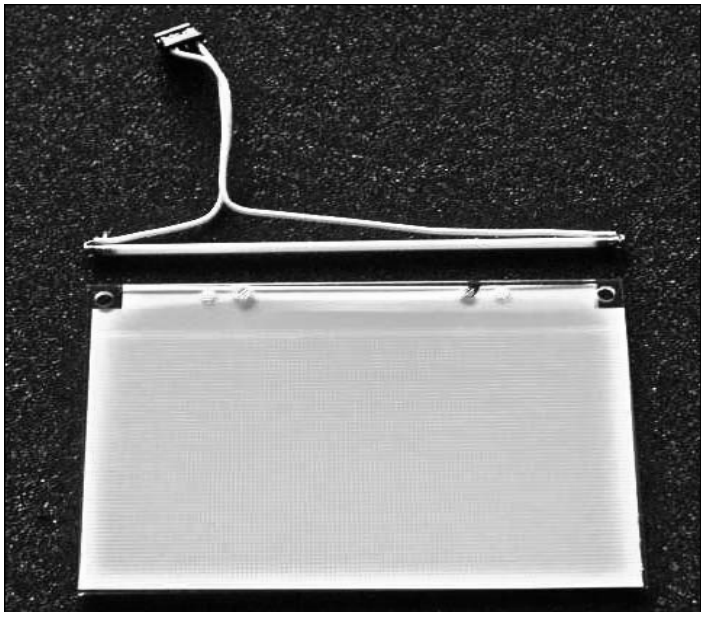


Figure 2.16 Cold Cathode Fluorescent Lamp (CCFL) with Light-Guide (Chaddertor, 1996)

One potential issue with Cold Cathode Fluorescent Lamps (CCFLs) is operation in cold temperatures. When a CCFL gets very cold (below 0°C), the strike voltages become excessive and it may not turn on at all. In addition, the lifetime of the CCFL at low temperatures will be reduced. At normal operating temperatures, CCFLs have a very long life – 50,000 hours is common for new generation lamps.

The CCFL is used with two main configurations. The primary configuration used in LCD backlighting is line source with a light-guide (sometimes called side lighting). The other configuration which increases the brightness at the expense of the power requirements uses several CCFLs directly behind the LCD without the use of a light-guide.

2.7.1 Light Emitting Diodes (LED)

Light Emitting Diode (LED) backlighting is a popular backlighting method for small and medium LCDs. The advantages of LED backlighting are low cost (at least for small area displays), long life, immunity to vibration, low operational voltage, and precise control over its intensity. LED backlights come in a variety of colors, with white becoming a cost effective and very popular option. LED backlights offer

a long operating life of 15,000 hours minimum for white and can be much longer for other colors. Being a solid state device, they are configured to operate typically with +5VDC power, so no inverter is required. The LED backlighting is also used in conjunction with a light-guide (Figure 2.17).

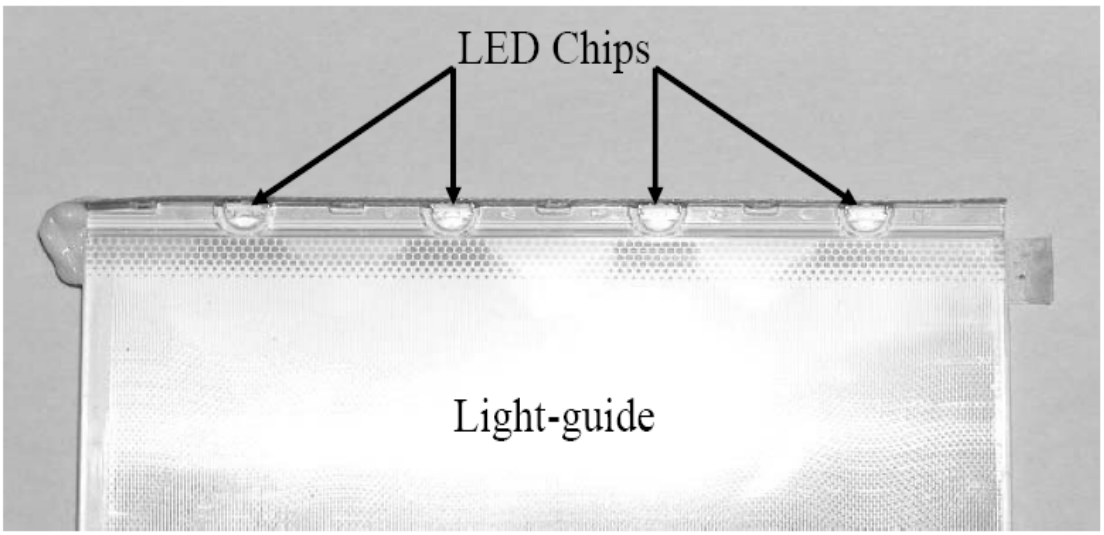


Figure 2.17 Light Emitting Diode (LED) with Light-Guide (Chaddertor, 1996)

LED backlights have two basic configurations. In the Array lit configuration there are many LEDs mounted uniformly behind the display offering a very bright illumination but with high power consumption (*Figure 5*). In the Edge lit configuration, the LEDs are mounted on the edge of a plastic light guide (*Figure 2*) and the light is focused into the light-guide (*Figure 6*). The edge lit configuration offers a thinner package with lower power consumption and is the most widely used system in the industry. (Yu, 2006)

2.7.2.1 Advantages of LEDs

The main advantages of LEDs are:

- Long Service Life
    - 100,000 hours time to ½ life- YG, Red and Amber
    - 50,000 hours Green
    - 20,000 to 40,000 hours for Blue and White

• Good environmental performance including high UV, high temperature and high humidity resistance
• High MBTF
• Solid-state chip embedded in epoxy- nothing to break or burn out
• LED consumption is increasing, driving costs down
• Low heat generation
• No EMI or RFI
• Low Power (5 to 30 mA at 3.6 or 2.2 Vdc)
• New narrower beam, light focusing packages that are better utilized in light guides
• Many color choices

2.7.2.2 Disadvantage of LEDs

The main disadvantages of LEDs are:

• Sensitive to ESD
• Sensitive to voltage spikes
• Heat dissipation in some applications
• Not true full spectrum White LED (unless tri-color) (Lim, 2006)

2.7.3 Electroluminescent Panel (ELP)

Electro Luminescent (EL) backlights use a solid state phenomenon based on colored phosphors to generate light when an AC voltage is applied to the EL panel. EL backlights are very thin, lightweight and provide an even distribution of light, without the need of a light-guide (Figure 2.18).

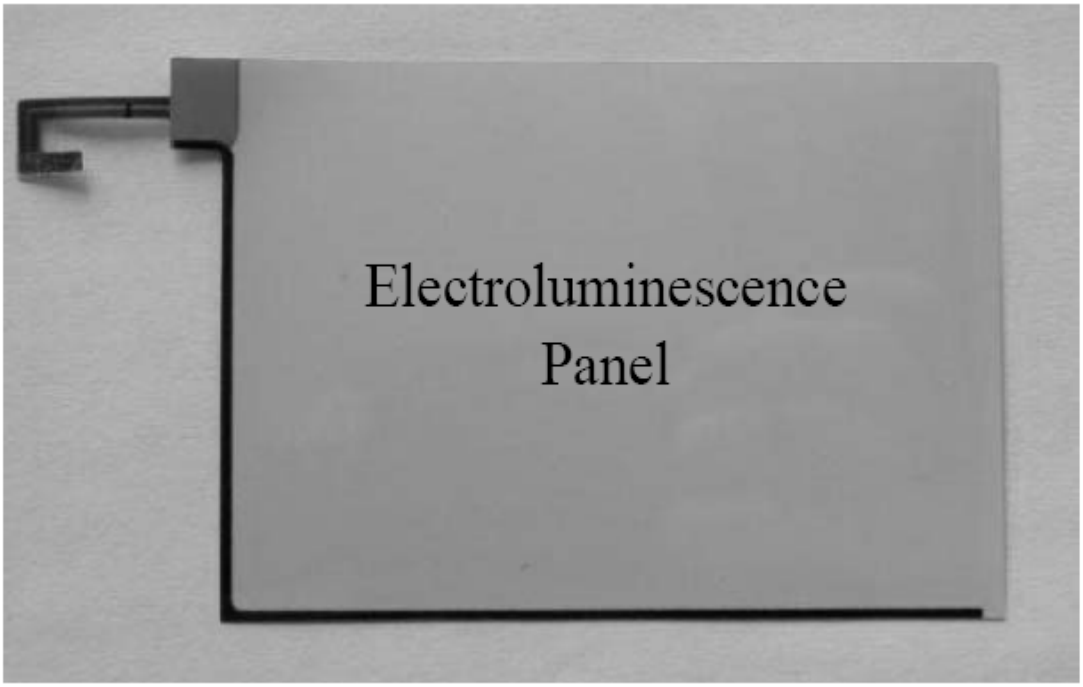


Figure 2.18 Electroluminescent Panel (ELP) (Lim, 2006)

They are available in a variety of colors, with white being the most popular for use with LCDs. While their power consumption is fairly low, they require voltages of 100 VAC @ 400Hz. This is supplied by an inverter that converts a 5, 12 or 24 VDC input to the AC output. EL backlights also have a limited life of 3,000 to 5,000 hours to half brightness (half-life). The limited brightness and lifetime of EL panels has made them unpopular and they are rarely used to backlight graphical LCDs. EL has only one configuration, broad area emitter. (Lim, 2006)

Backlight technology will play a critical role in the development of the LCD market going forward. As more importance is placed on picture quality, lifetime, and power consumption, the technologies that provide benefits in these areas will win out in the long run. Today, the vast majority of LCD-TVs utilize CCFL backlights. Accordingly, CCFL will continue to play an important role in the foreseeable future due to its good efficiency and price-to-performance ratio. The two emerging backlight technologies that are being embraced by the industry are EEFL and LED. EEFL offers improved power efficiency, though much work remains to solve the mercury issue. LED backlights have the most promising market and environmental improvement potential in the mid-term to long-term future.

CHAPTER THREE

FIELD PROGRAMMABLE GATE ARRAY

3.1 Introduction

Prompted by the development of new types of sophisticated field-programmable devices (FPDs), the process of designing digital hardware has changed dramatically over the past few years. Unlike previous generations of technology, in which board-level designs included large number of SSI chips containing basic gates, virtually every digital design produced today consists mostly of high-density devices. This applies not only to custom devices like processors and memory, but also for logic circuits such as state machine controllers, counters, registers, and decoders. When such circuits are destined for high-volume systems they have been integrated into high-density gate arrays. However, gate array NRE costs often are too expensive and gate arrays take too long to manufacture to be viable for prototyping or other low-volume scenarios. For these reasons, most prototypes, and also many production designs are now built using FPDs. The most compelling advantages of FPDs are instant manufacturing turnaround, low start-up costs, low financial risk and (since programming is done by the end user) ease of design changes. The market for FPDs has grown dramatically over the past decade to the point where there is now a wide assortment of devices to choose from. A designer today faces a daunting task to research the different types of chips, understand what they can best be used for, choose a particular manufacturer's product, learn the intricacies of vendor-specific software and then design the hardware. Confusion for designers is exacerbated by not only the sheer number of FPDs available, but also by the complexity of the more sophisticated devices. The emphasis is on devices with relatively high logic capacity; all of the most important commercial products are discussed. Before proceeding, we provide definitions of the terminology in this field. This is necessary because the technical jargon has become somewhat inconsistent over the

past few years as companies have attempted to compare and contrast their products in literature.

A field-programmable gate array (FPGA) is a semiconductor device that can be configured by the customer or designer after manufacturing—hence the name "field-programmable". FPGAs are programmed using a logic circuit diagram or a source code in a hardware description language (HDL) to specify how the chip will work. They can be used to implement any logical function that an application-specific integrated circuit (ASIC) could perform, but the ability to update the functionality after shipping offers advantages for many applications. (BETZ, 2000)

FPGAs contain programmable logic components called "logic blocks", and a hierarchy of reconfigurable interconnects that allow the blocks to be "wired together"—somewhat like a one-chip programmable breadboard. Logic blocks can be configured to perform complex combinational functions, or merely simple logic gates like AND and XOR. In most FPGAs, the logic blocks also include memory elements, which may be simple flip-flops or more complete blocks of memory.

The FPGA industry sprouted from programmable read only memory (PROM) and programmable logic devices (PLDs). PROMs and PLDs both had the option of being programmed in batches in a factory or in the field (field programmable), however programmable logic was hard-wired between logic gates.

3.2 Modern Developments

A recent trend has been to take the coarse-grained architectural approach a step further by combining the logic blocks and interconnects of traditional FPGAs with embedded microprocessors and related peripherals to form a complete "system on a programmable chip". This work mirrors the architecture by Ron Perlof and Hana Potash of Burroughs Advanced Systems Group which combined a reconfigurable CPU architecture on a single chip called the SB24. That work was done in 1982. Examples of such hybrid technologies can be found in the Xilinx Virtex-II PRO and Virtex-4 devices, which include one or more PowerPC processors embedded within

the FPGA's logic fabric. The Atmel FPSLIC is another such device, which uses an AVR processor in combination with Atmel's programmable logic architecture.

An alternate approach to using hard-macro processors is to make use of "soft" processor cores that are implemented within the FPGA logic. As previously mentioned, many modern FPGAs have the ability to be reprogrammed at "run time," and this is leading to the idea of reconfigurable computing or reconfigurable systems — CPUs that reconfigure themselves to suit the task at hand. The Mitrion Virtual Processor from Mitrionics is an example of a reconfigurable soft processor, implemented on FPGAs. However, it does not support dynamic reconfiguration at runtime, but instead adapts itself to a specific program.

Additionally, new, non-FPGA architectures are beginning to emerge. Software-configurable microprocessors such as the Stretch S5000 adopt a hybrid approach by providing an array of processor cores and FPGA-like programmable cores on the same chip.

3.2.1 Gates

- 1987: 9,000 gates, Xilinx
- 1992: 600,000, Naval Surface Warfare Department
- Early 2000s: Millions

3.2.2 Market Size

- 1985: First commercial FPGA technology invented by Xilinx
- 1987: $14 million
- ~1993: >$385 million
- 2005: $1.9 billion
- 2010 estimates: $2.75 billion

3.2.3 FPGA Design

- 10,000
- 2005: 80,000
- 2008:90,000
- 2010 estimates: 110,000 (Hewlett-Packard Co., 2001)

3.3 FPGA Comparisons

Historically, FPGAs have been slower, less energy efficient and generally achieved less functionality than their fixed ASIC counterparts. A combination of volume, fabrication improvements, research and development, and the I/O capabilities of new supercomputers have largely closed the performance gap between ASICs and FPGAs.

Advantages include a shorter time to market, ability to re-program in the field to fix bugs, and lower non-recurring engineering costs. Vendors can also take a middle road by developing their hardware on ordinary FPGAs, but manufacture their final version so it can no longer be modified after the design has been committed.

Xilinx claims that several market and technology dynamics are changing the ASIC/FPGA paradigm:

- IC costs are rising aggressively
- ASIC complexity has bolstered development time and costs
- R&D resources and headcount is decreasing
- Revenue losses for slow time-to-market are increasing
- Financial constraints in a poor economy are driving low-cost technologies

These trends make FPGAs a better alternative than ASICs for a growing number of higher-volume applications than they have been historically used for, to which the company attributes the growing number of FPGA design starts.

The primary differences between CPLDs and FPGAs are architectural. A CPLD has a somewhat restrictive structure consisting of one or more programmable sum-

of-products logic arrays feeding a relatively small number of clocked registers. The result of this is less flexibility, with the advantage of more predictable timing delays and a higher logic-to-interconnect ratio. The FPGA architectures, on the other hand, are dominated by interconnect. This makes them far more flexible (in terms of the range of designs that are practical for implementation within them) but also far more complex to design for.

Another notable difference between CPLDs and FPGAs are the presence in most FPGAs of higher-level embedded functions (such as adders and multipliers) and embedded memories, as well as to have logic blocks implement decoders or mathematical functions.

Some FPGAs have the capability of partial re-configuration that lets one portion of the device be re-programmed while other portions continue running.

3.4 FPGA Architecture

The most common FPGA architecture consists of an array of configurable logic blocks (CLBs), I/O pads, and routing channels. Generally, all the routing channels have the same width (number of wires). Multiple I/O pads may fit into the height of one row or the width of one column in the array.

An application circuit must be mapped into an FPGA with adequate resources. While the number of CLBs and I/Os required is easily determined from the design, the number of routing tracks needed may vary considerably even among designs with the same amount of logic. (For example, a crossbar switch requires much more routing than a systolic array with the same gate count.) Since unused routing tracks increase the cost (and decrease the performance) of the part without providing any benefit, FPGA manufacturers try to provide just enough tracks so that most designs that will fit in terms of LUTs and IOs can be routed. This is determined by estimates such as those derived from Rent's rule or by experiments with existing designs.

A classic FPGA logic block consists of a 4-input lookup table (LUT), and a flip-flop, as shown at Figure 3.1. In recent years, manufacturers have started moving to 6-input LUTs in their high performance parts, claiming increased performance.

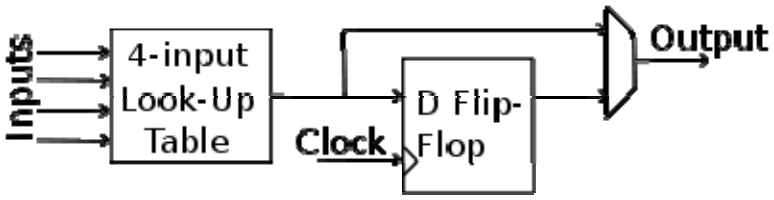


Figure 3.1 Typical logic block (BETZ, 2000)

There is only one output, which can be either the registered or the unregistered LUT output. The logic block has four inputs for the LUT and a clock input. Since clock signals (and often other high-fanout signals) are normally routed via special-purpose dedicated routing networks in commercial FPGAs, they and other signals are separately managed.

For this example architecture, the locations of the FPGA logic block pins are shown below at Figure 3.2.

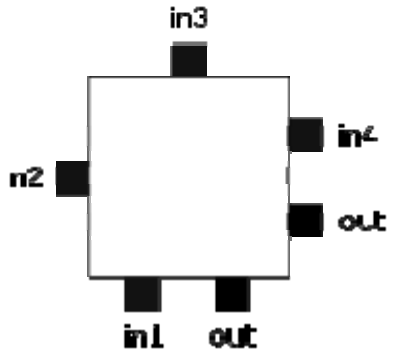


Figure 3.2 Logic Block Pin Locations (BETZ, 2000)

Each input is accessible from one side of the logic block, while the output pin can connect to routing wires in both the channel to the right and the channel below the logic block.

Each logic block output pin can connect to any of the wiring segments in the channels adjacent to it.

Similarly, an I/O pad can connect to any one of the wiring segments in the channel adjacent to it. For example, an I/O pad at the top of the chip can connect to

any of the W wires (where W is the channel width) in the horizontal channel immediately below it.

Generally, the FPGA routing is unsegmented. That is, each wiring segment span only one logic block before it terminates in a switch box. By turning on some of the programmable switches within a switch box, longer paths can be constructed. For higher speed interconnect, some FPGA architectures use longer routing lines that span multiple logic blocks.

Whenever a vertical and a horizontal channel intersect, there is a switch box. In this architecture, when a wire enters a switch box, there are three programmable switches that allow it to connect to three other wires in adjacent channel segments. The pattern, or topology, of switches used in this architecture is the planar or domain-based switch box topology and can be seen in Figure 3.3. In this switch box topology, a wire in track number one connects only to wires in track number one in adjacent channel segments, wires in track number 2 connect only to other wires in track number 2 and so on. The figure below illustrates the connections in a switch box.

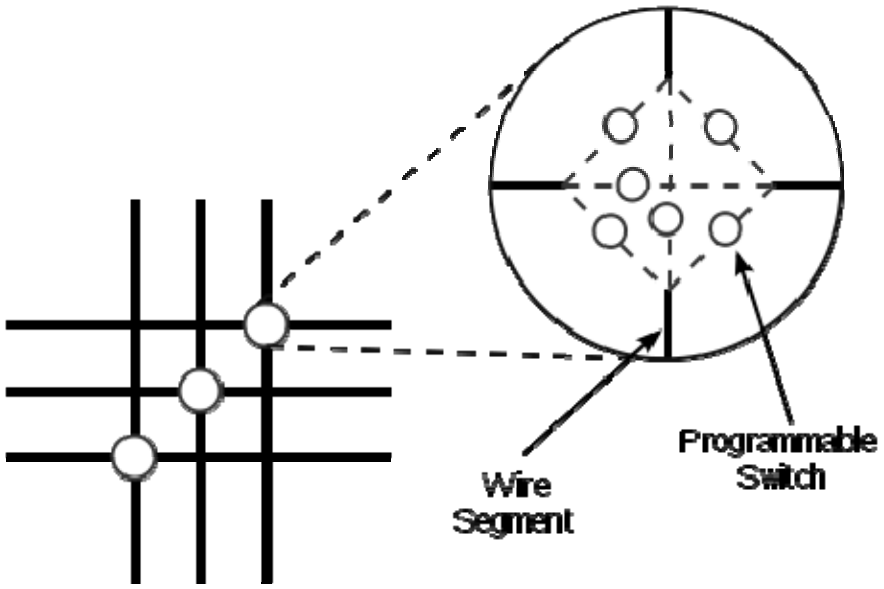


Figure 3.3 Switch box topology (BETZ, 2000)

Modern FPGA families expand upon the above capabilities to include higher level functionality fixed into the silicon. Having these common functions embedded into

the silicon reduces the area required and gives those functions increased speed compared to building them from primitives. Examples of these include multipliers, generic DSP blocks, embedded processors, high speed IO logic and embedded memories.

FPGAs are also widely used for systems validation including pre-silicon validation, post-silicon validation, and firmware development. This allows chip companies to validate their design before the chip is produced in the factory, reducing the time to market.

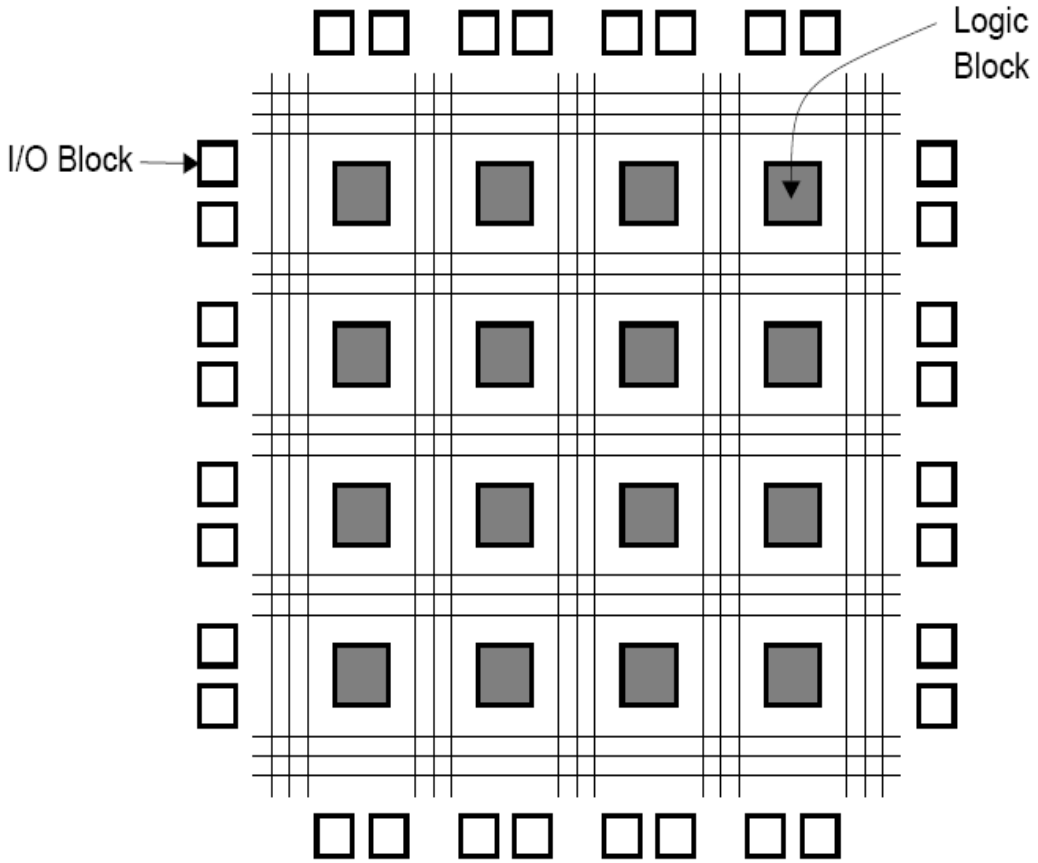


Figure 4.4 Structure of FPGA (BETZ, 2000)

4.4 FPGA Design and Programming

To define the behavior of the FPGA, the user provides a hardware description language (HDL) or a schematic design. The HDL form might be easier to work with when handling large structures because it's possible to just specify them numerically rather than having to draw every piece by hand. On the other hand, schematic entry can allow for easier visualization of a design.

Then, using an electronic design automation tool, a technology-mapped netlist is generated. The netlist can then be fitted to the actual FPGA architecture using a process called place-and-route, usually performed by the FPGA company's proprietary place-and-route software. The user will validate the map, place and route results via timing analysis, simulation, and other verification methodologies. Once the design and validation process is complete, the binary file generated (also using the FPGA company's proprietary software) is used to (re)configure the FPGA.

The source files are fed to a software suite from the FPGA/CPLD vendor that through different steps will produce a file. This file is then transferred to the FPGA/CPLD via a serial interface (JTAG) or to an external memory device like an EEPROM.

The most common HDLs are VHDL and Verilog, although in an attempt to reduce the complexity of designing in HDLs, which have been compared to the equivalent of assembly languages, there are moves to raise the abstraction level through the introduction of alternative languages.

To simplify the design of complex systems in FPGAs, there exist libraries of predefined complex functions and circuits that have been tested and optimized to speed up the design process. These predefined circuits are commonly called *IP cores*, and are available from FPGA vendors and third-party IP suppliers (rarely free, and typically released under proprietary licenses). Other predefined circuits are available from developer communities such as OpenCores (typically *free*, and released under the GPL, BSD or similar license), and other sources. (Hewlett-Packard Co., 2001)

In a typical design flow, an FPGA application developer will simulate the design at multiple stages throughout the design process. Initially the RTL description in VHDL or Verilog is simulated by creating test benches to simulate the system and observe results. Then, after the synthesis engine has mapped the design to a netlist, the netlist is translated to a gate level description where simulation is repeated to confirm the synthesis proceeded without errors. Finally the design is laid out in the FPGA at which point propagation delays can be added and the simulation run again with these values back-annotated onto the netlist.

4.5 Which FPGA is Chosen For This Project

For image processing applications, generally DSP FPGA chips are used. They have a lot of differential I/O pins and much more gates than other FPGA chipsets. This project is similar to image processing application so a DSP FPGA is chosen. Spartan 3A DSP1800A video starter kit is used. See Appendix K for datasheet.

CHAPTER FOUR

LOCAL DIMMING APPLICATION

4.1 Technical Information

4.1.1 LED Backlight Unit and Its Types

4.1.1.1 LED Overview

LEDs are the fastest growing backlight technology on the market today. They provide many benefits as a backlight source for LCDs including reasonably good efficiency, a wider range of color reproduction, enhanced contrast ratio (due to the option of arbitrarily scaling/dimming individual display areas), low voltage operation, mercury-free construction, good thermal dissipation properties and high luminance.

Many manufacturers have designed very large LCD-TV products utilizing red, green and blue (RGB) LEDs for the backlight and have achieved good performance. However, RGB LED backlights demand color mixing technology in order to overcome unevenness of luminance. Color mixing has significantly improved with an increased understanding of the design and function of direct backlight concept. Today, RGB LED clusters (usually 1x red, 2x green, and 1x blue) are grouped in matrices with some space provided between clusters to facilitate good color mixing and to minimize the need for design of thermal radiation structures. Another critical factor to consider in LED backlight design is the need for control of system temperature, as this is essential in order to avoid color shift, which is another challenge in LED backlight systems. Many new backlights are being designed utilizing white LED technology.

An LED is a semiconductor device that creates light using solid-state electronics. A diode is composed of a layer of electron rich material separated by a layer of electron deficient material which forms a junction. Power applied to this junction excites the electrons in the electron rich material leading to photon emission and the

creation of light. Depending on the chemical composition of the semiconductor layers, the color of light emission will vary.

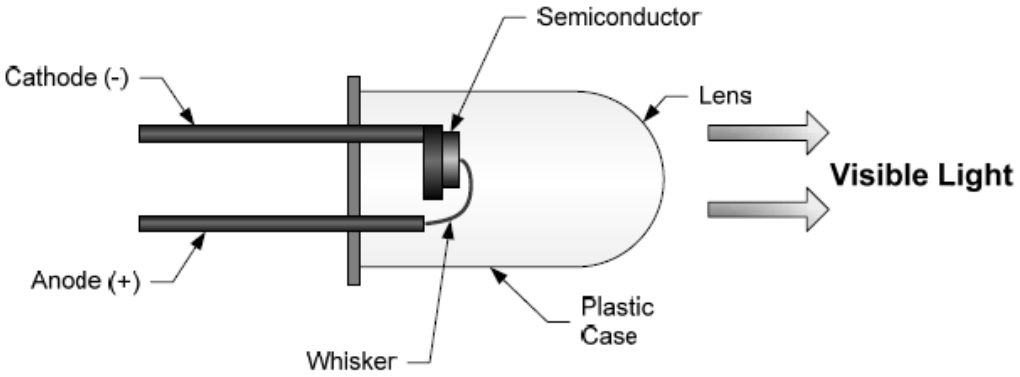


Figure 4.1 LED Construction

For outdoor applications, high bright backlights are constructed as a matrix of LEDs covered by a set of filters to diffuse and balance the light across the entire surface of the LCD. A typical LED backlight matrix is shown in the Figure 4.2.

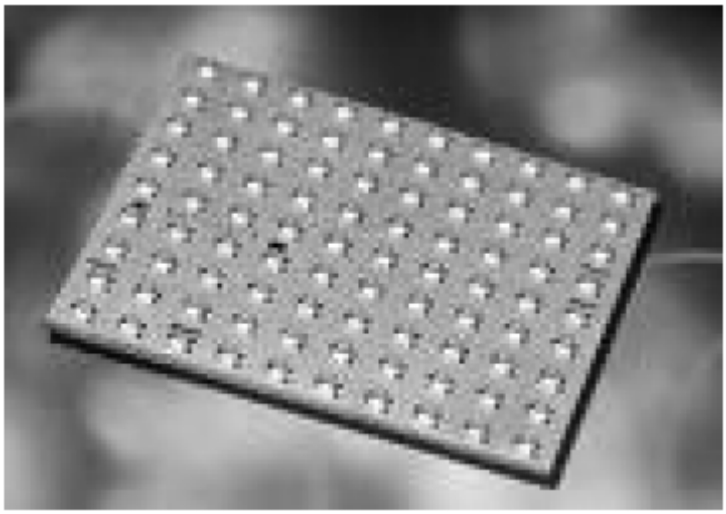


Figure 4.2 Typical LED matrix backlight

4.1.2 Contrast Ratio

The contrast ratio is a measure of a display system, defined as the ratio of the luminance of the brightest color (white) to that of the darkest color (black) that the system is capable of producing. A high contrast ratio is a desired aspect of any display, but with the various methods of measurement for a system or its part, remarkably different measured values can sometimes produce similar results.

Contrast ratio ratings provided by different manufacturers of display devices are not necessarily comparable to each other due to differences in method of measurement, operation, and unstated variables. Manufacturers have traditionally favored measurement methods that isolate the device from the system, whereas other designers have more often taken the effect of the room into account. An ideal room would absorb all the light reflecting from a projection screen or emitted by a CRT, and the only light seen in the room would come from the display device. With such a room, the contrast ratio of the image would be the same as the device. Real rooms reflect some of the light back to the displayed image, lowering the contrast ratio seen in the image.

Moving from a system that displays a static motionless image to a system that displays a dynamic, changing picture slightly complicates the definition of the contrast ratio, because of the need to take into account the extra temporal dimension to the measuring process. Thus the ratio of the luminosity of the brightest and the darkest color the system is capable of producing simultaneously at any instant of time is called static contrast ratio, while the ratio of the luminosity of the brightest and the darkest color the system is capable of producing over time is called dynamic contrast ratio. Demonstration of brightness perception can be seen at Figure 4.3.

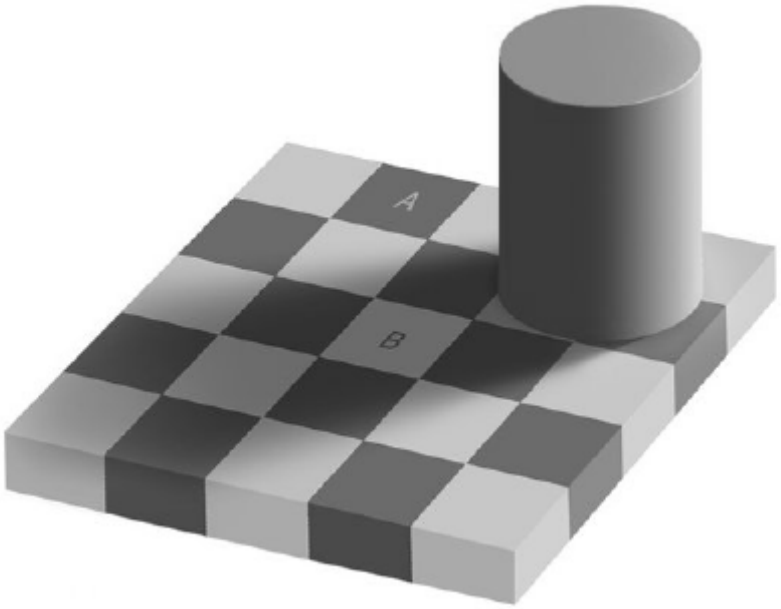


Figure 4.3 Demonstration of brightness perception

4.1.2.1 Methods of Contrast Ratio Measurements

Many display devices favor the use of the *full on/full off* method of measurement, as it cancels out the effect of the room and results in an ideal ratio. Equal proportions of light reflect from the display to the room and back in both "black" and "white" measurements, as long as the room stays the same. This will inflate the light levels of both measurements proportionally, leaving the black to white luminance ratio unaffected.

Some manufacturers have gone as far as using different device parameters for the three tests, even further inflating the calculated contrast ratio. With DLP projectors, one method to do this is to enable the clear sector of the color filter wheel for the *"on"* part and disable it for the *"off"* part. This practice is rather dubious, as it will be impossible to reproduce such contrast ratios with any useful image content.

Another measure is the *ANSI contrast*, in which the measurement is done with a checker board patterned test image where the luminosity values are measured

simultaneously. This is a more realistic measure of system capability, but contains the potential of including the effects of the room into the measurement, if the test is not performed in a room that is close to ideal.

It is useful to note that the *full on/full off* method effectively measures the dynamic contrast ratio of a display, while the *ANSI contrast* measures the static contrast ratio. Demonstration of perception of light and dark is shown at Figure 4.4.

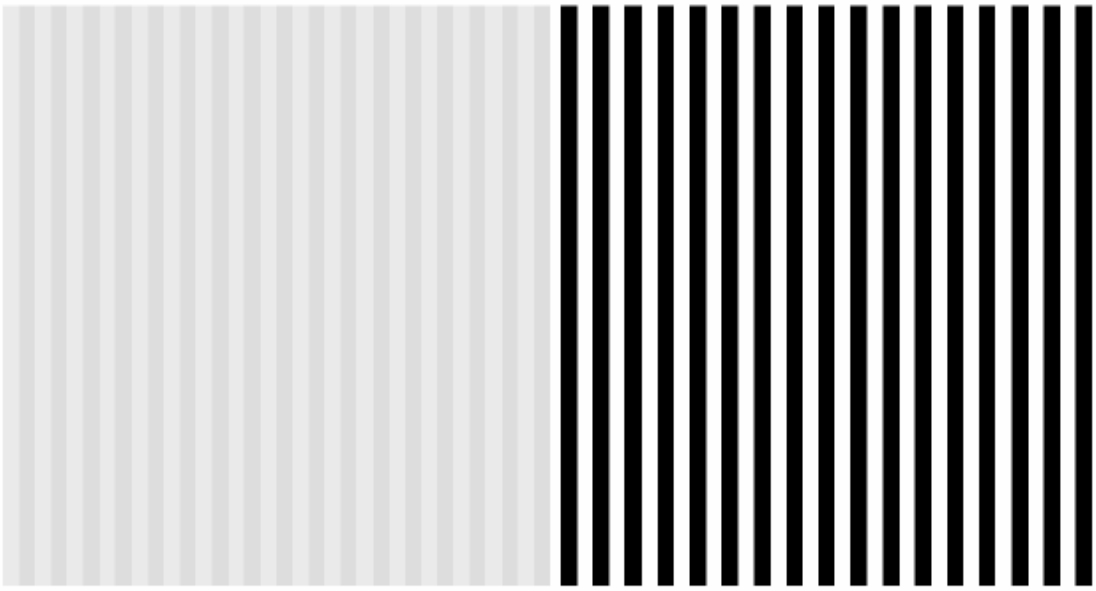


Figure 4.4 Demonstration of perception of light and dark

4.1.2.2 Dynamic Contrast Ratio

A notable recent development in the LCD technology is the so-called "dynamic contrast" (DC). When there is a need to display a dark image, the display would under-power the backlight lamp (or decrease the aperture of the projector's lens using an iris), but will proportionately amplify the transmission through the LCD panel. This gives the benefit of realizing the potential static contrast ratio of the LCD panel in dark scenes when the image is watched in a dark room. The drawback is that if a dark scene does contain small areas of super-bright light, image quality may be over exposed.

The trick for the display is to determine how much of the highlights may be unnoticeably blown out in a given image under the given ambient lighting conditions.

Brightness, as it is most often used in marketing literature, refers to the emitted luminous intensity on screen measured in candela per square meter (cd/m^2). The higher the number means the brighter the screen.

It is also common to market only the dynamic contrast ratio capability of a display (when it is better than its static contrast ratio), which should not be directly compared to the static contrast ratio. A plasma display with a static 5000:1 contrast ratio will show superior contrast to an LCD with 5000:1 dynamic and 1000:1 static contrast ratio when the input signal contains a full range of brightness from 0 to 100% simultaneously. They will, however, be on-par when input signal ranges only from 0 to 20% brightness.

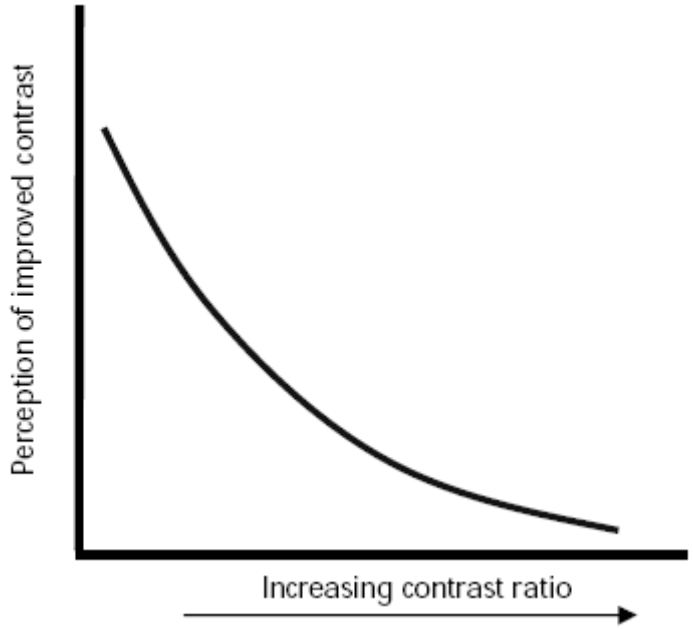


Figure 4.5 Perception of contrast ratio (Hewlett-Packard Co.)

As the numeric contrast ratio increases, the *perception* of continued contrast improvement declines. Somewhere above a 1,000:1 or so, further improvements in

the absolute, numeric ratio will be virtually unperceivable to the average viewer under any conditions.

4.2 Software Design

4.2.1 Definition of the Design Method

Local dimming algorithm has same structure on academic studies and commercial products so far, as shown at Figure 4.6. For this reason, local dimming control algorithm implemented to TV via this principle in this thesis. Sub blocks have been explained below, at Figure 4.6.

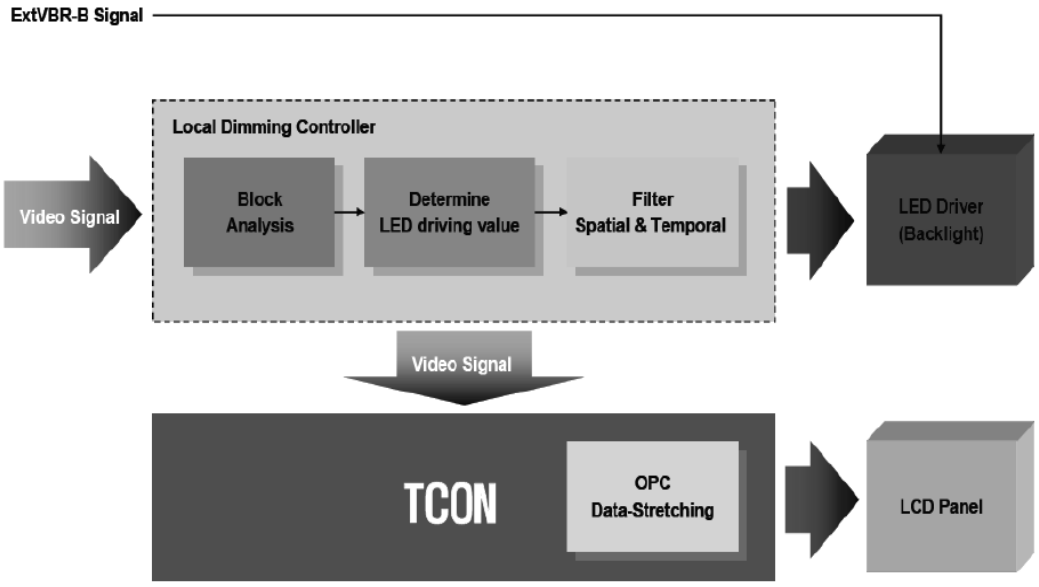


Figure 4.6 Block diagram of algorithm

4.2.1.1 Video Signal

For using the algorithm on all TV sets, Low Voltage Differential Signals (LVDS) have been chosen as input video signals. LVDS signals carry all information of pixels by differential way to Timer Controller part of panels. Timer Controller part converts LVDS signals to Transistor Transistor Logic signals and drives the all pixels. LVDS bit size must be adjusted according to the panel. 6-bit, 8-bit or 10-bit

panels are available panel market. This bit numbers refer to pixel resolution of panels, in other words the bit numbers of red, green and blue component of pixels. Panel resolution and refresh rate are determinant on structure of LVDS. LVDS can have 1 data channel up to 4 data channels and channels contain 4 or 5 data pairs. General full HD 100Hz panels have 4 channels and channels have 5 pairs. LED backlight panel that will be used on this thesis has 4 data channels and each channel has five data pairs. Detailed information of LVDS signals and data pairs can be found in datasheets of panels at Appendix M and Appendix L.

4.2.1.2 Block Analysis

Algorithm converts LVDS signals to 10-bit red, 10-bit green and 10-bit blue data. LVDS to RGB conversion is the first step of backlight data determination. Clock frequency of LVDS signals is 75MHz and 7 bits data is transported every clock period. De-serialization of LVDS pairs, FPGA works at 262,5MHz. There is a limitation at working frequency of FPGA at 525MHz. Data processing is similar to DDR. Signals process both negative and positive edge. Block analysis part contains de-serialization and grouping the pixels according to the backlight resolution.

B(1)	B(2)	B(3)	B(4)	B(5)	B(6)	B(7)	B(8)
B(9)	B(10)	B(11)	B(12)	B(13)	B(14)	B(15)	B(16)
B(17)	B(18)	B(19)	B(20)	B(21)	B(22)	B(23)	B(24)
B(25)	B(26)	B(27)	B(28)	B(29)	B(30)	B(31)	B(32)
B(33)	B(34)	B(35)	B(36)	B(37)	B(38)	B(39)	B(40)
B(41)	B(42)	B(43)	B(44)	B(45)	B(46)	B(47)	B(48)
B(49)	B(50)	B(51)	B(52)	B(53)	B(54)	B(55)	B(56)
B(57)	B(58)	B(59)	B(60)	B(61)	B(62)	B(63)	B(64)

Figure 4.7 The Backlight blocks location of LG panels

The panel used in this thesis has 64 blocks. It has 8x8 matrix structure. Considering the panel resolution, each block consists of 240x135 pixels.

The luminance information of pixel formulates based on R, G and B. Common approach for luminance information of pixel is found by calculating maximum of R, G, B. With a little tolerance, the maximum of R, G, B signals is approximate luminance value. Using maximum (R, G, B) method simplifies the implementation and saves FPGA capacity. Maximum (R, G, B) consist of 10-bit data, moreover panel backlight control unit needs 8-bit value for each block. So the least significant 2 bit will not be considered.

After de-serialization part, the luminance values of each pixel are obtained. It is not efficient to store all image pixel data in FPGA, because of this reason, de-serialized LVDS data should be serialized in this part.

Only the luminance values are stored in memory. Serialized LVDS pairs routed to the timer-controller board of panel.

The algorithm does not improve the original image however image data is not changed. Improvement is limited with backlight part by the way whole image becomes better. The application does not need as much memory as image processing algorithms do.

4.2.1.3 Determine LED Block Driving Value

In block analysis part, luminance value of each pixels were stored in maximum of R, G, B. In that part of algorithm, the value of backlight blocks will be calculated. The average values of pixels for each block represent the LED driving value. LED driving value is between 0 and 255. In contradiction to CCFL backlight panels, LED backlight panels can be fully off. If the block is driven with “0”, block is completely shut down.

Another characteristic parameter for panels is intensity of light. Panels have around 500 candela luminance per square meter. Using LED driving values will

decrease the average intensity of light. Avoiding decreasing luminance, there must be a look up table for converting led driving values to optimized values. The look up table can be seen at Figure 4.8. This graphic is obtained from a panel manufacturer. But just graphic as taken, any explanation is not given for commercial concerns. According to the graphic, backlight blocks should not be closed, but in some TV modes like PC mode, this offset is adjusted lower value. When LED driving value over 80, backlight should be driven at maximum. This look up table concerns average intensity of light and contrast ratio of panel.

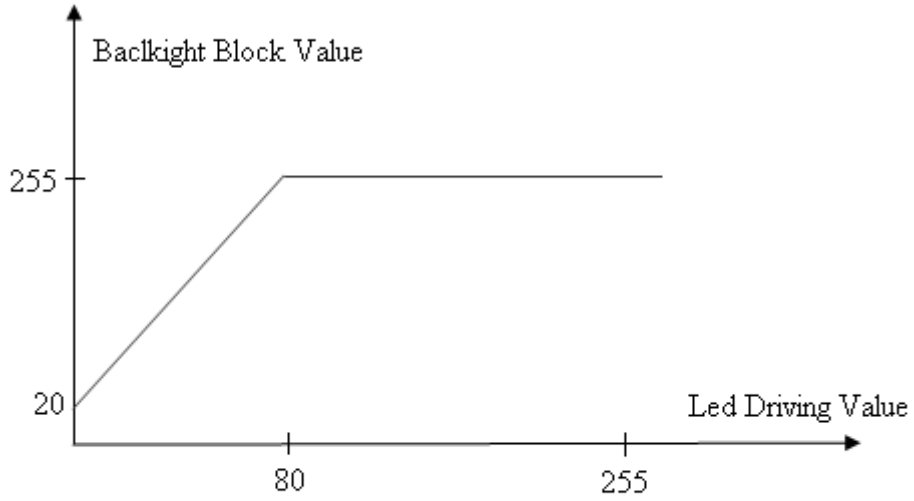
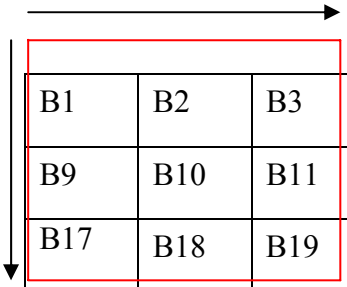


Figure 4.8 Look up table graphic for Led dimming value

Artifact of sending backlight controller “0” for block is flickering when this block is turned on. Avoiding on/off flicker effect always there must be an offset value.

4.2.1.4 Spatial Filtering

The LEDs in the blocks does not have uniform light propagation. Depend on manufacturers, seven or nine special type LEDs installed each block. Avoiding non-uniformity effect, spatial filter should be applied to the backlight block value. Spatial filter aims to decrease the difference between neighbor blocks. Spatial filter equals the value of each blocks in 3x3 area. The average value of 9 blocks is obtained as spatial filter output. The 3x3 frame applied to the 8x8 backlight matrix. Figure 4.9 shows the application of spatial filter.



B1	B2	B3	B4	B5	B6	B7	B8
B9	B10	B11	B12	B13	B14	B15	B16
B17	B18	B19	B20	B21	B22	B23	B24
B25	B26	B27	B28	B29	B30	B31	B32
B33	B34	B35	B36	B37	B38	B39	B40
B41	B42	B43	B44	B45	B46	B47	B48
B49	B50	B51	B52	B53	B54	B55	B56
B57	B58	B59	B60	B61	B62	B63	B64

Figure 4.9 Implementation of spatial filter

The new values of blocks in the 3x3 frame are calculated by the equation 4.1.

$$B_{sf\_out} = (B1+B2+B3+B9+B10+B11+B17+B18+B19) / 9 \qquad (4.1)$$

4.2.1.5 Temporal Filtering

LED Backlight units with local dimming algorithm have another effect called flicker effect. Refresh rate of the panel is 10 ms so the transition of frames is very fast. Difference of the black levels between two frames causes flickering. Temporal filter prevents the effect derived from the wide difference of black level between two frames.

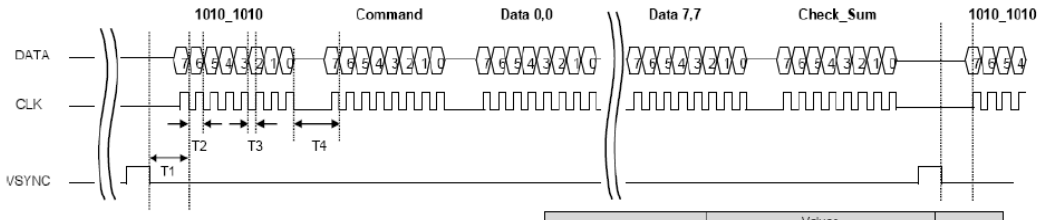
Temporal filter works on time domain and correlates between blocks data of two frames. The current data is calculated by the equation 4.2.

$$B_x(t) = [a.B_x(t-1) + b.B_x(t)] \qquad a+b = 1 \qquad (4.2)$$

Experimental results determine the coefficients a and b. Panel manufacturer fixes the value of a and b and shares it without explanation because of commercial concerns, a = 0.875 and b = 0.125.

Temporal filter is the last stage of data manipulating. After this filter, FPGA sends the filter output to the backlight controller of the panel.

4.2.1.6 Driving LED Blocks



Parameter	Values			Units
	Min	Typ	Max	
T1	9	10	TBD	us
T2	3	3.33	TBD	us
T3	1.5	1.65	TBD	us
T4	9	10	TBD	us

Figure 4.10 SPI timings of LG panel.

Backlight controller of panel is driven with Serial Peripheral Interface (SPI) signals. SPI contains three signals as seen on Figure 4.10. SPI sequence starts with

vertical synchronization (Vsync) pulse. Vsync should be sent from FPGA. Considering timing specifications are important. 3 μs high pulse generates the Vsync for panel. After that 6.66 μs delay must be generated. Serial binary 10101010 data synchronization data should be sent and the SPI clock frequency should be 30 KHz. 6.66 μs delay located between all 8-bit data packages. Panel needs checksum byte for error check which is generated by implementing XOR operations all 64 block data. Panel calculates checksum itself and compares with the coming from FPGA. If they are matched, backlight controller drives blocks, otherwise does not.

4.2.2 Algorithm

All algorithm schematics represent FPGA algorithms. Not only programming specifications are shown, but also electrical signals are represented at algorithm schematics.

4.2.2.1 Algorithm of De-serialization Block

The LVDS data transport data of pixels serially. In one period of clock, seven data is transported in all pairs. In this block this seven data are de-serialized. Inputs of this block are all differential pairs and outputs are seven bits parallel data. Steps of algorithm are shown at Figure 4.11.

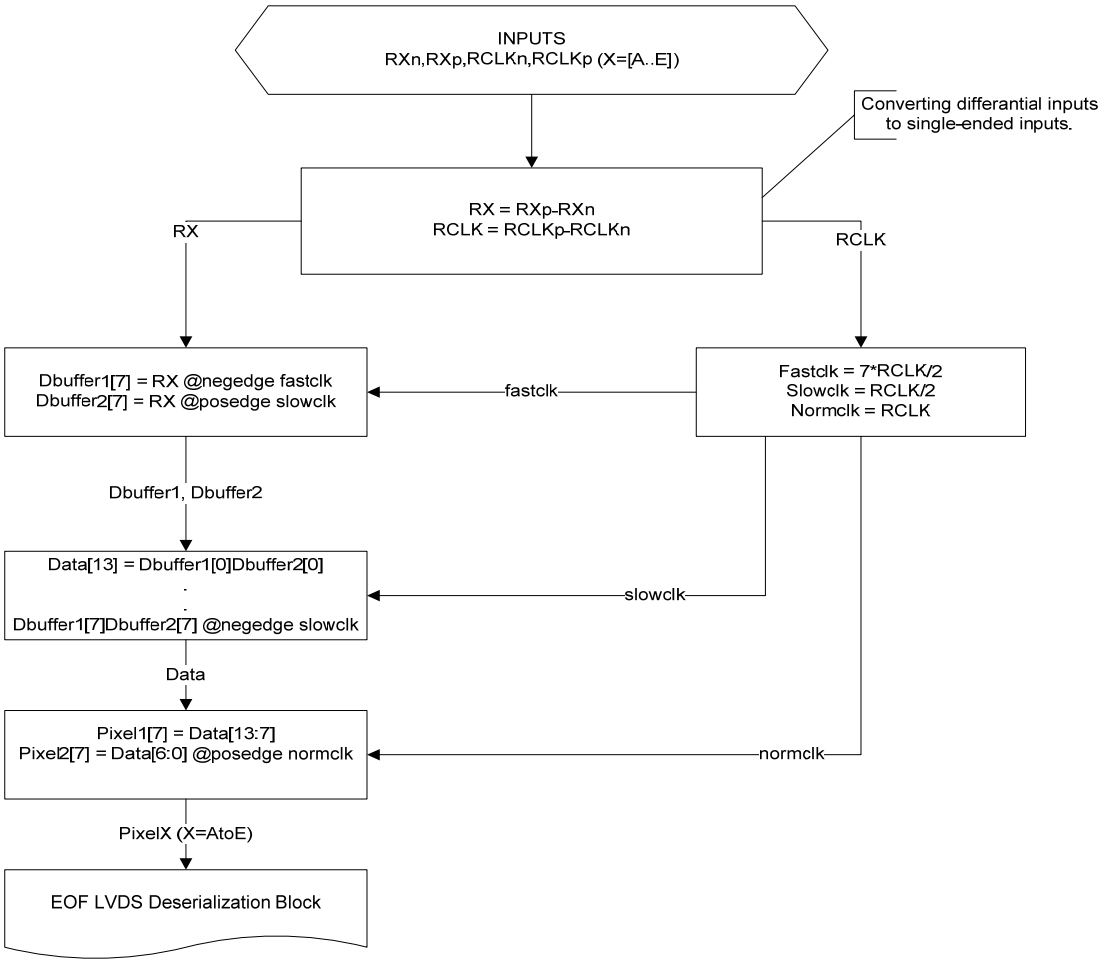


Figure 4.11 Steps of de-serialization algorithm

4.2.2.2 Algorithm of LVDS Mapping

LVDS mapping block is convert seven bits LVDS channel data to 10-bits R, G, B data of each pixel. After that for not capturing all the pixel data, only maximum of R, G and B is obtained. Then the most significant 8 bits of maximum data is directed to the output. Steps of algorithm are given at Figure 4.12.

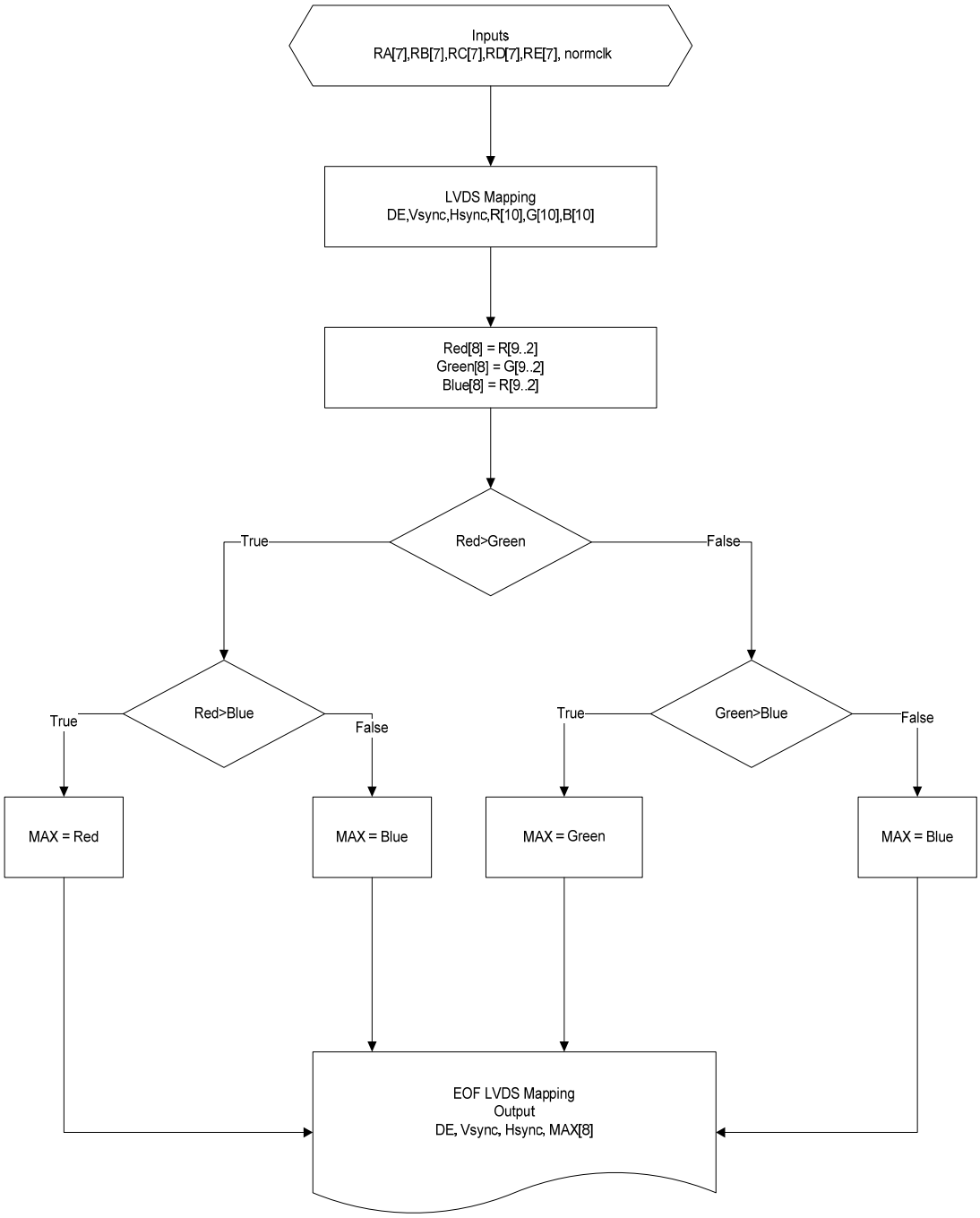


Figure 4.12 Steps of LVDS mapping algorithm.

4.2.2.3 Algorithm of Dimming Value Calculation Block

Inputs that coming from previous block are max(R, G, B) and sync signals. This part of algorithm calculates the data of each backlight block. Each block has 240 horizontal, 180 vertical pixels. Calculation is average value of all these pixels. Figure 4.13 shows the details of algorithm.

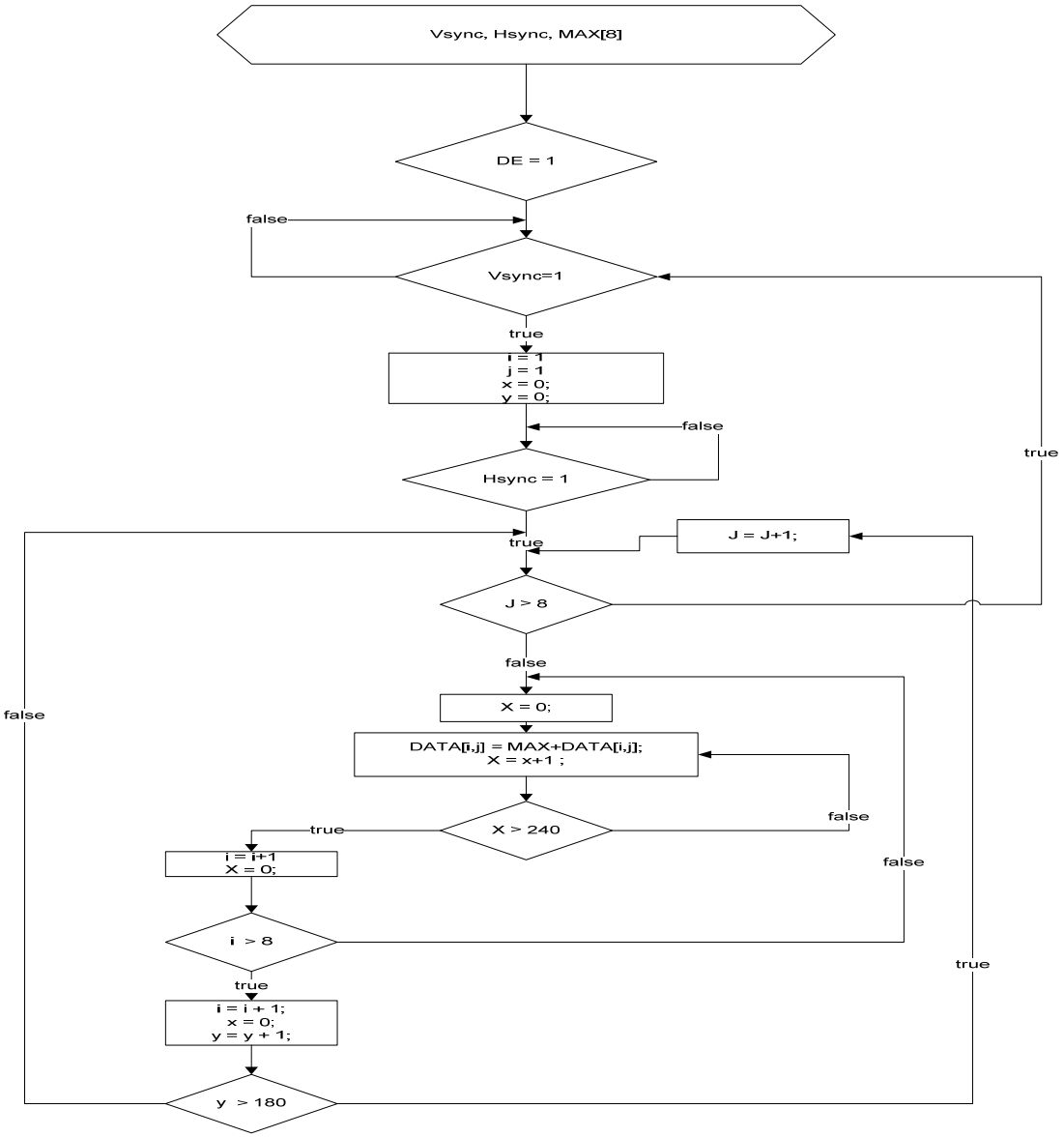


Figure 4.13 Algorithm diagram of dimming value calculation block

4.2.2.4 Algorithm of Data Mapping Block

There exists a 64 byte ram in previous block. This block converts each data according to the look up table. If the backlight data is smaller than 80, then new

value is 3 times of data. If data equals or is bigger than 80, then new value becomes 255. Figure 4.14 explains the details of algorithm.

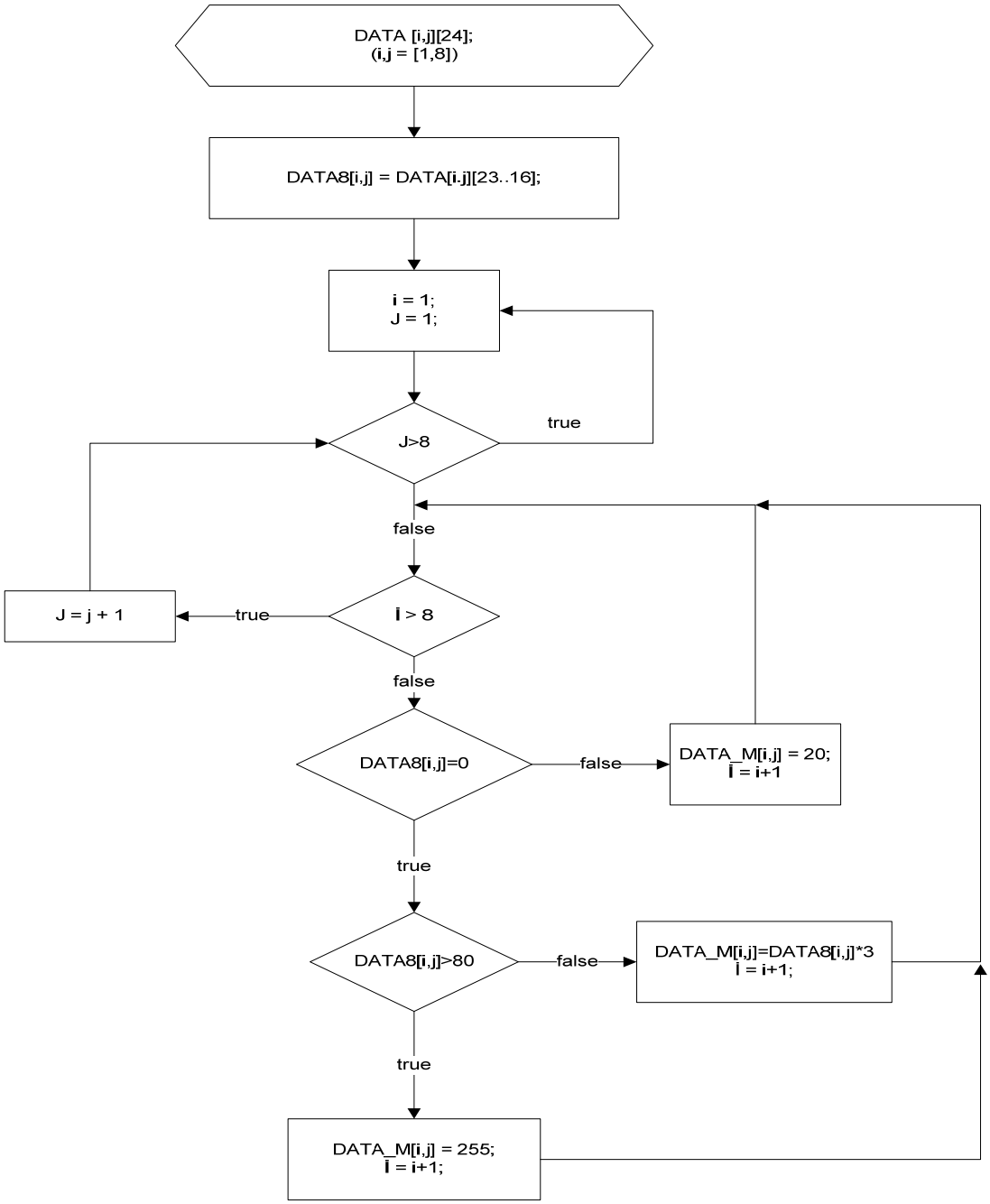


Figure 4.14 Detailed blocks of data mapping algorithm.

4.2.2.5 Algorithm of Spatial Filtering Block

Spatial filtering application is calculating average of neighbor 9 blocks. Used for avoiding non-uniformity effect. Figure 4.15 shows the blocks of spatial filtering.

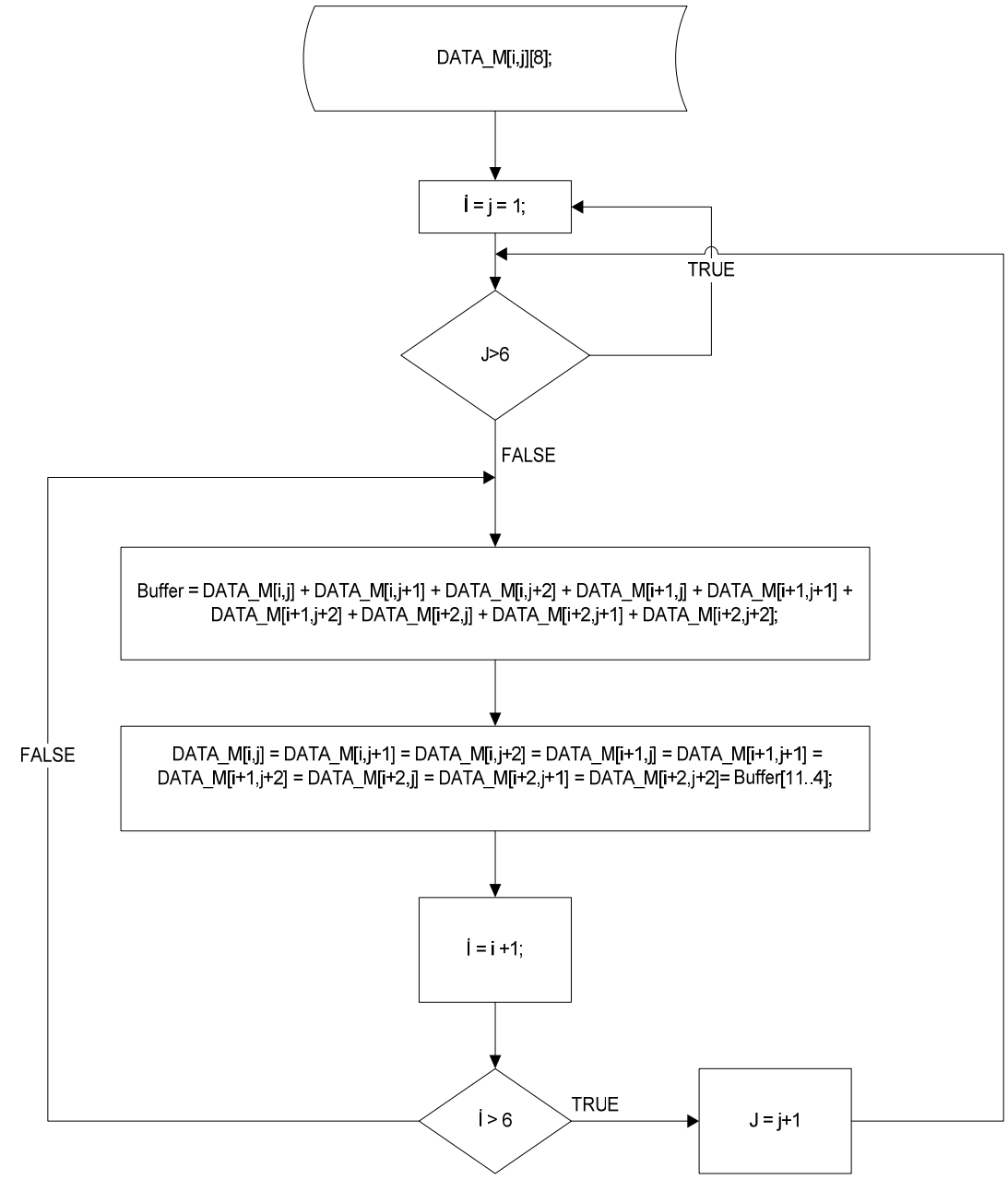


Figure 4.15 Spatial filtering blocks.

4.2.2.6 Algorithm of Temporal Filtering Block

Temporal filter is working on time domain. Previous backlight data are stored and processed with actual data. 0.875 times of previous data and 0,125 times of actual data are added and new value is produced. Figure 4.16 shows the blocks of algorithm.

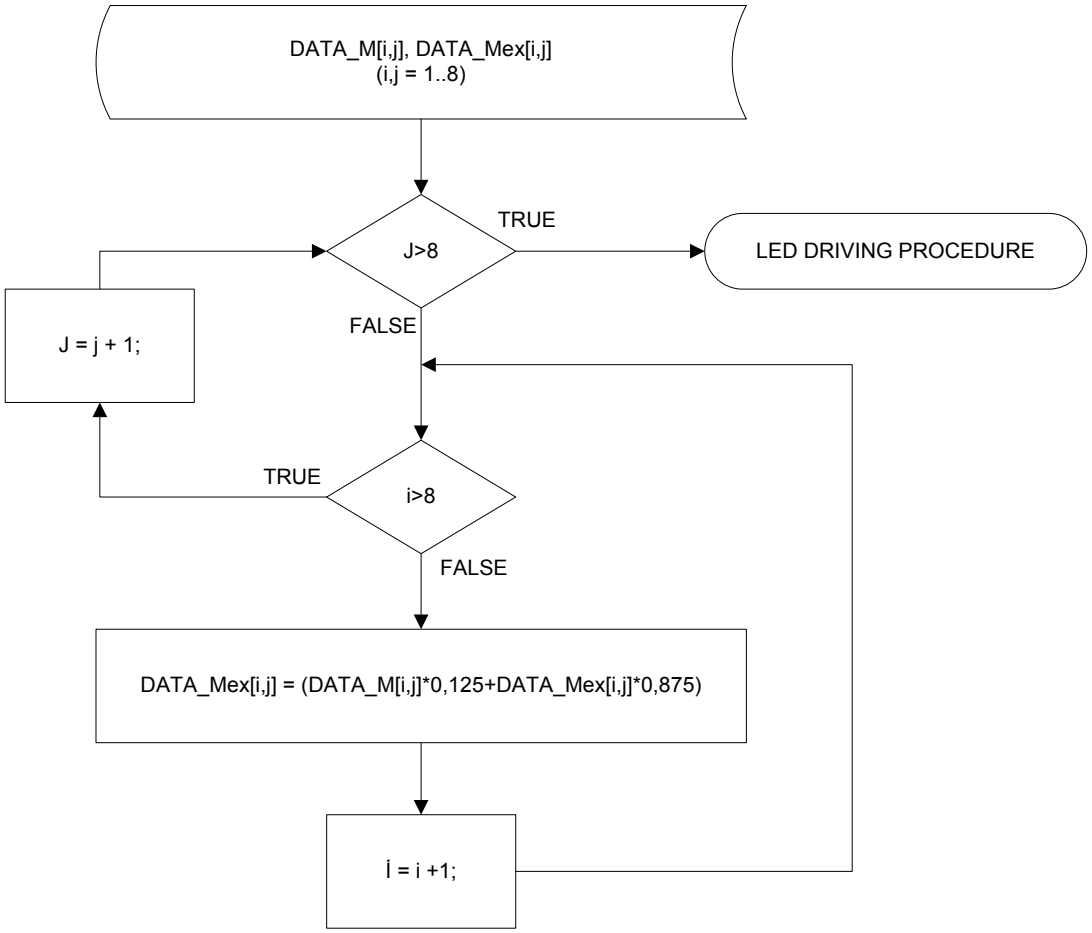


Figure 4.16 Temporal Filtering algorithm blocks.

4.2.2.7 Algorithm of SPI Data Generation Block

This step is the last step of algorithm. The data, which is calculated after temporal filter, is ready for sending to the backlight part. But backlight block has special interface for data. According to panel datasheet, the data is sent in SPI format. The blocks of algorithm can be seen at Figure 4.17.

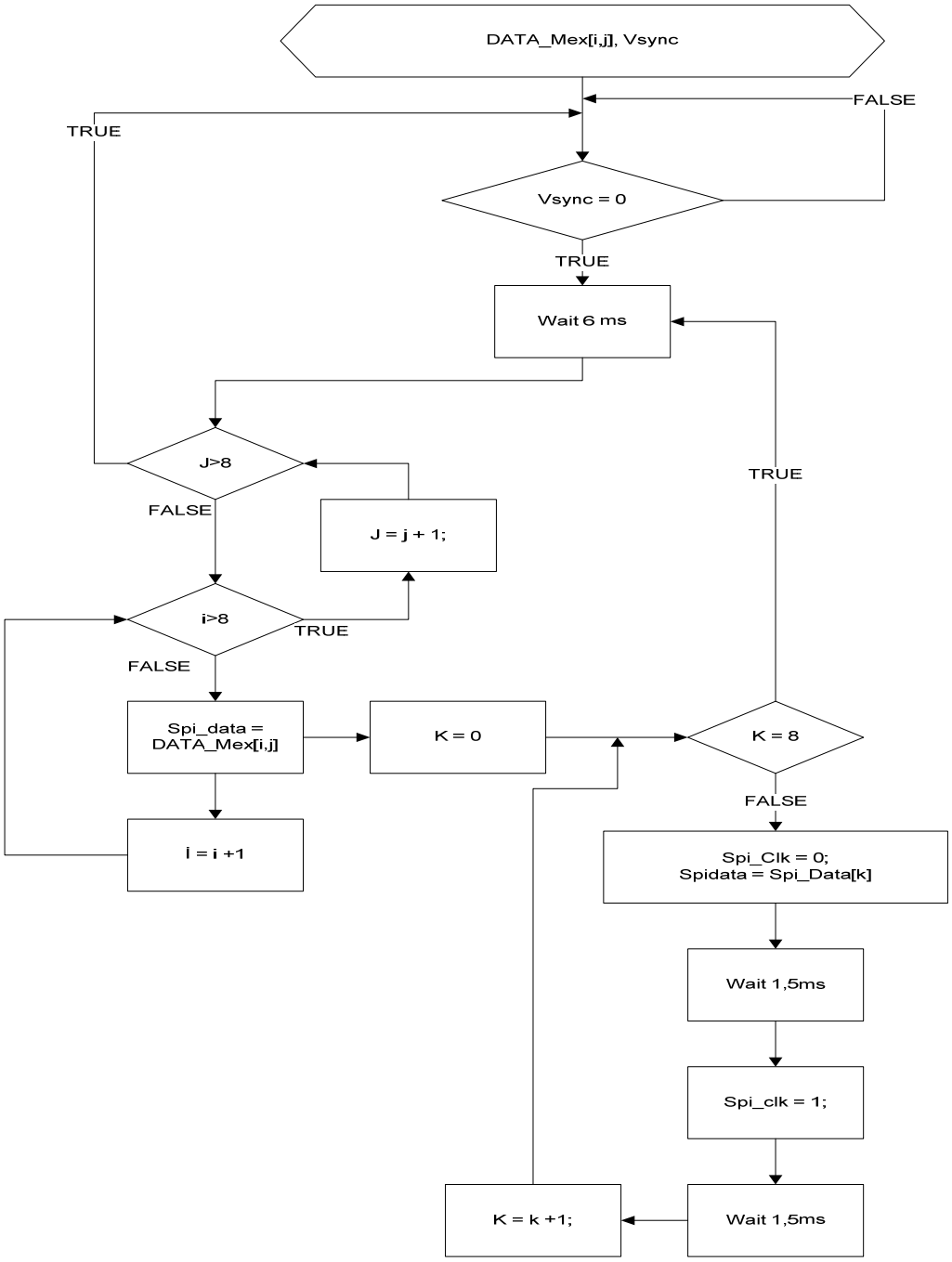


Figure 4.17 Steps of SPI data generation

4.2.3 Hardware Structure

The hardware blocks of this project are based on a full HD TV sets. Only an FPGA chip should be connected between LED backlight panel and chassis. The LVDS pins are tied up FPGA input ports. FPGA rehashes LVDS data and generates SPI data for dimming. Xilinx Spartan 3A DSP 1800A video kit is used as FPGA part. Vestel Electronics A.S. provides full HD chassis and panels. For commercial concerns, the detailed information can not be given about chassis.

The algorithm can easily be applied with image processing algorithms. The structure of algorithm and flexibility of FPGA allow designers to take part in their applications. This algorithm uses 600K gates of FPGA. Approximately 200K gates are used for de-serialization of LVDS data. All image processing algorithms already do this part. For this reason, image processing algorithms need extra 400K gates for dimming algorithm.

The Spartan-3A DSP Starter Platform provides the following features and block diagram of starter platform is shown in Figure 4.18.

- Xilinx 3SD1800A-FG676 FPGA
- Clocks
- 125 MHz LVTTL SMT Oscillator
- LVTTL Oscillator Socket
- 25.175 MHz LVTTL SMT Oscillator (Video clock)
- Memory
- 128M x 32-bit DDR2 SDRAM
- 16Mx8 Parallel / BPI Configuration Flash
- 64Mb SPI Configuration / Storage Flash (with 4 extra SPI selects)
- Interfaces
- 10/100/1000 PHY
- JTAG Programming/Configuration Port
- RS232 Port
- Low-cost VGA
- Buttons and switches

- 8 User LEDs
- 8-position User DIP Switch
- User Push Button Switches
- Reset Push Button Switch
- User I/O and expansion
- Digilent 6-pin header (2)
- EXP Expansion Connector (2)
- Configuration and Debug
- JTAG
- SystemACE™ Module Connector
- Eridon debug connector (SATA)

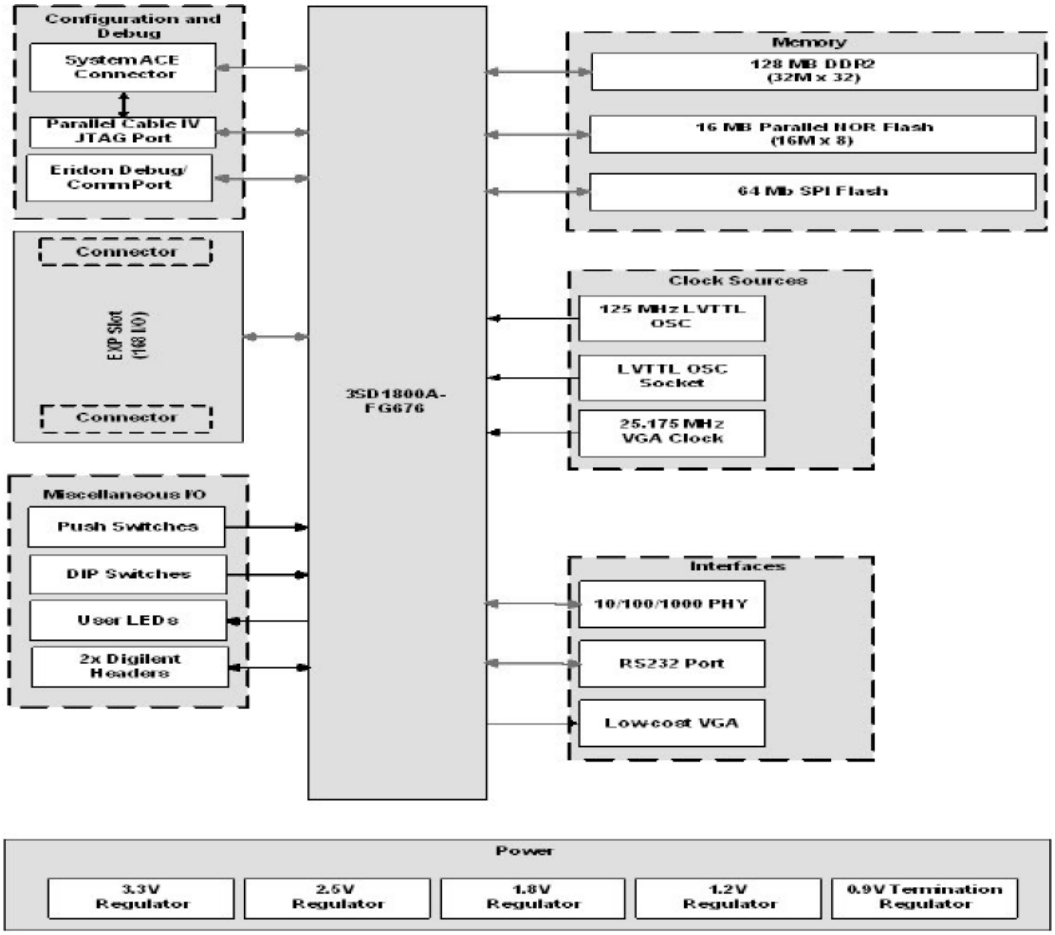


Figure 4.18 Block diagram of DSP Starter Platform

CHAPTER FIVE

RESULTS

FPGA algorithm that is designed in Chapter 4, is implemented to one of TV sets that can drive full HD 100Hz panels. LVDS output of TV sets wired to input pins of FPGA and outputs of FPGA are sent to the LG 42" full HD LED backlight 100Hz panel. Measurements are performed on three different set-ups. Figure 5.1 to Figure 5.5 are the patterns which are applied to LED backlight panel with local dimming, LED backlight panel without local dimming and CCFL backlight panel. Figure 5.6 is the backlight pattern of Figure 5.5, generated by local dimming algorithm.

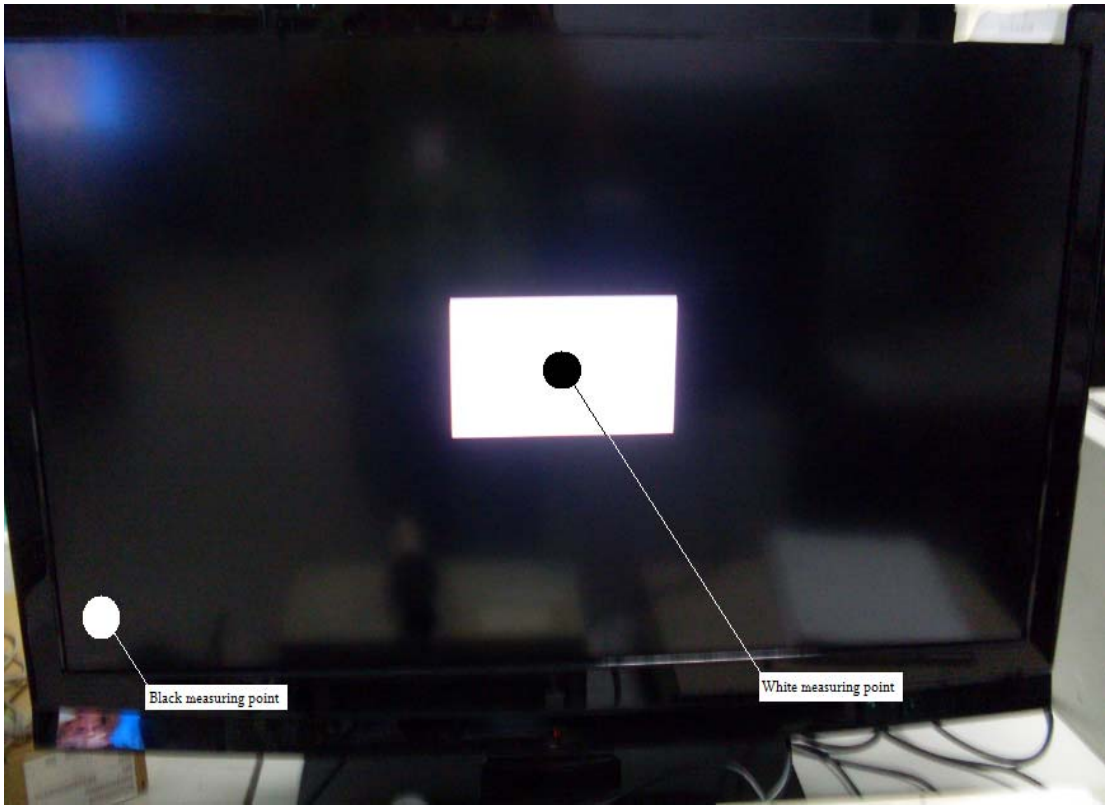


Figure 5.1 Pattern 1. (%20 white, centered)

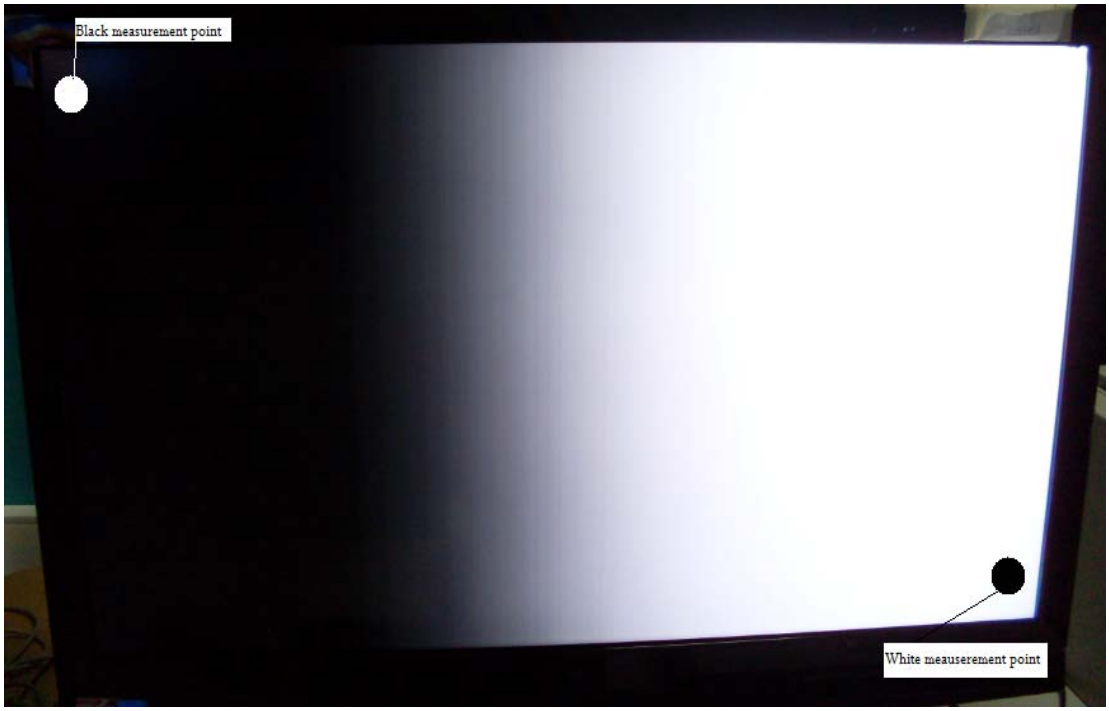


Figure 5.2 Pattern 2. (Gray scale)

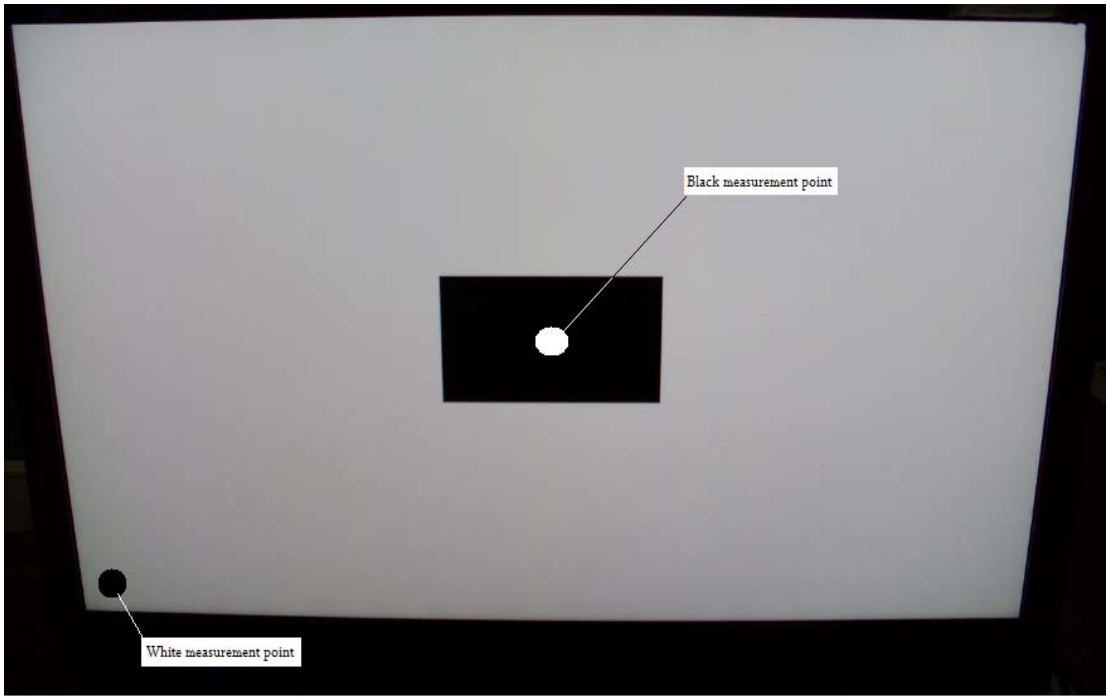


Figure 5.3 Pattern 3. (%20 black, centered)

Figure 5.4 Pattern 4. (%15 white, left-up aligned)

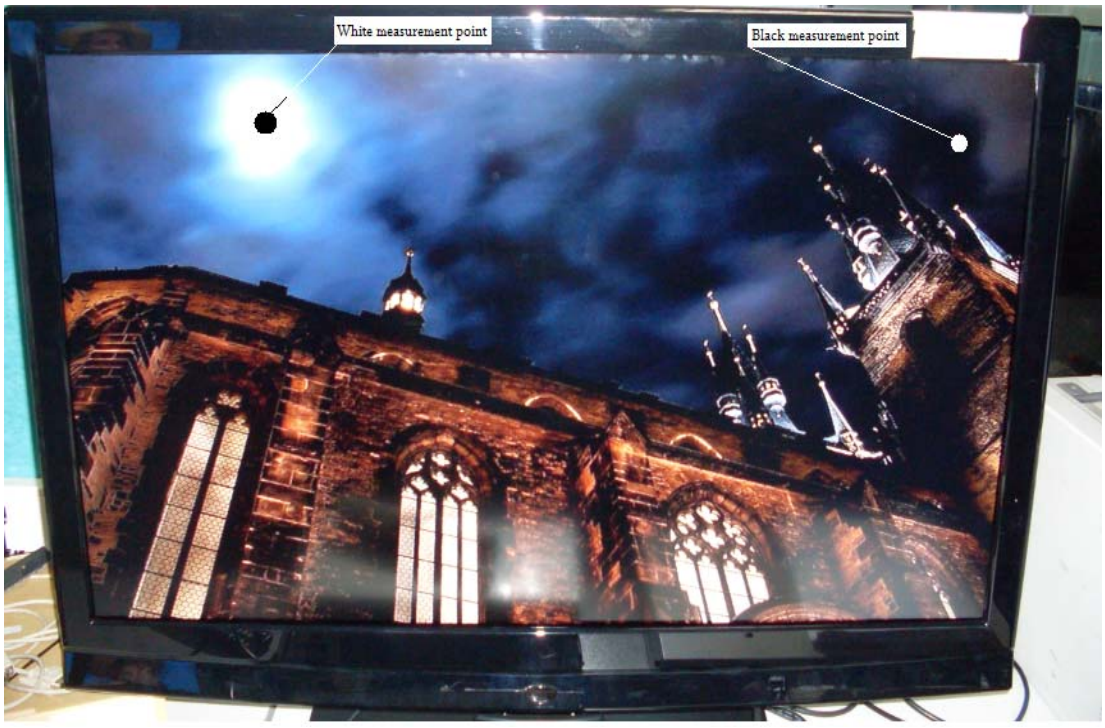


Figure 5.5 Pattern 5. (1920x1080 resolution image)

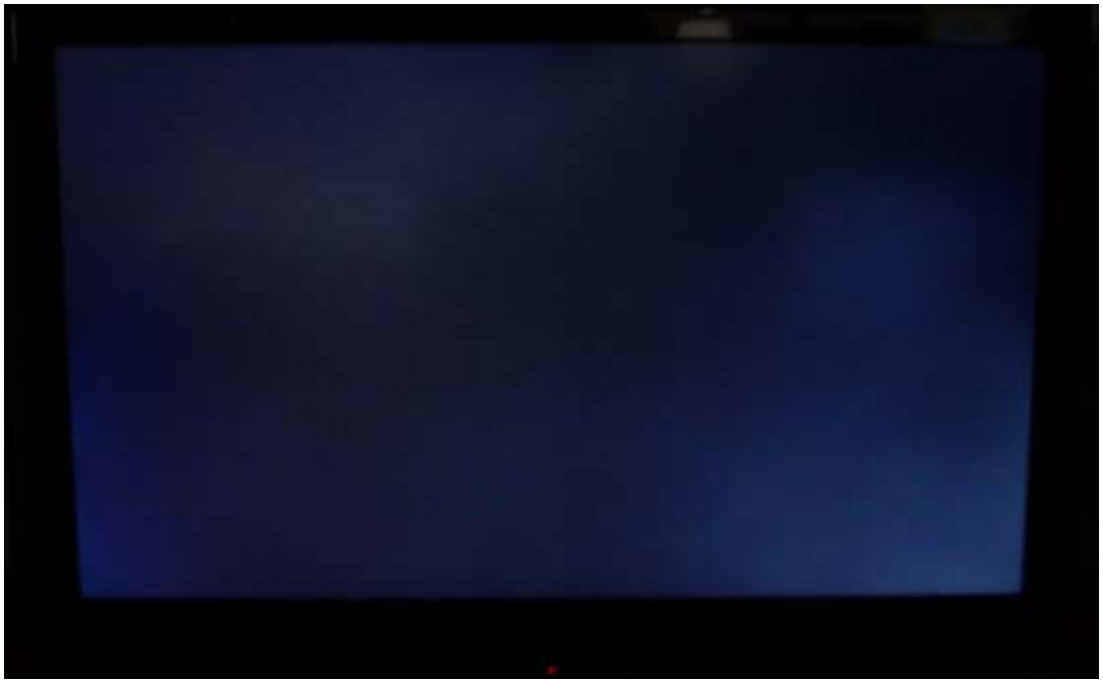


Figure 5.6 Backlight levels of pattern 5.

Table 5.1 shows the contrast ratios of LED backlight with local dimming platform. The static contrast ratio of Pattern 1 and Pattern 4 is very high. The structure of algorithm says that it is much more effective on black-weighted images than white-weighted images on increasing contrast ratio. This is realized according to test results. Pattern 3 is black-white complement of Pattern 1. Pattern 1 is %20 white so Pattern 3 is %20 black. The static contrast ratio changes with the amount of black level. Pattern 4 is %15 white and has the highest contrast ratio.

Table 5.1 Static contrast ratio of LED backlight panel with local dimming.

	LED backlight with local dimming		
	White level	Black Level	Contrast Ratio
Pattern 1	229	0,0001	2290000
Pattern 2	406	0,07	5800
Pattern 3	397	0,51	778
Pattern 4	253	0,0001	2530000
Pattern 5	372	0,2	1860

Table 5.2 shows the tests results of LED backlight panel without local dimming application. Static contrast ratio depends on both black and white level. The maximum contrast ratio belongs to Pattern 1. The highest white level and lowest black level are measured on this pattern.

Table 5.2 Static contrast ratio of LED backlight panel without local dimming.

	LED backlight		
	White level	Black Level	Contrast Ratio
Pattern 1	453	0,42	1079
Pattern 2	406	0,45	902
Pattern 3	399	0,54	739
Pattern 4	390	0,6	650
Pattern 5	408	0,44	927

Table 5.3 shows the static contrast ratio of CCFL backlight panel. Because of the structure of CCFL, the black levels of all patterns are the highest. The major problem of CCFL panels is the weakness of displaying black scenes. Thin Film Transistors (TFT) can not filter the backlight when they switched off. The amount of black level decreases the contrast ratio.

Table 5.3 Static contrast ratio of CCFL backlight panel.

	CCFL backlight		
	White level	Black Level	Contrast Ratio
Pattern 1	430	0,6	717
Pattern 2	390	0,62	629
Pattern 3	350	0,7	500
Pattern 4	385	0,82	470
Pattern 5	392	0,6	653

See Table 5.4 for power consumption of three different platforms. Power consumption changes inversely proportional to contrast ratio on LED backlight with local dimming. On the other hand, on LED backlight and CCFL backlight platforms power consumption changes according to the white level. The power consumption is the maximum where white level of pattern is measured maximum. Moreover, LED backlight is better than CCFL backlight on same patterns in terms of power consumption. Consequently, the local dimming algorithm is successfully applied to the set-ups and the aims of this thesis are achieved and proved with the measurements.

Table 5.4 Power consumption of 3 different panels.

	LED backlight with local dimming	LED backlight	CCFL backlight
Pattern 1	122 W	210 W	233 W
Pattern 2	134 W	199 W	214 W
Pattern 3	169 W	172 W	199 W
Pattern 4	110 W	188 W	209 W
Pattern 5	146 W	200 W	214 W

CHAPTER SIX

CONCLUSION

Known as, the most common disadvantage of LCD-TV sets to plasma and CRT is contrast ratio. LCD TV technology leaks out the strong backlight and the black areas of images are not viewed as real black. Distortion of black level affects the image quality. LCD is the worst at black area displaying in comparative test of the market among all technologies. As well as joining LED backlight panels to the market, the contrast ratio of LCD TV sets increase a little bit than CCFL backlight panels. However, LCD is not able to display blacks like plasma or CRT.

Furthermore, LED backlight technology gives the ability of controlling backlight according to the video content. Many algorithms are developed for dimming backlight locally and aim to increase the contrast ratio. LED backlight technology is economical than CCFL backlight. With local dimming, LED backlight panel saves much more power.

Besides the all advantages of LCD TV sets, LED backlight local dimming algorithms take away the disadvantage of contrast ratio and obtain very quality image.

The algorithm developed in this thesis aims improving contrast ratio and minimizing power consumption. As is understood from results, LED backlight panels are better than CCFL backlight panels in terms of contrast ratio and power consumption. Applying the local dimming to the platform, the improvements in terms of contrast ratio and power consumption are apparent. Power consumption is about %50 less than CCFL panels and contrast ratio 2000 times higher depend on applied pattern. The aim of thesis, increasing contrast ratio and power consumption minimizing is achieved. But the algorithm is not effective on white-weighted images. This is the result of design principle of algorithm. The look up table and filtering stages cause that non-effective result. However, if look up table and filtering stages

are disabled, artifacts are appeared. Also it is known high contrast ratio is much more perceptible on black-weighted image. So the contrast ratio on white-weighted images is not important for this case.

By using the algorithm, high quality image is generated for viewing. In contrary to known image processing methods, local dimming algorithm does not change the content of video, only utilizes the image. Local dimming algorithm controls only backlight.

Local dimming feature highlights the LED backlight panels in market. In addition to this, their slim designs, shows that not only image quality is improved, but also physical design is developed.

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APPENDICES

Appendix A Verilog Codes Of Doubling Data

```
`timescale 1ns / 1ps
module ddata(
input rx,
input fast_clk,
output out1,
output out2
);
reg dataout1, dataout2;
always @ (posedge fast_clk)
begin
dataout1 = rx;
end
always @ (negedge fast_clk)
begin
dataout2 = rx;
end
assign out1 = dataout1;
assign out2 = dataout2;
endmodule
```

Appendix B Verilod Codes of Shift Register

```
module shiftreg(
input data,
input fast_clk,
output [6:0] regdataout
);
integer i = 0;
reg [6:0] dataout;
always @ (posedge fast_clk)
begin
dataout[i] = data;
i = i+1;
if (i==7) i = 0;
end
assign regdataout = dataout;
endmodule
```

Appendix C Verilog Codes of Parallel Register

```
module ddata_sr(
input fast_clk,
input slow_clk,
input r_in,
output [13:0] parallelout
);
wire datahigh, datalow;
wire [6:0] reg_data_high, reg_data_low;
reg [6:0] par_data_high,par_data_low;
reg data_high, data_low;
ddata U_dd(.rx(r_in), .fast_clk(fast_clk), .out1(datahigh), .out2(datalow));
always @ (posedge fast_clk)
begin
data_high = datahigh;
data_low = datalow;
end
always @ (posedge slow_clk)
begin
par_data_high = reg_data_high;
par_data_low = reg_data_low;
end
shiftreg U_sr1(.data(data_high),  .fast_clk(fast_clk), .regdataout(reg_data_high));
shiftreg U_sr2(.data(data_low),  .fast_clk(fast_clk), .regdataout(reg_data_low));
assign parallelout =
{par_data_high[0],par_data_low[0],par_data_high[1],par_data_low[1],par_data_high
[2],par_data_low[2],par_data_high[3],par_data_low[3],par_data_high[4],par_data_lo
w[4],par_data_high[5],par_data_low[5],par_data_high[6],par_data_low[6]};
endmodule
```

Appendix D Verilog Codes of Aligner

```
module aligner(
input [13:0] data_in,
input norm_clk,
input slow_clk,
output [6:0] data_out
);
reg [6:0] out_data;
reg [6:0] pixel_1, pixel_2;
always @ (posedge slow_clk)
begin
pixel_1 = data_in [13:7];
pixel_2 = data_in [6:0];
end
always @ (posedge norm_clk)
begin
if (slow_clk) out_data = pixel_1;
else out_data = pixel_2;
end
assign data_out = out_data;
endmodule
```

Appendix E Verilog Codes of LVDS Mapping

```
module dimmer(
a,
b,
c,
d,
e,
clk,
maxrgb,
den,
h_sync,
v_sync
);
input [6:0] a;
input [6:0] b;
input [6:0] c;
input [6:0] d;
input [6:0] e;
input clk;
output [7:0] maxrgb;
output den;
output h_sync;
output v_sync;
reg [9:0] kirmizi, yesil, mavi,en_buyuk;
integer i ;
reg vsync,hsync,de;
reg [6:0] data_a,data_b,data_c,data_d,data_e;
always @ (posedge clk)
begin
case (i)
0: begin
```

```
data_a = a;
data_b = b;
data_c = c;
data_d = d;
data_e = e;
i = 1;
end
1: begin          //rgb mapping "ysf" vesa format
kirmizi [0] = a[1];
kirmizi [1] = a[0];
kirmizi [2] = data_a[6];
kirmizi [3] = data_a[5];
kirmizi [4] = data_a[4];
kirmizi [5] = data_a[3];
kirmizi [6] = d[1];
kirmizi [7] = d[0];
kirmizi [8] = e[1];
kirmizi [9] = e[0];
mavi [0] = data_b[3];
mavi [1] = data_b[2];
mavi [2] = c[1];
mavi [3] = c[0];
mavi [4] = data_c[6];
mavi [5] = data_c[5];
mavi [6] = data_d[4];
mavi [7] = data_d[3];
mavi [8] = data_e[4];
mavi [9] = data_e[3];
yesil [0] = data_a[2];
yesil [1] = b[1];
yesil [2] = b[0];
yesil [3] = data_b[6];
```

```
yesil [4] = data_b[5];
yesil [5] = data_b[4];
yesil [6] = data_d[6];
yesil [7] = data_d[5];
yesil [8] = data_e[6];
yesil [9] = data_e[5];
if (yesil >= kirmizi)
begin
if ( kirmizi >= mavi) en_buyuk = yesil;
else
begin
if (yesil >= mavi) en_buyuk = yesil;
else en_buyuk = mavi;
end
end
else
begin
if (yesil >= mavi) en_buyuk = kirmizi;
else
begin
if (kirmizi >=  mavi) en_buyuk =kirmizi;
else en_buyuk = mavi;
end
end
vsync = data_c[3];
hsync = data_c[2];
de = data_c[1];
i = 0;
end
endcase
end
assign maxrgb = en_buyuk[9:2];
```

```
assign v_sync = vsync;
assign h_sync = hsync;
assign den = de;
endmodule
```

Appendix F Verilog Codes of Generating Dimming Value

```
module dimming_value(
hsync,
vsync,
max_rgb,
norm_clk,
data_out
   );
input hsync;
input vsync;
input [7:0] max_rgb;
input norm_clk;
output [2:0][2:0][23:0] data_out;
integer j = 0;
integer i= 0;
integer k = 0;
integer a = 0;
integer y = 0;
reg [2:0][2:0][23:0] dataout;
always @ (posedge norm_clk)
begin
case (k)
0: begin
if (vsync) k = 1;
end
1: begin
if (hsync)
begin
i = 0;
end
if (a<240)
```

```
begin
dataout[j][i][24:0]= dataout[j][i][24:0] + max_rgb[7:0];
a = a + 1;
end
else
begin
i = i + 1;
a = 0;
if (i > 7)
begin
i = 0;
y = y +1;
end
end
if (y>180)
begin
j = j +1;
y = 0;
if (j > 7)
begin
j = 0;
k = 0;
end
end
endcase  // eof case
end //eof alwayw-begin
assign data_out = dataout;
endmodule
```

Appendix G Verilog Codes of Mapping Dimming Data

```
module data_map(
data_in,
data_out,
norm_clk
   );
input [2:0][2:0][23:0] data_in;
input norm_clk;
output [7:0][7:0] data_out;
reg [7:0][7:0] dataout;
integer i = 0;
integer j = 0;
integer k = 0;
integer a = 0;
always @ (negedge norm_clk)
begin
case (a)
0:        begin
if (j>8) a = 1;
if (i>8) j = j + 1;
if (data_in[j][i]=0)
begin
dataout[k] = 20;
i = i+1;
end
else
begin
if (data_in[j][i]<80)
begin
dataout[k] = data_in[j][i]+data_in[i][j]+data_in[i][j];
i = i + 1;
```

```
end
else
begin
dataout[k] = 255;
i = i + 1;
end
end
end // eof case
1:        begin
i = 0;
j = 0;
end
endcase
end // eof always
assign data_out = dataout;
endmodule
```

Appendix H Verilog Codes of Spatial Filtering

```
module spatial_filter(
ram_data_in,
ram_data_out,
data_address,
we,
norm_clk
   );
input [7:0] ram_data_in;
input norm_clk;
output we;
output [7:0] ram_data_out;
output [7:0] data_address;
reg [7:0] ram_dataout;
reg write_enable;
reg [7:0] k;
reg [11:0] buffer;
reg a;
always @ (negedge norm_clk)
begin
case (a)
0:       begin
if (k>45) k = 0;
buffer  = ram_data_in[k] + ram_data_in[k+1] +ram_data_in[k+2]
+ram_data_in[k+8] +ram_data_in[k+9] +ram_data_in[k+10] +ram_data_in[k+16]
+ram_data_in[k+17] +ram_data_in[k+18];
write_enable = 0;
ram_dataout[k] = buffer[11:4];
ram_dataout[k] = buffer[11:4];
ram_dataout[k] = buffer[11:4];
ram_dataout[k] = buffer[11:4];
```

```
ram_dataout[k] = buffer[11:4];
ram_dataout[k] = buffer[11:4];
ram_dataout[k] = buffer[11:4];
ram_dataout[k] = buffer[11:4];
a = 1;
end
1: begin
write_enable = 1;
a = 0;
k = k +1;
end
endcase
end
assign ram_data_out = ram_data_out;
assign we = write_enable;
assign k = data_address;
endmodule
```

Appendix I Temporal Filtering

```
module temporal_filter(
spram_data_in,
data_address,
panelram_data_in,
panelram_data_out,
norm_clk,
we);
output [7:0] data_address;
input [7:0] spram_data_in ;
input [7:0] panelram_data_in ;
output [7:0] panelram_data_out ;
input  norm_clk;
output we;
reg [7:0] dataout ;
reg write_enable;
reg [7:0] k;
always @ (negedge norm_clk)
begin
dataout[k] = spram_data_in[k]/8 + panelram_data_in[k] /4 + spram_data_in[k]/2;
write_enable = 1;
end
always @ (posedge norm_clk)
begin
k = k+1;
write_enable = 0;
end
assign we = write_enable;
assign panelram_data_out = dataout;
assign data_address = k;
endmodule
```

Appendix J Verilog Codes of SPI Data Sending

```
module lg(
input saat,
input ac_kapa,
input [7:0] ram_data,
output [7:0] ram_adres,
output ram_read,
output spi_clk,
output spi_data,
output v_sync
);
reg vertical = 0;
integer a = 0;
integer i = 0;
reg [7:0] data = 0;
integer m = 0;
reg clock_out = 0;
integer j = 0;
integer b = 7;
integer l = 0;
reg ser_data = 0;
reg check_sum = 0;
integer c = 0;
reg [7:0] adres;
reg read = 0;
always @ (posedge saat)
begin
if (ac_kapa)
begin
case (i)
0:      begin                   //vertical sync generation
```

```
if (a < 150 )
begin
vertical = 1;
a = a+1;
end
else
begin
vertical = 0;
a = 0;
i = 1;
end
end //eof case 0
1:      begin       //vertical sync wait condition
if ( a < 330 )
begin
a = a+1;
end
else
begin
a = 0;
i = 2;
end
end //eof case 1
2:      begin    // data generation
adres = m;
read = 1;
data = ram_data;
if (m > 66 )
begin
m = 0;
i = 5;
end
```

```
else
begin
i = 3;
b = 7;
end
end //eof case 2
3: begin //clock data
if (j < 8)
begin
if (l >= 80 && l <=160)
begin
clock_out = 1;
l = l+1;
if ( l ==160 )
begin
j = j+1;
b = b-1;
l = 0;
end
else
begin
clock_out= 0;
l = l+1 ;
ser_data = data[b];
end
end
else
begin
b = 7;
i = 4;
m = m+1;
j = 0;
```

```
end
end   //eof clock data
4: begin
if (a < 330 )
begin
a = a+1;
clock_out = 0;
end
else
begin
i = 2;
a = 0;
end
end
5: begin
if (c < 8)
begin
if (a < 50000)
begin
a = a+1;
end
else
begin
c = c+1;
a = 0;
end
end
else
begin
c = 0;
i = 0;
a = 0;
```

```
end
end
endcase
end //eof if
end //eof always
assign spi_data = ser_data;
assign spi_clk = clock_out;
assign v_sync = vertical;
assign ram_adres = adres;
assign ram_read = read;
endmodule
```

Appendix K Brief datasheet of FPGA

XILINX®

Spartan-3A DSP FPGA Family: Introduction and Ordering Information

DS610-1 (v2.2) March 11, 2009 — Product Specification

Introduction

The Spartan®-3A DSP family of Field-Programmable Gate Arrays (FPGAs) solves the design challenges in most high-volume, cost-sensitive, high-performance DSP applications. The two-member family offers densities ranging from 1.8 to 3.4 million system gates, as shown in Table 1.

The Spartan-3A DSP family builds on the success of the Spartan-3A FPGA family by increasing the amount of memory per logic and adding XtremeDSP™ DSP48A slices. New features improve system performance and reduce the cost of configuration. These Spartan-3A DSP FPGA enhancements, combined with proven 90 nm process technology, deliver more functionality and bandwidth per dollar than ever before, setting the new standard in the programmable logic and DSP processing industry.

The Spartan-3A DSP FPGAs extend and enhance the Spartan-3A FPGA family. The XC3SD1800A and the XC3SD3400A devices are tailored for DSP applications and have additional block RAM and XtremeDSP DSP48A slices. The XtremeDSP DSP48A slices replace the 18x18 multipliers found in the Spartan-3A devices and are based on the DSP48 blocks found in the Virtex®-4 devices. The block RAMs are also enhanced to run faster by adding an output register. Both the block RAM and DSP48A slices in the Spartan-3A DSP devices run at 250 MHz in the lowest cost, standard -4 speed grade.

Because of their exceptional DSP price/performance ratio, Spartan-3A DSP FPGAs are ideally suited to a wide range of consumer electronics applications, including broadband access, home networking, display/projection, and digital television.

The Spartan-3A DSP family is a superior alternative to mask programmed ASICs. FPGAs avoid the high initial cost, lengthy development cycles, and the inherent inflexibility of conventional ASICs. Also, FPGA programmability permits design upgrades in the field with no hardware replacement necessary, an impossibility with ASICs.

Features

- Very low cost, high-performance DSP solution for high-volume, cost-conscious applications
- 250 MHz XtremeDSP DSP48A Slices
  - Dedicated 18-bit by 18-bit multiplier
  - Available pipeline stages for enhanced performance of at least 250 MHz in the standard -4 speed grade
  - 48-bit accumulator for multiply-accumulate (MAC) operation
  - Integrated adder for complex multiply or multiply-add operation
  - Integrated 18-bit pre-adder
  - Optional cascaded Multiply or MAC
- Hierarchical SelectRAM™ memory architecture
  - Up to 2268 Kbits of fast block RAM with byte write enables for processor applications
  - Up to 373 Kbits of efficient distributed RAM
  - Registered outputs on the block RAM with operation of at least 280 MHz in the standard -4 speed grade
- Dual-range V_{CCAUX} supply simplifies 3.3V-only design
- Suspend, Hibernate modes reduce system power
- Low-power option reduces quiescent current
- Multi-voltage, multi-standard SelectIO™ interface pins
  - Up to 519 I/O pins or 227 differential signal pairs
  - LVCMOS, LVTTL, HSTL, and SSTL single-ended I/O
  - 3.3V, 2.5V, 1.8V, 1.5V, and 1.2V signaling
  - Selectable output drive, up to 24 mA per pin
  - QUIETIO standard reduces I/O switching noise
  - Full 3.3V ±10% compatibility and hot swap compliance
  - 622+ Mb/s data transfer rate per differential I/O
  - LVDS, RSDS, mini-LVDS, HSTL/SSTL differential I/O with integrated differential termination resistors
  - Enhanced Double Data Rate (DDR) support
  - DDR/DDR2 SDRAM support up to 333 Mb/s
  - Fully compliant 32-/64-bit, 33/66 MHz PCI support
- Abundant, flexible logic resources
  - Densities up to 53712 logic cells, including optional shift register
  - Efficient wide multiplexers, wide logic, fast carry logic
  - IEEE 1149.1/1532 JTAG programming/debug port
- Eight Digital Clock Managers (DCMs)
  - Clock skew elimination (delay locked loop)
  - Frequency synthesis, multiplication, division
  - High-resolution phase shifting
  - Wide frequency range (5 MHz to over 320 MHz)
- Eight low-skew global clock networks, eight additional clocks per half device, plus abundant low-skew routing
- Configuration interface to industry-standard PROMs
  - Low-cost, space-saving SPI serial Flash PROM
  - x8 or x8/x16 BPI parallel NOR Flash PROM
  - Low-cost Xilinx® Platform Flash with JTAG
  - Unique Device DNA identifier for design authentication
  - Load multiple bitstreams under FPGA control
  - Post-configuration CRC checking
- MicroBlaze™ and PicoBlaze™ embedded processor cores
- BGA and CSP packaging with Pb-free options
  - Common footprints support easy density migration
- XA Automotive version available

Table 1: Summary of Spartan-3A DSP FPGA Attributes

Device	System Gates	Equivalent Logic Cells	CLB Array (One CLB = Four Slices) Rows	Columns	Total CLBs	Total Slices	Distributed RAM Bits(1)	Block RAM Bits(1)	DSP48As	DCMs	Maximum User I/O	Maximum Differential I/O Pairs
XC3SD1800A	1800K	37,440	88	48	4,160	16,640	260K	1512K	84	8	519	227
XC3SD3400A	3400K	53,712	104	58	5,968	23,872	373K	2268K	126	8	469	213

Notes: 1. By convention, one Kb is equivalent to 1,024 bits.

Architectural Overview

The Spartan-3A DSP family architecture consists of five fundamental programmable functional elements:

- **XtremeDSP™ DSP48A Slice** provides an 18-bit x 18-bit multiplier, 18-bit pre-adder, 48-bit post-adder/accumulator, and cascade capabilities for various DSP applications.
- **Block RAM** provides data storage in the form of 18-Kbit dual-port blocks.
- **Configurable Logic Blocks (CLBs)** contain flexible Look-Up Tables (LUTs) that implement logic plus storage elements used as flip-flops or latches. CLBs perform a wide variety of logical functions as well as store data.
- **Input/Output Blocks (IOBs)** control the flow of data between the I/O pins and the internal logic of the device. IOBs support bidirectional data flow plus 3-state operation. Supports a variety of signal standards, including several high-performance differential standards. Double Data-Rate (DDR) registers are included.
- **Digital Clock Manager (DCM) Blocks** provide self-calibrating, fully digital solutions for distributing, delaying, multiplying, dividing, and phase-shifting clock signals.

These elements are organized as shown in Figure 1. A dual ring of staggered IOBs surrounds a regular array of CLBs. The XC3SD1800A has four columns of DSP48As, and the XC3SD3400A has five columns of DSP48As. Each DSP48A has an associated block RAM. The DCMs are positioned in the center with two at the top and two at the bottom of the device and in the two outer columns of the 4 or 5 columns of block RAM and DSP48As.

The Spartan-3A DSP family features a rich network of routing that interconnect all five functional elements, transmitting signals among them. Each functional element has an associated switch matrix that permits multiple connections to the routing.

Configuration

Spartan-3A DSP FPGAs are programmed by loading configuration data into robust, reprogrammable, static CMOS configuration latches (CCLs) that collectively control all functional elements and routing resources. The FPGA's configuration data is stored externally in a PROM or some other non-volatile medium, either on or off the board. After applying power, the configuration data is written to the FPGA using any of seven different modes:

- Master Serial from a Xilinx Platform Flash PROM
- Serial Peripheral Interface (SPI) from an industry-standard SPI serial Flash
- Byte Peripheral Interface (BPI) Up from an industry-standard x8 or x8/x16 parallel NOR Flash
- Slave Serial, typically downloaded from a processor
- Slave Parallel, typically downloaded from a processor
- Boundary Scan (JTAG), typically downloaded from a processor or system tester

Furthermore, Spartan-3A DSP FPGAs support MultiBoot configuration, allowing two or more FPGA configuration bitstreams to be stored in a single SPI serial Flash or a BPI parallel NOR Flash. The FPGA application controls which configuration to load next and when to load it.

Additionally, each Spartan-3A DSP FPGA contains a unique, factory-programmed Device DNA identifier useful for tracking purposes, anti-cloning designs, or IP protection.

I/O Capabilities

The Spartan-3A DSP FPGA SelectIO interface supports many popular single-ended and differential standards. Table 2 shows the number of user I/Os as well as the number of differential I/O pairs available for each device/package combination. Some of the user I/Os are unidirectional input-only pins as indicated in Table 2.

Spartan-3A DSP FPGAs support the following single-ended standards:

- 3.3V low-voltage TTL (LVTTL)
- Low-voltage CMOS (LVCMOS) at 3.3V, 2.5V, 1.8V, 1.5V, or 1.2V
- 3.3V PCI at 33 MHz or 66 MHz
- HSTL I, II, and III at 1.5V and 1.8V, commonly used in memory applications
- SSTL I and II at 1.8V, 2.5V, and 3.3V, commonly used for memory applications

Spartan-3A DSP FPGAs support the following differential standards:

- LVDS, mini-LVDS, RSDS, and PPDS I/O at 2.5V or 3.3V
- Bus LVDS I/O at 2.5V
- TMDS I/O at 3.3V
- Differential HSTL and SSTL I/O
- LVPECL inputs at 2.5V or 3.3V

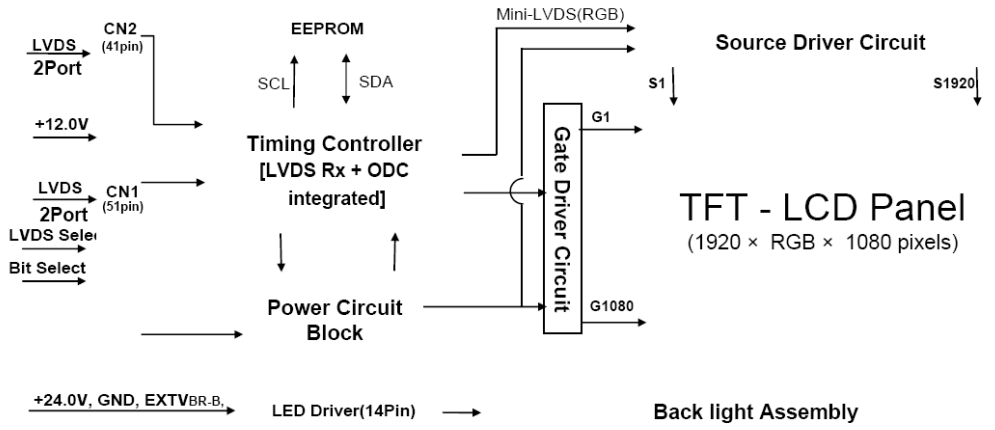
Appendix L Datasheet of Panel

LC420WUL

Product Specification

1. General Description

The LC420WUL is a Color Active Matrix Liquid Crystal Display with an integral Light Emitting Diode (LED) backlight system. The matrix employs a-Si Thin Film Transistor as the active element.
It is a transmissive display type which is operating in the normally black mode. It has a 42.02 inch diagonally measured active display area with WUXGA resolution (1080 vertical by 1920 horizontal pixel array). Each pixel is divided into Red, Green and Blue sub-pixels or dots which are arrayed in vertical stripes.
Gray scale or the luminance of the sub-pixel color is determined with a 10-bit(D) gray scale signal for each dot. Therefore, it can present a palette of more than 1.06B colors.
It has been designed to apply the 10-bit 4-port LVDS interface.
It is intended to support LCD TV, PCTV where high brightness, super wide viewing angle, high color gamut, high color depth and fast response time are important.



General Features

Active Screen Size	42.02 inches(1067.31mm) diagonal
Outline Dimension	983.0(H) x 576.0 (V) x 63.0 mm(D) (Typ.)
Pixel Pitch	0.4845 mm x 0.4845 mm
Pixel Format	1920 horiz. by 1080 vert. Pixels, RGB stripe arrangement
Color Depth	10-bit(D), 1.06 B colors
Luminance, White	500 cd/m^2 (Center 1point ,Typ.)
Viewing Angle (CR>10)	Viewing angle free (R/L 178 (Min.), U/D 178 (Min.))
Power Consumption	Total TBD W (Typ.) (Logic=TBD W, LED Driver=132W [ExtVBR-B=100%])
Weight	11.5 Kg (Typ.)
Display Mode	Transmissive mode, Normally black
Surface Treatment	Hard coating(3H), Anti-glare treatment of the front polarizer (Haze 10%)

Table 3. ELECTRICAL CHARACTERISTICS (Continue)

Parameter			Symbol	Values			Unit	Notes
				Min	Typ	Max		
LED Driver :								
Power Supply Input Voltage			VBL	22.8	24.0	25.2	Vdc	1
Power Supply Input Voltage Ripple				-	-	0.5	Vp-p	1
Power Supply Input Current			IBL_A	-	5.5	6.2	A	Ext V_{BR-B} = 100%
Power Supply Input Current (In-Rush)			Irush	-	10	-	A	Ext V_{BR-B} = 100% … 5
Power Consumption			PBL	-	132	156.2	W	Ext V_{BR-B} = 100%
Input Voltage for Control System Signals	On/Off	On	V on	2.5	-	5.0	Vdc	
		Off	V off	-0.3	0.0	0.8	Vdc	
	Brightness Adjust		ExtV_{BR-B}	10	-	100	%	On Duty
	PWM Frequency for NTSC & PAL		PAL	90	100	210	Hz	4
			NTSC	110	120	252	Hz	4
	Pulse Duty Level(PWM) (Burst mode)		High Level	2.5	-	5.0	Vdc	HIGH: LED on LOW:LED off
			Low Level	0.0	-	0.8	Vdc	
LED :								
Life Time					TBD		Hrs	3

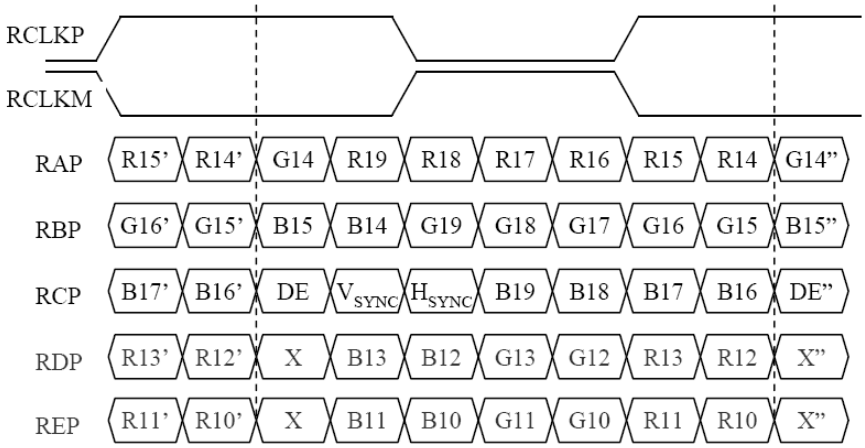
Notes :

1. Electrical characteristics are determined after the unit has been 'ON' and stable for approximately 120 minutes at 25± 2°C. The specified current and power consumption are under the typical supply Input voltage 24Vand V_{BR} (ExtVBR-B : 100%), it is total power consumption.
   The ripple voltage of the power supply input voltage is under 0.5 Vp-p. LGD recommend Input Voltage is 24.0V ± 5%.
2. Electrical characteristics are determined within 30 minutes at 25± 2°C.
   The specified currents are under the typical supply Input voltage 24V.
3. The life time is determined as the time which luminance of the LED is 50% compared to that of initial value at the typical LED current (ExtVBR-B :100%) on condition of continuous operating in LCM state at 25°C.
4. LGD recommend that the PWM freq. is synchronized with One time harmonic of Vsync signal of system. Though PWM frequency is over 120Hz (max 252Hz), function of LED Driver is not affected.
5. The duration of rush current is about 10ms.
6. Even though inrush current is over the specified value, there is no problem if I2T spec of fuse is satisfied.

Appendix M LVDS Data Mapping

LVDS Data-Mapping info. (10bit)

■ LVDS Select : “H” Data-Mapping (JEIDA format)



■ LVDS Select : “L” Data-Mapping (VESA format)