DOKUZ EYLÜL UNIVERSITY

GRADUATE SCHOOL OF NATURAL AND APPLIED SCIENCES

LOG-DOMAIN FILTER DESIGN FOR RF STAGE OF DIGITAL TV RECEIVER SYSTEMS

by

Sadık ŞEHİT

September, 2009

İZMİR

LOG-DOMAIN FILTER DESIGN FOR RF STAGE OF DIGITAL TV RECEIVER SYSTEMS

A Thesis Submitted to the

Graduate School of Natural and Applied Sciences of Dokuz Eylül University

In Partial Fulfillment of the Requirements for the Degree of Master of Science

in Electrical and Electronics Engineering, Electrical and Electronics Engineering Program

by

Sadık ŞEHİT

September, 2009

İZMİR

M.Sc THESIS EXAMINATION RESULT FORM

We have read the thesis entitled **"LOG-DOMAIN FILTER DESIGN FOR RF STAGE OF DIGITAL TV RECEIVER SYSTEMS"** completed by **SADIK ŞEHİT** under supervision of **PROF. DR. UĞUR ÇAM** and we certify that in our opinion it is fully adequate, in scope and in quality, as a thesis for the degree of Master of Science.

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ACKNOWLEDGEMENTS

First of all, I would like to thank my advisor Prof. Dr. Uğur ÇAM who supported and encouraged me to work on this dissertation. I want to present my respects to him, for his worthy advices, guidance, and supports during every stage of this study, with sincerely.

I would like to thank TÜBİTAK for supporting me during my master study.

Sadık ŞEHİT

LOG-DOMAIN FILTER DESIGN FOR RF STAGE OF DIGITAL TV RECEIVER SYSTEMS

ABSTRACT

Surface Acoustic Wave (SAW) filters are used for very different RF applications and well-known with their perfect and sharp filter characteristics. Log-domain filtering is one of the most popular current-mode filtering methods. The aim of this thesis is to design a completely electrical SAW filter by applying log-domain filter methods. SAW filters that are specific for TV applications are the subject of this thesis.

In this thesis, how an RF&IF stage works and importance of SAW filter for this stage are described. Signal flow graph method and state space synthesis are important approaches for log-domain filtering. Third order and fifth order Chebyshev type low-pass filter are given as examples. Sixth order Chebyshev type bandpass filter is designed by using two different log-domain approaches.

Key Words: Log-domain filters, state-space synthesis method, signal flow graph method, current-mode circuits, SAW filters, RF filters.

SAYISAL TV ALICI SİSTEMLERİ RF KATI İÇİN LOGARİTMİK ORTAM SÜZGECİ TASARIMI

ÖZ

Yüzeysel akustik dalga süzgeçleri çok farklı radyo dalga uygulamalarında kullanılır ve keskin karakteristiği ile bilinirler. Logaritmik ortam süzgeçleri ise önemli akım mod süzme metotlarından biridir. Bu tezin amacı logaritmik ortam süzgeç tasarım metotlarına başvurularak tamamıyla elektriksel eşdeğer bir yüzeysel akustik dalga süzgeci tasarlamaktır. Bu çalışmada TV uygulamalarına özel yüzeysel akustik dalga süzgeçleri konu alınmıştır.

Bu tezde RF&IF bloğunun nasıl çalıştığı ve yüzeysel akustik dalga süzgeçlerinin bu blok için önemi açıklanmıştır. İşaret akış diyagramları metodu ve durum-uzay sentez metodu önemli logaritmik ortam süzgeç yaklaşımlarıdır. Üçüncü ve beşinci derece Chebyshev tipi alçak geçiren süzgeçler örnek olarak verilmiştir. İki farklı logaritmik ortam süzgeç yaklaşımı kullanılarak altıncı derece Chebyshev tipi bant geçiren süzgeç tasarlanmıştır.

Anahtar Kelimeler: Logaritmik ortam süzgeçleri, durum-uzay sentez metodu, işaret akış diyagramları metodu, akım modlu devreler, yüzeysel akustik dalga süzgeçleri, radyo dalga süzgeçleri.

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CHAPTER ONE

INTRODUCTION

1.1 Introduction

Since ancient times, humans have dream of distant lands. Hearing and seeing events occurring far away had not been possible for people. It was in the 19th century that the dreams of the tele (far off)-phone (to hear) and tele-vision (to see) started to be given thought from a scientific standpoint and to be considered subjects for technical proof.

The story of television had begun in 1873 with Joseph May, who is a young Irish telegraph operator, discovered the photoelectric effect: selenium bars, exposed to sunlight, show a variation in resistance. Variations in light intensity can therefore be transformed into electrical signals. That means they can be transmitted.

In 1875 George Carey proposed a system based on the exploration of every point in the image simultaneously: a large number of photoelectric cells are arranged on a panel, facing the image, and wired to a panel carrying the same number of bulbs.

Constantin Senlecq published a sketch detailing a similar idea in an improved form: two rotating switches were proposed between the panels of cells and lamps, and as these turned at the same rate they connected each cell, in turn, with the corresponding lamp. With this system, all the points in the picture could be sent one after the other along a single wire in France in 1881. This is the basis of modern television: the picture is converted into a series of picture elements. (Peters, 2000)

The cathode ray tube with a fluorescent scene was invented in 1897. Karl Ferdinand Braun, of the University of Strasbourg, had the idea of placing two electromagnets around the neck of the tube to make the electron beam move horizontally and vertically. On the fluorescent screen the movement of the electron beam had the effect of tracing visible lines on the screen.

In 1908 the Scotsman A. A. Campbell Swinton outlined a system using cathode ray tubes at both sending and receiving ends. This was the first purely electronic proposal. He published a description of it in 1911.

In 1925, an electrical engineer from Scotland, John Logie Baird, exhibited in Selfridges department store in London an apparatus with which he reproduced a simple image, in fact white letters on a black background, at a distance. It was not really television because the two discs which served to transmit the image and to reproduce it were mounted on the same shaft. However Baird did effectively demonstrate that the principle of successive scanning could be applied in practice. He did it again in 1926, in his laboratory, with the first transmission of a real scene the head of a person. The picture was scanned in 30 lines, with 5 full pictures every second. The adventure of television has kept on with great contributions of many scientists and engineers. (Peters, 2000)

In 1965 Gordon E. Moore described that the number of transistors that can be placed on an integrated circuit has increased exponentially. He estimated that number of transistors used in an integrated circuit would double approximately every two years. This observation and forecast have continued for almost half a century.

Processing speed, memory capacity, even the number and size of pixels in digital electronic devices are strongly linked to Moore's law.

Nowadays, a television electronic board is not different than a notebook main board. Lots of ICs with different functions, high speed DDR2 RAMs, EEPROMs, high capacity FLASH memories, and even PVR hard disk units are included in a TV chassis. USB, SD-MMC card and Bluetooth applications are some digital input-output applications of today's televisions.

Increasing of digital applications in TV has a lot of reasons. Huge companies directed R&D studies to digital world because of its indisputable advantages over analog, widely using of digital modulation techniques and popularity of digital transmission methods, increasing number of internet applications, market trends to digital contents like CD, DVD, etc. are main reasons of introducing digital components to TV main boards.

Amongst the all reasons, one definitely has the biggest influence, which is growing digital modulation techniques up. Because the RF and IF stages, which are one of the oldest and most important traditional analog blocks of television, should be revised and regenerated.

Surface Acoustic Wave filter abbreviated as SAW filter is an electromechanical device commonly used in radio frequency applications. Electrical signals are converted to a mechanical wave in a piezoelectric crystal. SAW filters are limited to frequencies up to 3GHz.

SAW filter is a sharp, high-order band-pass filter. Because of its high order, an acoustic filter is being used to complete obtaining a pure IF signal. However, an exhausting design process needs different than traditional filter design. For each application a new design needs specifically because of its nonadjustable characteristic.

1.2 Objectives of Thesis

The aims of this thesis are proposing log-domain filtering methods for designing applicable high order electronic filters that can satisfy the sharp characteristics of SAW filters and presenting the determination of log-domain filters that has prototype characteristic as a SAW filter.

Logarithmic-domain filter is one of very different filtering methods which constitute the subject of this study.

Basically, the electrical signal of a linear domain is converted to logarithmic domain. The filtering operation is being done in log-domain.

The thesis consists of six chapters. An introduction to the thesis is given in Chapter One.

Basics of RF stage and tuning operation of a TV are explained in Chapter Two. The functions of tuner, IF demodulator and SAW filter is given with details.

The logarithmic domain filters are introduced in Chapter Three. First, basic log-domain building blocks are explained with a short historical and theoretical background. There are some log-domain network examples and their equations like damped integrator, input and output stages.

There are several types of log-domain integrators. Each integrator type can be proposed for different performance criteria. The basic integrators will be shown next

pages. These building blocks can easily be developed for specific applications. Integrators that attend to purpose of high-speed or low-power are the other popular basic integrators. Although improving integrators are really important in order to improving the log-domain filtering method, first question in this thesis should be how to synthesise a log-domain network from with respect to an ordinary analog filter. Chapter Four achieves to describe the signal flow graph method and apply that method to the reference circuit of the thesis. Design steps given in the chapter are first applied for an example fifth order Chebyshev filter and than for the subject of thesis, which is sixth order Chebyshev bandpass filter.

State space synthesis which is another log domain design method is examined in Chapter five. After design steps are given with detailed, a third order Chebyshev low pass filter is converted to log-domain by using state space synthesis method as an example. At the final step an equivalent log-domain circuit to the reference sixth order Chebyshev bandpass filter is determined.

Finally, in Chapter Six the final results of two methods are compared and conclusions are given.

CHAPTER TWO

TV SYSTEMS, RF STAGE, AND CLASSICAL FILTERING FOR RF APPLICATIONS

2.1 Basics of RF Stage and Tuning Operation

The electromagnetic spectrum, which is the range of all possible electromagnetic radiation frequencies extends from below the frequencies used for modern radio (at the long-wavelength end) through gamma radiation (at the short-wavelength end), covering wavelengths from thousands of kilometres down to a fraction the size of an atom.

Radio frequency (RF) is a frequency or rate of oscillation within the range of about 3 Hz to 300 GHz. (Huang, 2002) This is the table of contents to a list showing how the radio frequency spectrum is allocated to different users.

For television literature RF means three different bands, which are named VHF-H (Very High Frequency- High band), VHF-L (Very High Frequency-Low band) and UHF (Ultra High Frequency). The band between 40MHz and 140MHz is VHF-L, VHF-H band extends from 141MHz to 425MHz, and UHF band is between 426MHz and 870MHz. These bands are total combination of frequencies that are used for both analog and digital TV broadcasting systems at different countries. Table 2.1 is related with the frequency bands, which are allowed for public channel transmission for different countries. Broadcasting systems for analog TV and modulation standards for digital TV are other important subjects in TV transmission.

Table 2.1 Frequency band used in different countries (Huang, 2002)

COUNTRY	CHANNEL TRANSMITTED FREQUENCY BAND
CCIR	48.25~855.25 MHz
CHINA	44.25~863.25 MHz
FRANCE	47.75~216.25 MHz
TAIWAN	55~991.25 MHz
JAPAN	91.25~765.25 MHz
UK	471~855.255 MHz
FM RADIO 1	79~90 MHz
FM RADIO 2	88~108 MHz
DVB-T	55~860 MHz

There are three analog broadcasting systems, which are still used and differ from country to country in the world. PAL, NTSC and SECAM are three video broadcasting systems while B/G, D/K, I, M, N, L, and L′ are sound broadcasting systems. The map below shows how three video broadcasting systems are spreading at different regions of all over the world.

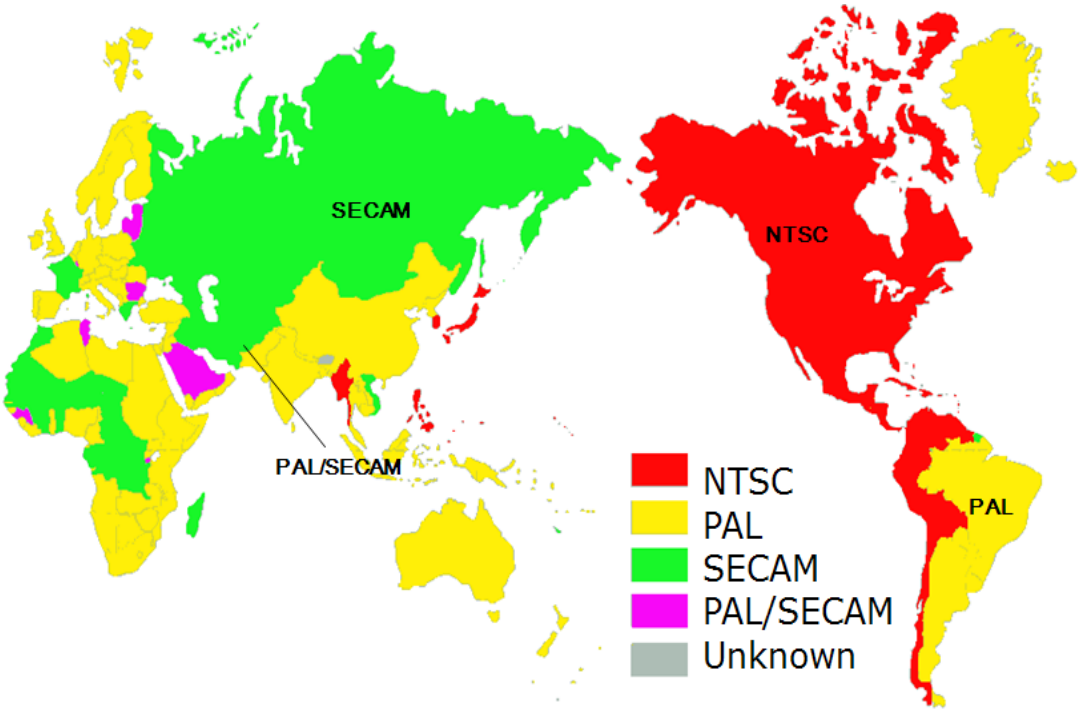

Figure 2.1 Video broadcasting systems at different regions of all over the world. (Huang, 2002)

Digital TV standards are as complex as analog TV standards. ATSC, DVB, ISDB and Open Cable are four important digital television standards that are developed by different countries.

MPEG2 or newly MPEG4 are used as video compression. MPEG or Dolby digital is accepted as audio compression standards. Terrestrial, cable or satellite transmission methods are developed.

ATSC accepts 8-VSB modulation for terrestrial transmission, 16-VSB3 for cable, and QPSK, 8-PSKor 16QAM modulation techniques for satellite.

DVB accepts COFDM for terrestrial, 16-QAM, 32-QAM, 64-QAM, 128-QAM, and 256-QAM for cable, and QPSK for satellite.

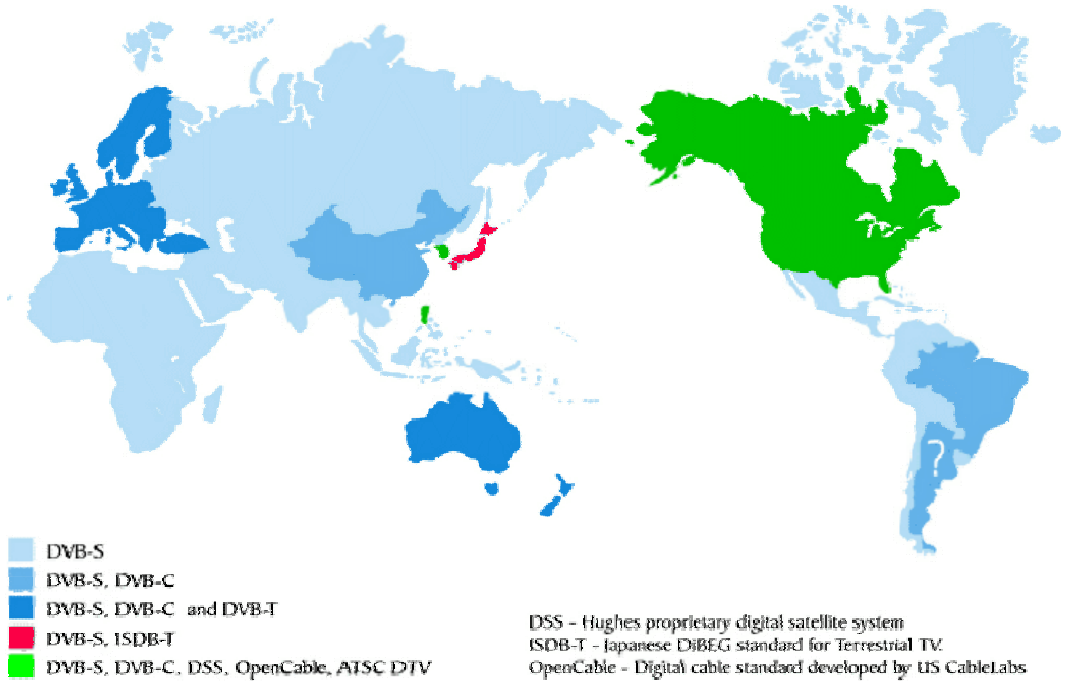

Figure 2.2 Digital Television standards that are used by different countries. (Huang, 2002)

Channel Bandwidth is also another parameter makes the systems different. An ATSC standard channel has 6 MHz bandwidth, while in DVB standard it can be 6, 7 or 8MHz bandwidth. A short table of comparison is given in table 2.2 in order to see main differences of four digital TV (DTV) standards.

Table 2.2 Accepted parameters of four standards (Huang, 2002)

PARAMETER	ATSC	DVB	ISDB	OPEN CABLE
Video compression	MPEG2 or MPEG4			
Audio compression	DOLBY DIGITAL	MPEG DOLBY DIGITAL		DOLBY DIGITAL
Bitstream format	MPEG TRANSPORT STREAM			
Modulation for Terrestrial	8-VSB	COFDM	BST-OFDM	
Modulation for Cable	16-VSB3	16,32,64,128,256-QAM		64,256-QAM
Modulation for Satellite	QPSK, 8PSK,16QAM	QPSK		
	6MHz	6,7,8MHz		6MHz

All these variety of transmission, modulation, broadcasting systems and other parameters make a television system have a perfect RF & IF stage. So, it is obvious that RF & IF stage is the most important block of a receiver system in order to present a high quality picture and sound.

An analog RF & IF stage has sub-blocks as balum, tuner, SAW filter, IF demodulator. RF wave is the input of the block while a video signal in CVBS format and an audio signal or Sound IF (SIF) are output of the block.

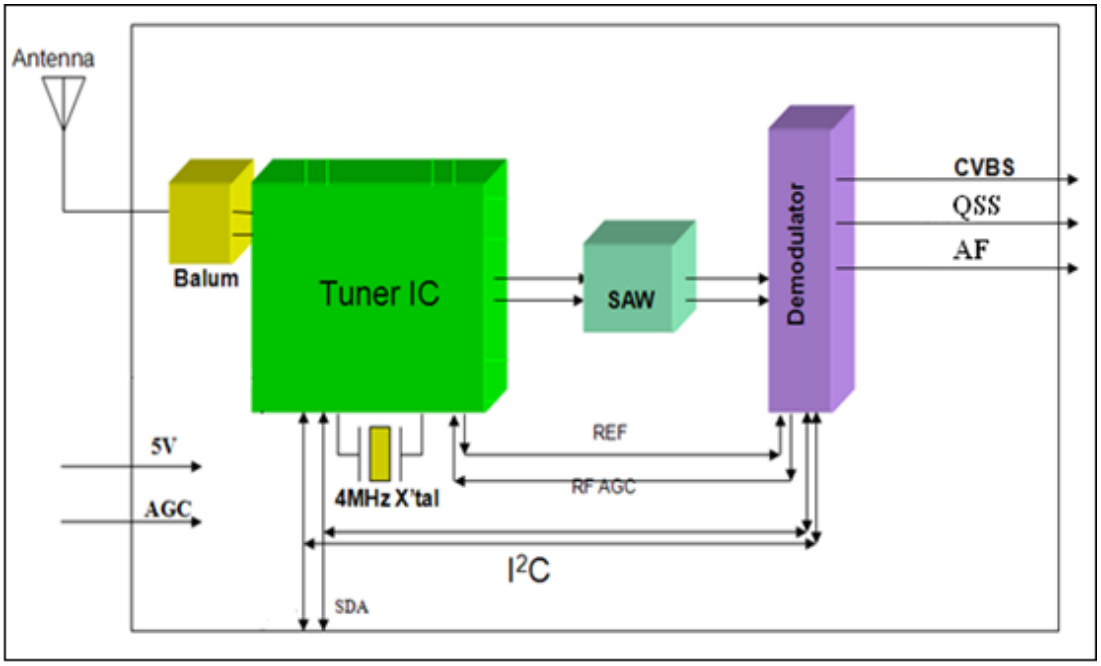

Figure 2.3 RF & IF stage of an analog TV.

Balum has a trap circuit, a filter, and a MOSFET amplifier circuit. Tuner is the block, which channel tuning is done. Input of the tuner is three wide bands, VHF-H, VHF-L and UHF, where the output is an 8-10MHz bandwidth IF signal. Tuner has PLL, three band mixer and IF amplifier sub-blocks. Balum is also accepted as a sub-block of new tuners. Figure 2.2 shows the tuner sub-blocks.

A tuning operation starts at IF demodulator IC. IC sends a command includes channel frequency. This is called tuning frequency. As tuning filter filters RF in order to get this frequency, PLL produce a signal for mixer. The signal frequency is calculating according to accepted IF signal frequency of the system. The mixer is responsible for changing the tuning frequency to IF frequency which is mostly smaller than tuning frequency. By the way modulated and transmitted channel data is also transferred to IF frequency.

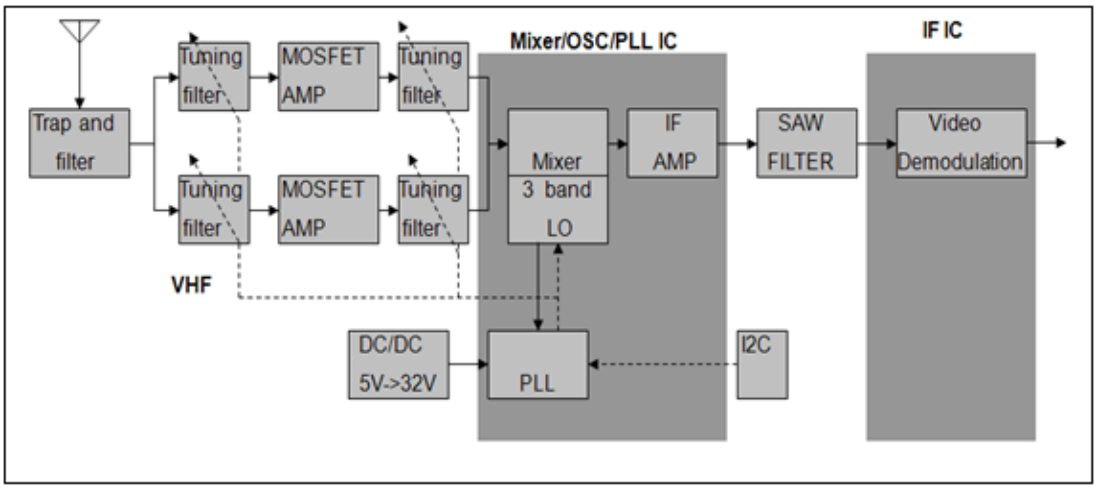

Figure 2.4 Tuning operation.

The explanation of this operation mathematically is requested tuning frequency minus the signal generated by PLL should be equal to IF frequency. The example given in the figure 2.5 can be shown mathematically as:

$$LO = tuning\ freq. + IF\ freq.$$

$$LO = 193.25MHz + 45.75MHz = 239MHz$$

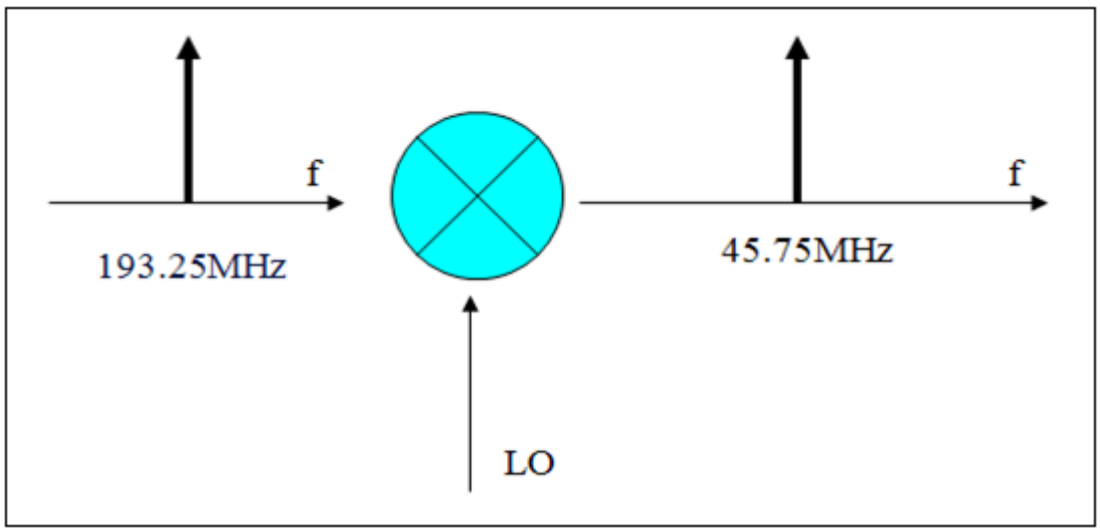

Figure 2.5 The mathematical representation of IF frequency.

Surface Acoustic Wave filter abbreviated as SAW is a sharp, high-order band-pass filter. Because of its high order, an acoustic filter is being used to complete obtaining required 6-8MHz IF signal. There needs an exhausting design process different than traditional filter design steps. For each application a new design needs specifically because of its nonadjustable characteristic.

SAW filter is the heart of RF & IF stage because of its great contributions to tuning process. Tuner block should be more complex, unless SAW filter exists. This is why SAW filter is unchangeable block of an RF&IF stage. Today some tuner companies has SAW filter inside model tuners in the market. Because of its importance at RF&IF stage and acoustic design difficulties, this thesis is related SAW filter designing. Following chapters include suggestions for SAW filter design electronically.

This nonadjustable filter's characteristic has serious importance for the performance of demodulation process by suppressing the side lobs and pass the 6-8MHz IF signal. Some SAW filters are used for video and audio filtering separately. But some are used for filtering both video and audio signals simultaneously.

IF demodulator, which is the master of RF & IF stage used to demodulate the IF signal converted from transmitted signal. The outputs of a demodulator are video and audio information. Video output is composite video abbreviated as CVBS. Audio output is AF for mono sound and QSS for stereo sound. CVBS and QSS information wire to audio and video processing units of main board.

IF demodulator can be conducted in order to demodulate PAL, NTSC, or SECAM for video and B/G, D/K, I, M, N, L, or L′ for audio by microcontroller. If the user wants to watch a channel of SECAM L′, IF demodulator should use SECAM colour

system and L′ sound system. Hence, microcontroller communicate with IF demodulator by using I2C protocol. IF demodulator and tuner also use another I2C wire for tuning.

A digital RF & IF stage has sub-blocks as balum, tuner, SAW filter, IF demodulator. RF & IF stage working principle in a digital TV is completely same as analog one. The main difference is the demodulation process. Instead of analog modulation techniques, various types of digital modulation techniques are used. Because of this reason a digital demodulator is being used. Input of a digital modulator is IF signal, where the output is MPEG2 or MPEG4 transport streams. Transport stream consists of 8 bit digital data, clocks and error bits. TS signals wires to microcontroller for TS and MPEG decoding and video obtaining.

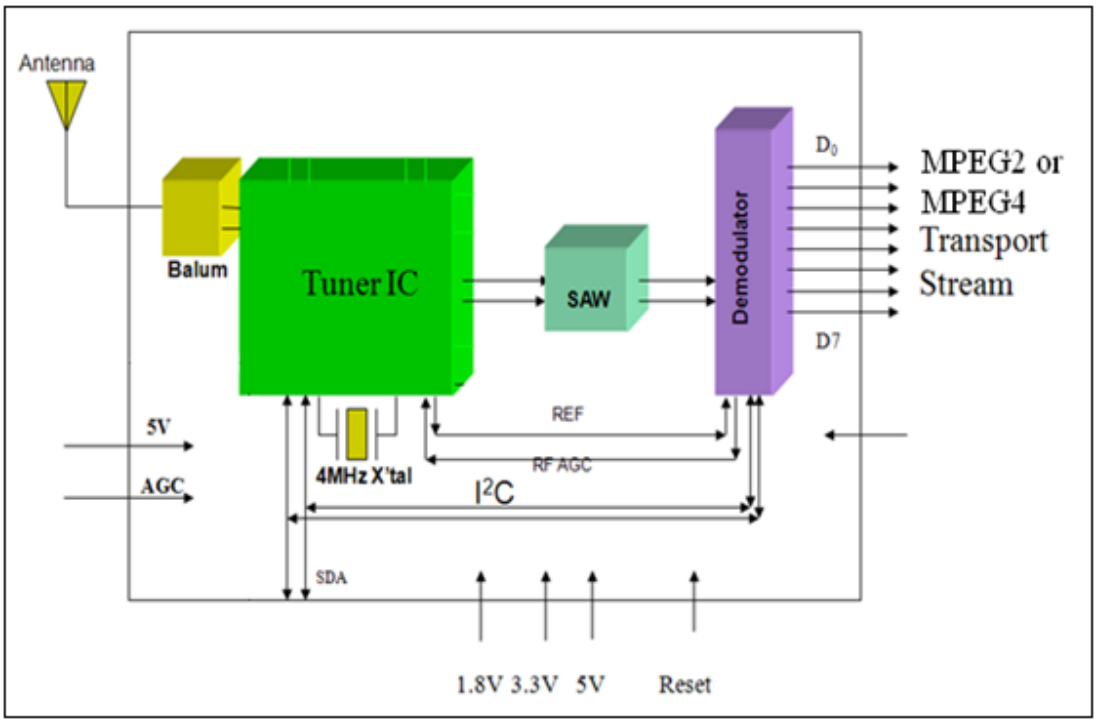

Figure 2.6 RF & IF stage of a digital TV.

DVB standards accept COFDM (Coded Orthogonal Frequency Division Multiplexing modulation) for terrestrial digital video broadcasting. For cable digital video broadcasting QAM (Quadrature Amplitude Modulation) and for satellite digital video broadcasting QPSK (Quadrature Phase-Shift Keying) are used. In order to tune one of these broadcasting, a demodulator which the related demodulation supported IC is needed. Today nearly most of the demodulators support only one modulation type. Some manufacturers are newly started to support both COFDM and QAM modulation with respect to increasing market requests of DVB-T and DVB-C.

2.2 SAW Filters

2.2.1 Basics of a SAW Filter

A surface acoustic wave (SAW) is a type of mechanical wave motion which travels along the surface of a solid material. The wave was discovered in 1885 by Lord Rayleigh. Rayleigh showed that SAWs could explain one component of the seismic signal due to an earthquake, a phenomenon not previously understood. Today, these acoustic waves are often used in electronic devices.

Starting around 1970, SAW devices were developed for pulse compression radar, oscillators, and bandpass filters for domestic TV and professional radio. In the 1980s the rise of mobile radio, particularly for cellular telephones, caused a dramatic increase in demand for filters.

Electronic devices need to generate the SAWs from an electrical input signal, and then use the SAW to generate an electrical output signal. The conversion process of electric to acoustic or acoustic to electric is called ‘transduction’. This can be achieved by piezoelectricity, which is a property of many solid materials. In a

piezoelectric material there is a mechanism which offers coupling between electrical and mechanical disturbances. Hence, application of an electric field sets up mechanical stresses and strains. Conversely, a mechanical stress due to pressure, for example, gives an electric field, and hence a voltage.

Piezoelectricity occurs in many materials but there is a primary requirement that the material must be anisotropic, so that its properties depend on the orientation relative to the internal arrangement of the atoms. Usually, this means that crystalline materials must be used. The common materials for SAWs are crystals of quartz, lithium niobate or lithium tantalate, which are all piezoelectric.

RF filters and IF filters using SAW technologies have an important role to improve the performance cut-off characteristics.There are three kinds of IDT (Inter-Digital Transducer) design method for RF SAW filters. These are an IIDT (Inter-digitated IDT) design, a ladder-type SAW filter design and a DMS (Double Mode SAW) design (figure 2.7). Ladder-type SAW filters is the most suitable design method for the high frequency and wide-band requirement.

The ladder type is suitable for the requirement with a low insertion loss, a wide band, and/or a high-power durability, while the DMS is available for a low insertion loss and a high attenuation level of the out-of-band in the low power application. Recently, the IIDT is less used in the RF application for its high insertion loss.

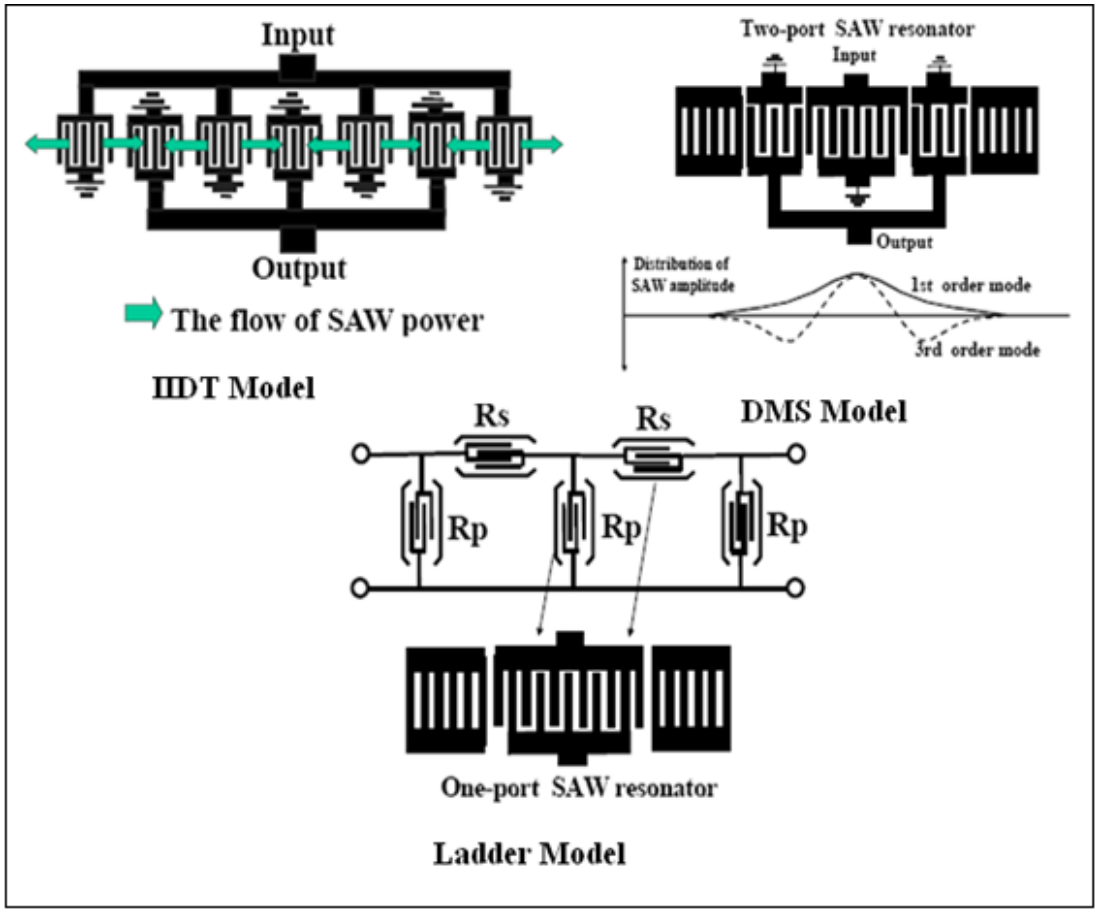

Figure 2.7 IIDT (Inter-digitated IDT) design, ladder-type SAW filter design and DMS (Double Mode SAW) design. (Rukhlenko, 2005)

2.2.2 Parameters for Specifying a SAW Filter

Because of the special qualities of SAW devices, it is not helpful to think in terms of standard responses such as Butterworth or Chebyshev. Instead, it is better to specify the basic requirements directly. The main parameters which need to be specified are:

- Centre frequency (f_0)
- Width of passband (Bp)
- Amplitude variation over the above bandwidth (Ap)

- Phase variation over the above band width (Δφ)
- Transition bandwidth (Bs)
- Stop-band rejection (REJ)
- Insertion loss (IL)

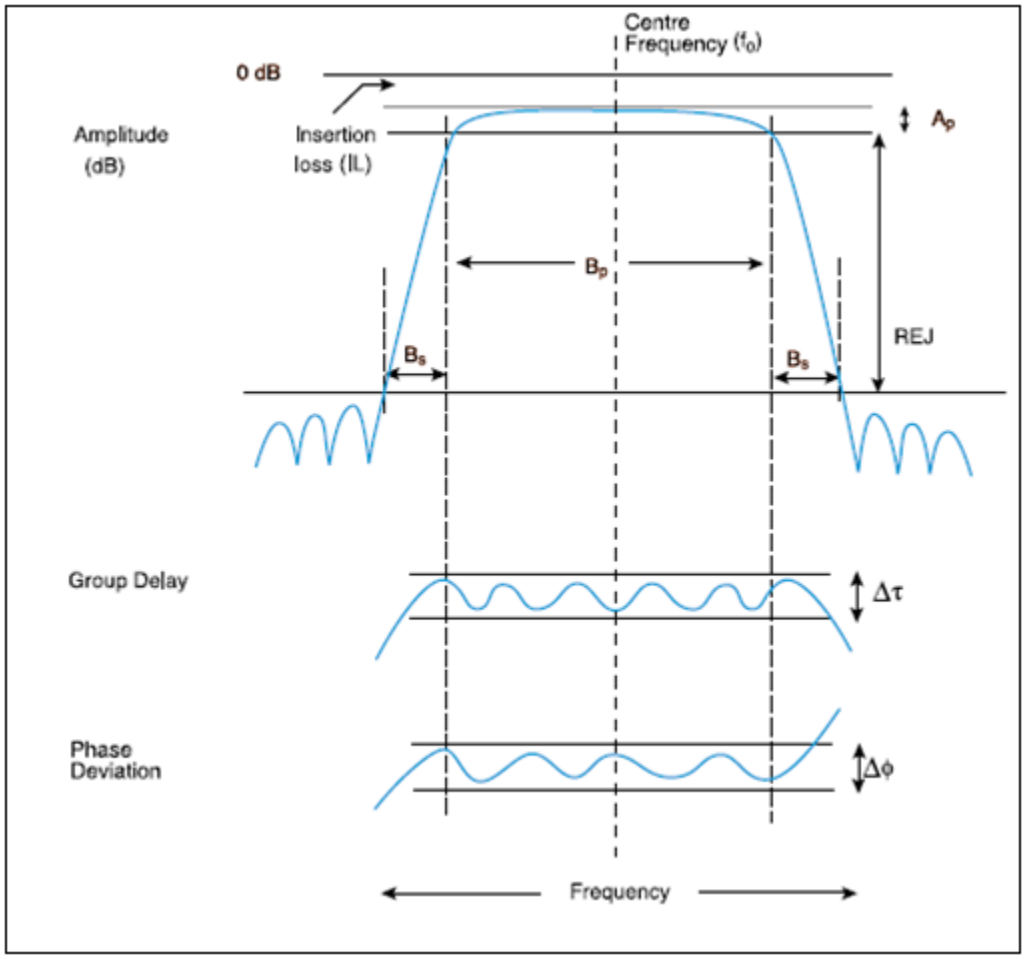

Figure 2.8 Main parameters of SAW filter. (Rukhlenko, 2005)

The fractional bandwidth is Bp ÷ f_0. This ratio has a strong bearing on the substrate material to be used, and hence the temperature coefficient. The first consideration for the SAW designer is to select a suitable material and device type.

The shape factor is the bandwidth at the stopband edges divided by the width of the passband, i.e. (Bp + 2 •Bs) ÷ Bp. The minimum possible value for this depends on the filter type. Transversal filters can have shape factor as low as 1.1. The actual filter size is largely determined by Bs. The minimum value for Bs is approximately 200 kHz.

2.2.3 Different SAW Characteristics in the Market

Today, SAW devices are key components for TV applications, DVB receivers, cellular phones, and other mobile communication products with small and thin size. The productions of RF and IF SAW filters are growing up year by year according to the growth of the consumer electronics and cellular markets.

Almost all of the SAW manufacturers' SAW device selection table contents various type of SAW characteristics and parameters for multimedia applications. This is why each manufacturer has a different customer profile. For instance manufacturer should satisfy both TV industry and mobile industry at the same time. A TV or a DVB receiver manufacturer should need completely different devices for ATV, CATV, VCR, DVD-R, DVB, DAB, SAT applications and transmission standards. The most common applications, which can be found at almost each manufacturer, are given below:

- IF filters for intercarrier applications,
- IF filters for video applications,
- IF filters for audio applications,
- IF filters with switching function between two channels,
- IF filters for quasi/split sound applications,

- Bandpass filters for TV applications,
- Vestigial sideband filters,
- Bandpass filters for digital audio applications,
- RF bandpass filters,
- Bandstop filters,
- Satellite filters

At the end of this chapter, there are three SAW device characteristics, which are used for different purposes.

EPCOS X6966M: IF filter for digital TV applications. Using for both video and audio applications. The center frequency is 36.125MHz.

Table 2.3 Filter Characteristics of EPCOS X6966M

				min.	typ.	max.	
Insertion attenuation			α				
Reference level for the following data		36,125 MHz		18,0	20,3	21,0	dB
Amplitude ripple			$\Delta\alpha$				
	32,65 ...	39,60 MHz		0,0	0,5	1,0	dB
Pass bandwith							
α_{rel} ≤1 dB			B_{1dB}	—	7,5	—	MHz
α_{rel} ≤3 dB			B_{3dB}	—	8,0	—	MHz
α_{rel} ≤30 dB			B_{30dB}	—	9,4	—	MHz
Relative attenuation			α_{rel}				
		32,32 MHz		–0,1	0,9	1,9	dB
		39,93 MHz		0,4	1,4	2,4	dB
		32,13 MHz		1,5	2,7	3,9	dB
		40,13 MHz		2,3	3,5	4,7	dB
		31,25 MHz		37,0	51,0	—	dB
		47,25 MHz		45,0	60,0	—	dB
Lower sidelobe	25,00 ...	31,25 MHz		35,0	41,0	—	dB
Upper sidelobe	40,90 ...	50,00 MHz		32,0	39,0	—	dB

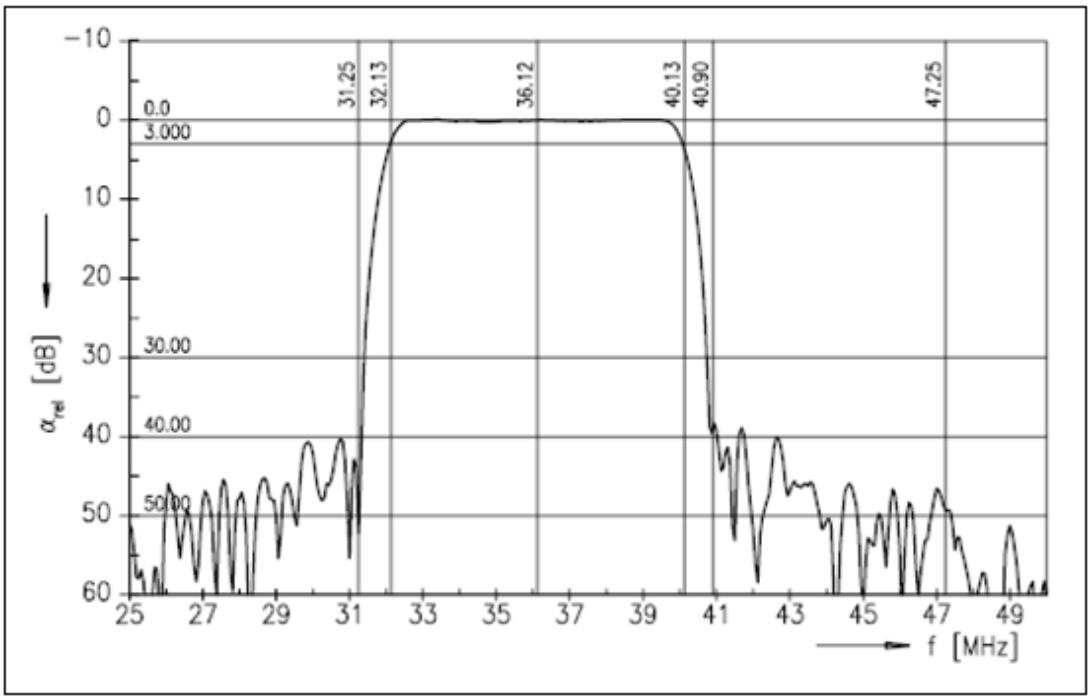

Figure 2.9 Gain response of EPCOS X6966M.

EPCOS X6872D:

Table 2.4 Filter Characteristics of EPCOS X6872D

				min.	typ.	max.	
Center frequency (center between 10 dB points)			f_C	—	36,125	—	MHz
Insertion attenuation			α				
Reference level for the following data		36,13 MHz		18,5	20,0	21,5	dB
Pass bandwith							
α_{rel} ≤3 dB			B_{3dB}	—	6,9	—	MHz
α_{rel} ≤30 dB			B_{30dB}	—	8,5	—	MHz
Relative attenuation			α_{rel}				
		33,08 MHz		—	0,5	—	dB
		39,17 MHz		—	0,6	—	dB
		32,63 MHz		—	3,6	—	dB
		39,63 MHz		—	3,8	—	dB
Lower sidelobe	25,00 ...	31,65 MHz		38,0	46,0	—	
Upper sidelobe	40,65 ...	45,00 MHz		37,0	42,0	—	

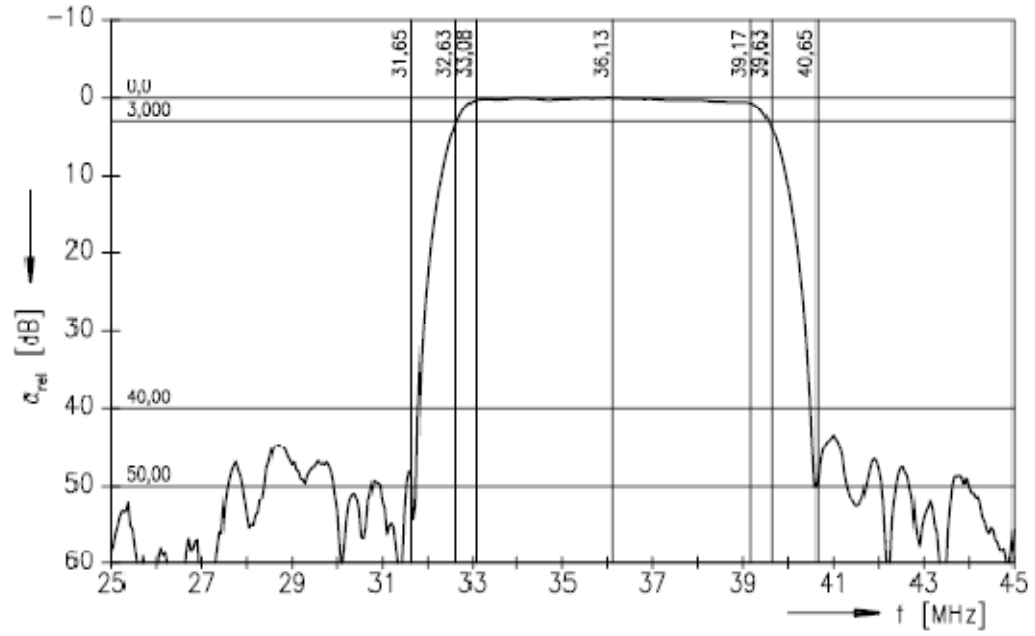

Figure 2.10 Gain response of EPCOS X6872D.

EPCOS X6865D:

Table 2.5 Filter Characteristics of EPCOS X6865D

			min.	typ. @ 25 °C	max.	
Center frequency (center between 3 dB points)		f_C	—	36.125	—	MHz
Insertion attenuation		α				
Reference level for the following data	36.13 MHz		16.1	17.6	19.1	dB
Pass bandwith						
α_{rel} ≤3 dB		B_{3dB}	5.8	6.0	6.2	MHz
α_{rel} ≤30 dB		B_{30dB}	7.4	7.6	7.8	MHz
Relative attenuation		α_{rel}				
	33.59 MHz		–1.1	0.1	1.3	dB
	38.65 MHz		–0.8	0.1	1.6	dB
	33.12 MHz		1.3	2.5	3.7	dB
	39.12 MHz		1.9	3.1	4.3	dB
Lower sidelobe						
25.00 ...	32.12 MHz		38.0	44.0	—	dB
Upper sidelobe						
40.12 ...	41.42 MHz		36.0	40.0	—	dB
41.42 ...	45.00 MHz		38.0	45.0	—	dB

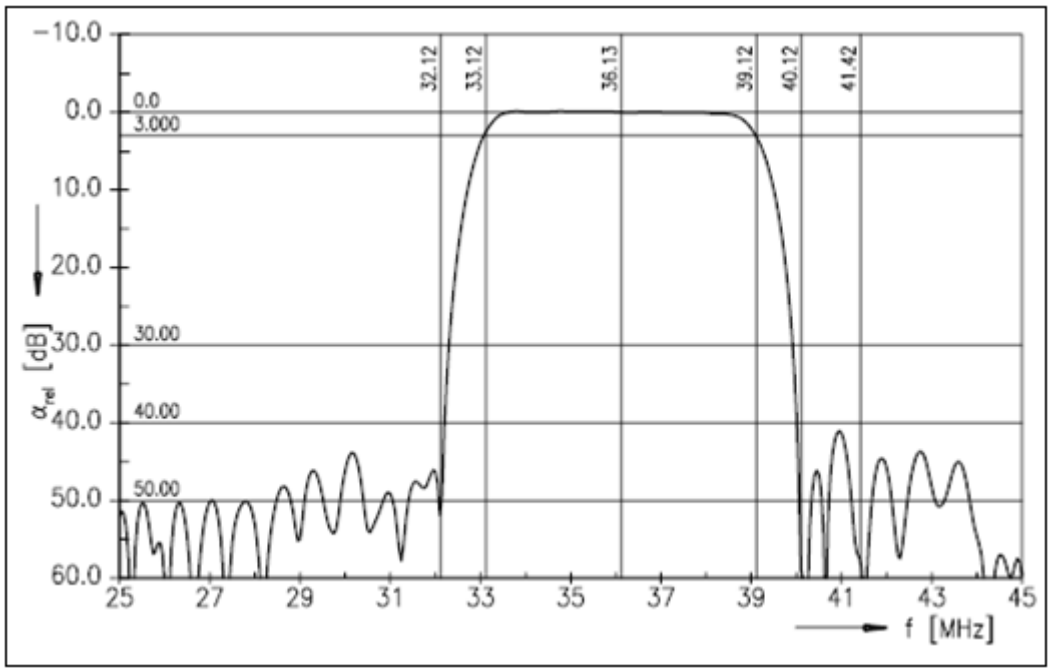

Figure 2.11 Gain response of EPCOS X6865D.

CHAPTER THREE

LOGARITHMIC DOMAIN FILTERS

3.1 Theory of Log- Domain Filters

The log-domain concept was first introduced by Adams in 1979. Interest this area has been started with the introduction of a compounding current-mode integrator and a general state-space strategy for the design of log-domain filters (Adams, 1979).

He demonstrated that an overall linear transfer function could be implemented with a highly nonlinear circuit. Specifically, he showed that one could use the logarithm (specifically, the natural logarithm) of an input signal in a ‘filter’ comprising only diodes, capacitors, current sources and operational amplifiers in such a way as to achieve the log of the linearly filtered response at an output node, which could be subsequently exponentiated to recover the linearly filtered version of the original input.

Generally most of the papers related with this method suffer from the high-frequency limitations of the active elements. However, in recent years, more attention has been given to the integration of high-frequency tunable filters. Gopinathan showed the design of an electronically tunable anti-aliasing filter for use in digital video. (Frey, 1993)

Adam introduced the log-filtering idea with a simple example given in Figure 3.1. An input current is forced through a diode to produce a voltage that is the log of the input. (Frey, 1993)

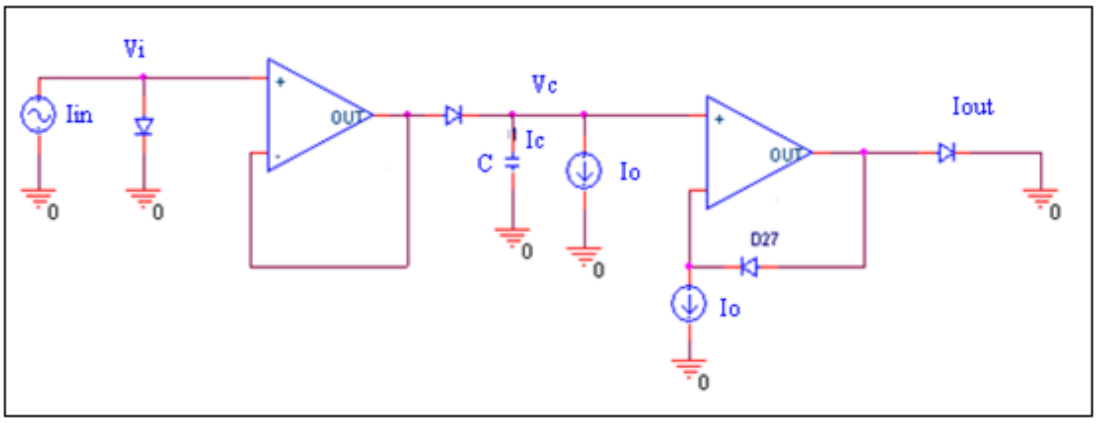

Figure 3.1 Adam's log-domain circuit.

The voltage across the capacitor can be shown to be the natural log of a linear filter function applied to the input. The equations for the filter are derived as follows, where the diodes are assumed to obey the ideal diode law and are in forward bias.

$$V_i = \frac{1}{k}\ln\left(\frac{I_{in}}{I_s}\right) \text{ Where } k = q/kT$$

$$I_c = I_s e^{k[V_i - V_c]} - I_0 = C\frac{dV_c}{dt} = C\dot{V}_c$$

$$I_{out} = I_s e^{k[V_c + (1/k)\ln(I_0/I_s)]} = I_0 e^{kV_c}$$

Combining the above equations yields,

$$C\dot{V}_c e^{kV_c} = -I_0 e^{kV_c} + I_s e^{kV_i}$$

$$= -I_0 e^{kV_c} + I_s(I_{in}/I_s)$$

$$= -I_0 e^{kV_c} + I_{in}$$

If we define $X = e^{kV_c}$

$$C\frac{dX}{dt} + kI_0 X = kI_{in}$$

$$I_{out} = I_o X \Rightarrow \dot{I_{out}} + k\frac{I_0}{C}I_{out} = k\frac{I_0}{C}I_{in}$$

This is a linear differential equation relating the output I_{out} to the input I_{in}, and, hence, the output is a linearly filtered version of the input. It is simple to see that the filter is a one-pole low-pass type with cutoff frequency equal to kI_0/C.

So, the filter is electronically tunable. If the diode looks like a resistor equal to its dynamic impedance $1/kI_0$, the circuit looks like a simple RC filter with cutoff frequency given by $1/RC=1/(1/kI_0)C=kI_0/C$ (Adams, 1979).

3.2 The Basic Log-Domain Building Blocks

The basic log-domain block consists of two NPN and two PNP transistors as shown in Figure 3.2.

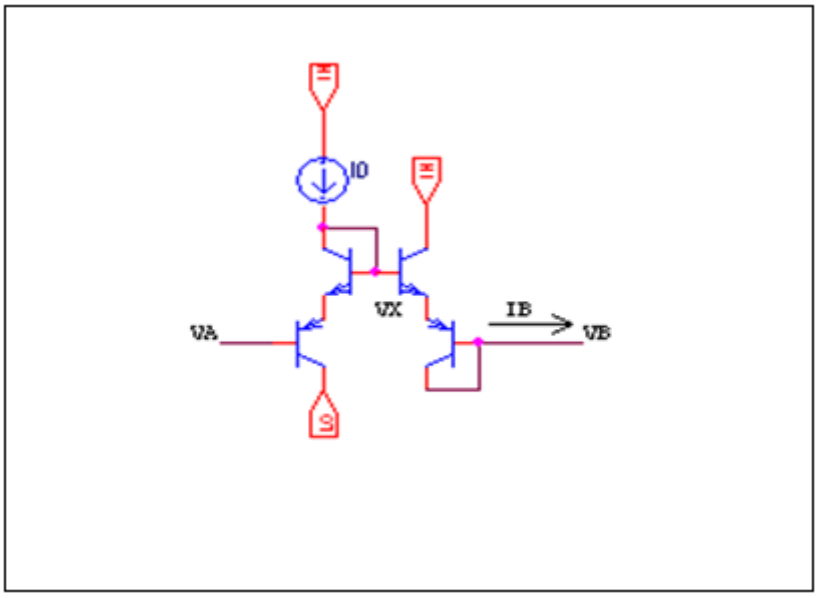

Figure 3.2 The basic log-domain building block.

The output current I_B, which is shown in Figure, can be derived as given below.

$$V_X - V_A = \frac{1}{k}\ln\left(\frac{KI_0}{I_S}\right)$$

$$V_X = V_A + \frac{1}{k}\ln\left(\frac{KI_0}{I_S}\right)$$

$$I_B = I_S e^{k\left[V_A + \frac{1}{k}\ln\left(\frac{KI_0}{I_S}\right) - V_B\right]}$$

$$I_B = I_S e^{k(V_A - V_B)} . e^{k \cdot \frac{1}{k}\ln\left(\frac{KI_0}{I_S}\right)} = KI_0 e^{k(V_A - V_B)} \qquad \text{where } k = \frac{1}{2V_T}$$

$$I_B = KI_0 e^{(V_A - V_B)/2V_T}$$

$$EXP(X) = KI_0 . e^{X/2V_T}$$

Two mathematical inverse operators, LOG and EXP functions are defined as given below and these operations can be accepted as basic building blocks of log-domain cell.

$$EXP(X) = KI_0 . e^{X/2V_T}$$

$$LOG(Y) = 2V_T . \ln\left(\frac{Y}{KI_0}\right)$$

The block diagram of a typical linear system is shown in Figure 3.3. (Perry & Roberts, 1996) For practical reasons exp blocks appear at the input and log blocks appear at the output. Variables marked with circumflex (^) represent signals in the log domain.

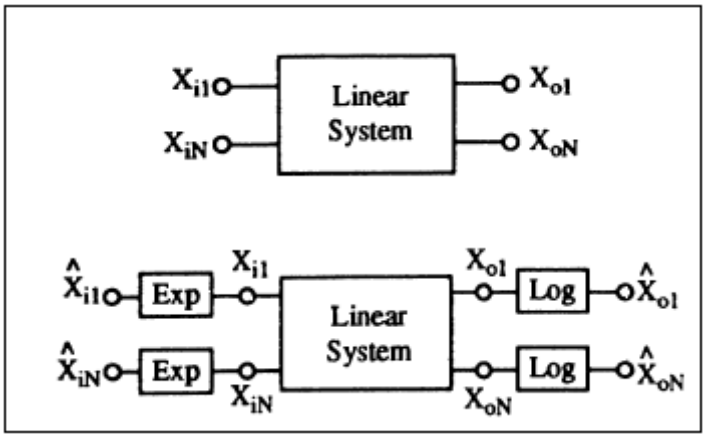

Figure 3.3 Representation of the block diagram of a typical linear system and logarithmic system.

3.3 Log-domain integrator

Log-domain integrators are the smallest and the basic building blocks of log-domain filtering. A log domain cell consists of two NPN, two PNP transistors and a current source. Figure below shows the log-domain cells with opposite polarities.

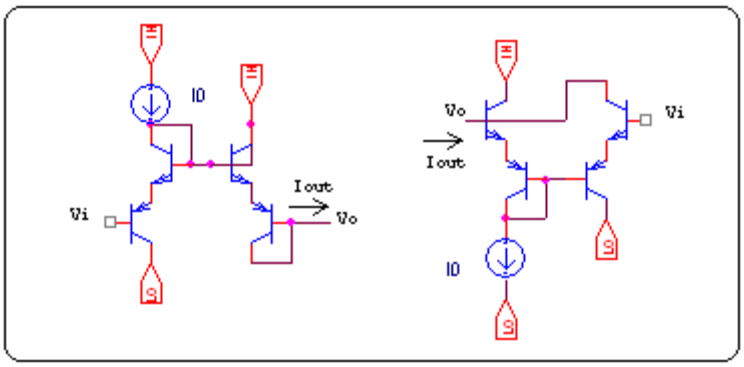

Figure 3.4 Log-domain cells with opposite polarities.

If different integrator pairs are wired as given below by adding a capacitor, the circuit below is obtained. V_a, V_b, and V_0 are positive input, negative input and output respectively.

By applying KCL at node h, a logarithmic equation can be obtained.

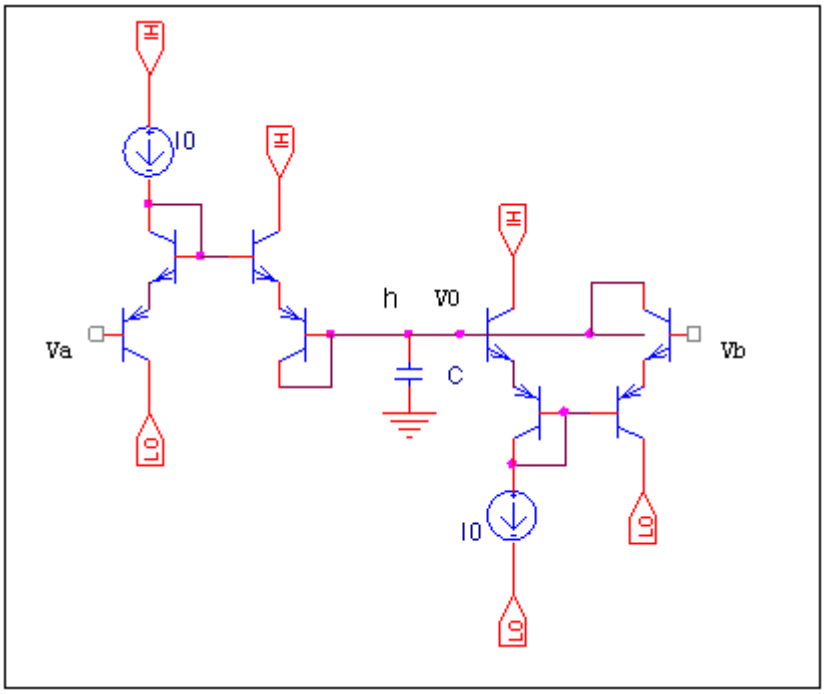

Figure 3.5 Example circuit of log-domain cells with opposite polarities.

$$C\frac{dV_0}{dt} = I_0 e^{\frac{V_a - V_0}{2V_T}} - I_0 e^{\frac{V_b - V_0}{2V_T}}$$

Second step is multiplying the equation by $e^{V_0/2V_T}$ and arranging the equation.

$$\frac{2V_T}{I_0}.C.\frac{d}{dt}\left\{I_0 e^{\frac{V_0}{2V_T}} - I_0\right\} = \left\{I_0 e^{\frac{V_a}{2V_T}} - I_0\right\} - \left\{I_0 e^{\frac{V_b}{2V_T}} - I_0\right\}$$

The result may also be represented as:

$$EXP(V_0) = \frac{I_0}{2V_T}.\frac{1}{C}.\int\{EXP(V_a) - EXP(V_b)\}\,dt$$

Where $EXP(X) = I_0 e^{\frac{X}{2V_T}} - I_0$ and $LOG(X) = 2V_T \ln(\frac{I_0 + X}{I_0})$

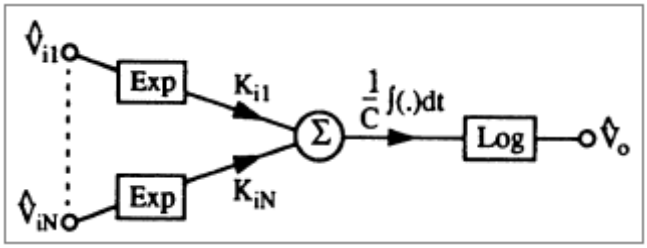

Figure 3.6 The representation as block-diagram.

The last step is symbolical representation of the result by SFG as given in Figure 3.6 (Perry & Roberts, 1996).

3.4 The Damped Integrator

The damped log-domain integrator is shown in Figure 3.7 (Perry & Roberts, 1996). Electronic tenability and damping are important points of logarithmic domain. After the system has introduced to log-domain, $\hat{V}_{i_n}$ became inputs. After the EXP and summing operations, the output is a voltage at the logarithmic system by using LOG operation.

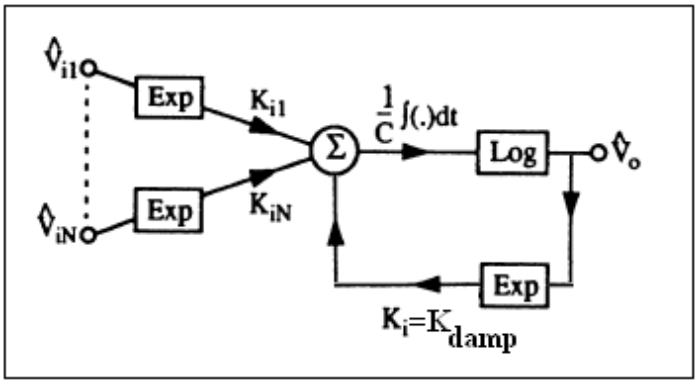

Figure 3.7 Block-diagram representation of damped integrator.

The circuit shown in Figure 3.8 is the suitable electronic circuit that can be offered for the SFG drawn in Figure 3.7. (Perry & Roberts, 1996)

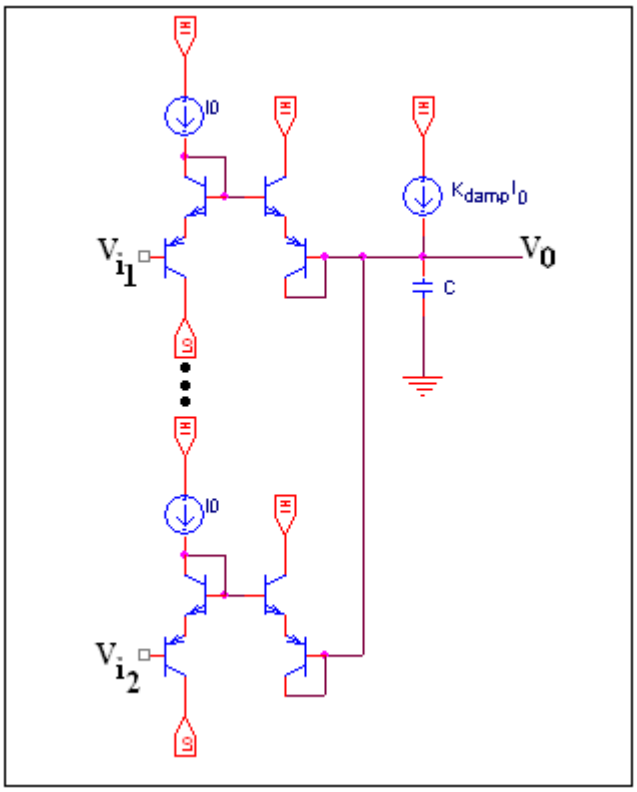

Figure 3.8 Damped integrator circuit.

3.5 Input and Output Stages

As mentioned before, a LOG block must be placed at the input and an EXP block must be placed at the output of the system. This is needed for the overall linearity of the system. An input stage which is a LOG cell converts the linear current input to logarithmic voltage. Next stage is the main log-domain circuit which is placed in order to realize the filtering function. The resulting log-domain output voltage is converted to a linear current at the final stage. This is not different than an EXP cell.

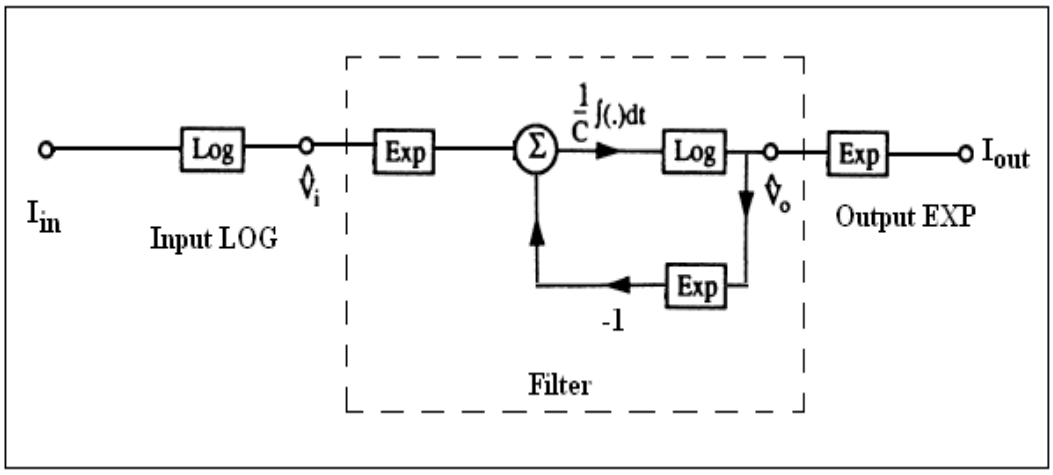

Figure 3.9 Block-diagram representation of a log domain circuit including input and output stages.

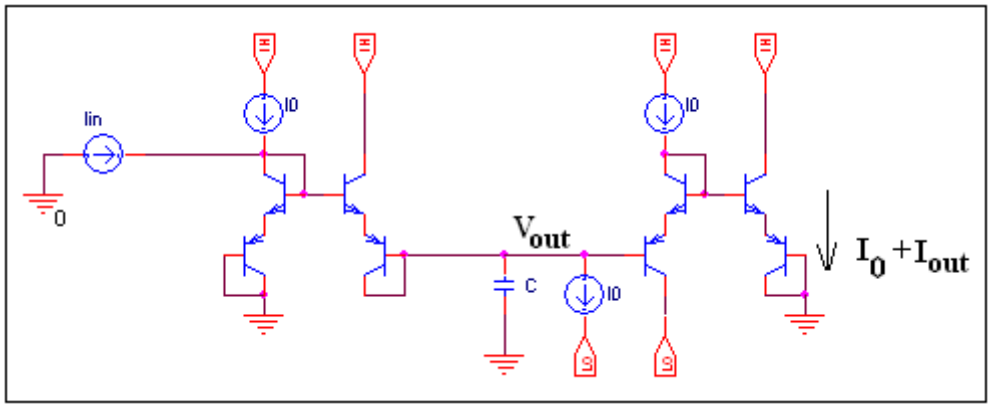

Figure 3.10 Log domain circuit including input and output stages.

A first-order filter example is given in Figure 3.10. The input current I_{in} is firstly converted to a logarithmic voltage and then a damped integrator performs a filtering operation. Finally $\hat{V}_o$ which is the output of the circuit is converted to a linear current.

The node equation can be written as:

$$C\frac{d\hat{V}_{out}}{dt} = (I_0 + I_{in}).e^{\frac{-\hat{V}_{out}}{2V_T}} - I_0$$

CHAPTER FOUR

LOG-DOMAIN FILTER SYNTHESIS BY USING SIGNAL FLOW GRAPH METHOD

4.1 Design Steps of The Method

This chapter describes the signal flow graph (SFG) method. The signal flow graph is a method that also used to synthesize active filters from LC ladders.

Transforming a linear network into logarithmic domain and get a log-domain network by using SFG method has some design steps which are shown below.

1) Determine an LC ladder circuit that can be used as a reference.
2) Determine KVL and KCL equations of the reference circuit.
3) Generate the signal flow graph of the reference circuit with respect to KVL and KCL equations.
4) Place a LOG block after each integrator.
5) Place an EXP block at the input to each summer (before multiplier).
6) Place an EXP block at the output.
7) Place a LOG block at the input.
8) Replace the integrator branches of the log-domain SFG with log-domain integrator circuits.

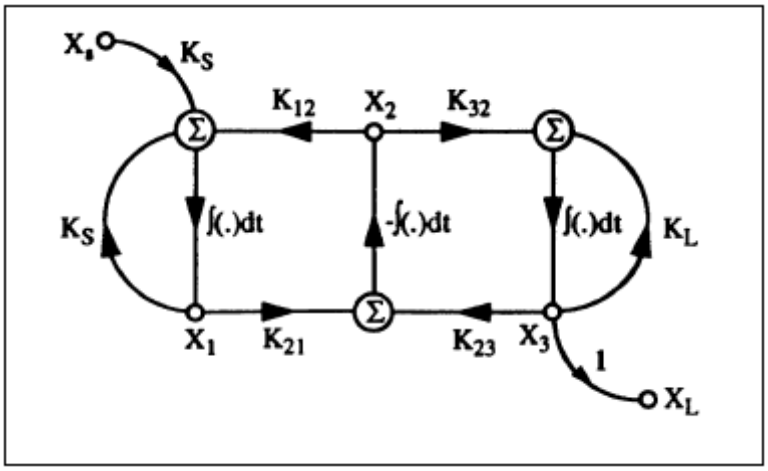

Figure 4.1 An example of an SFG representation.

An SFG of an LC ladder like Figure 4.1 (Perry & Roberts, 1996) above should be converted to another SFG, but this time to log-domain one. It is obvious to see that this process can easily be completed by using the steps given above. By the way the SFG at the log domain is given in Figure 4.2 (Perry, 1996).

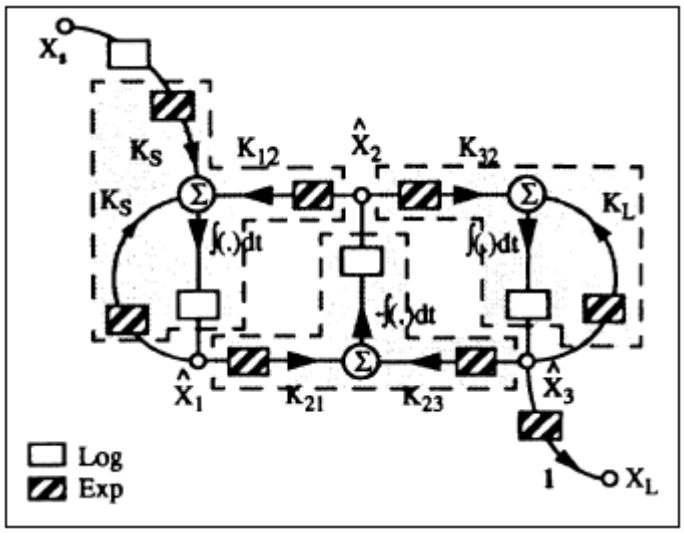

Figure 4.2 SFG representation in logarithmic system.

4.2 The Design of A Fifth Order Chebyshev Low Pass Filter

The Chebyshev filter which has cut off frequency of 100 kHz and ripple width 1dB is given as below. The circuit is an LC ladder that is suitable to the first item of the design steps.

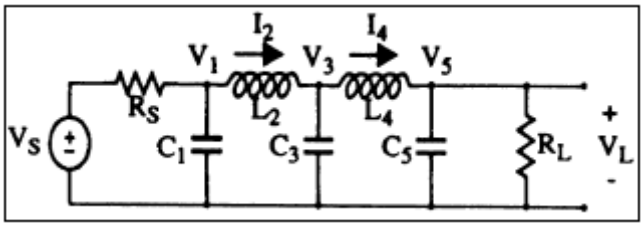

Figure 4.3 A fifth order Chebyshev filter.

According to the circuit theory, there are five unknowns, which are V_1, V_3, V_5, I_2, and I_4. So, five different Kirchhoff current and voltage equations are determined and given below (Perry & Roberts, 1996).

$$C_1 \frac{d}{dt} V_1 = \frac{V_S - V_1}{R_S} - I_2$$

$$C_3 \frac{d}{dt} V_3 = I_2 - I_4$$

$$C_5 \frac{d}{dt} V_5 = I_4 - \frac{V_5}{R_L}$$

$$L_2 \frac{d}{dt} I_2 = V_1 - V_3$$

$$L_4 \frac{d}{dt} I_4 = V_3 - V_5$$

Third step emphasizes generating the linear signal flow graph of the circuit with respect to acceptable KVL and KCL equations that are determined at the second step. The linear SFG that has not converted to log-domain yet, is given below (Perry & Roberts, 1996). Design steps given at the beginning of the chapter are applied.

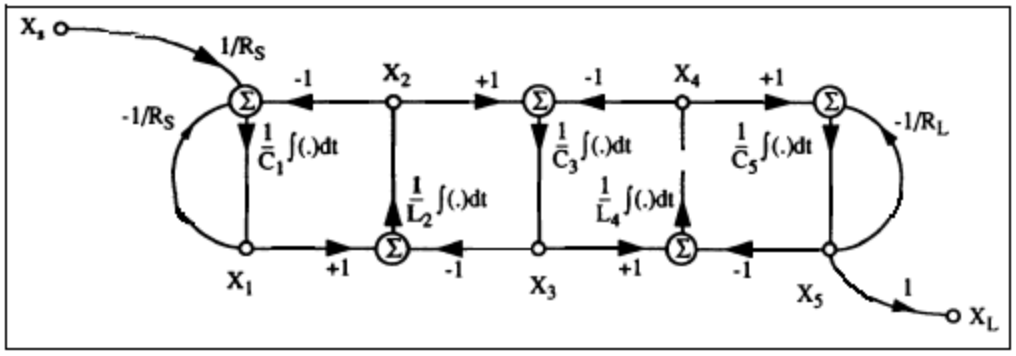

Figure 4.4 Linear SFG of fifth order Chebyshev filter.

Steps 4-7 are completely related with the log-domain transformation of a linear system. LOG blocks are added after each integrator and at the input of the system, while EXP blocks are added at the input of each summer and at the output of the system. The log-domain signal flow graph is obtained and given in Figure 4.5 (Perry, 1996).

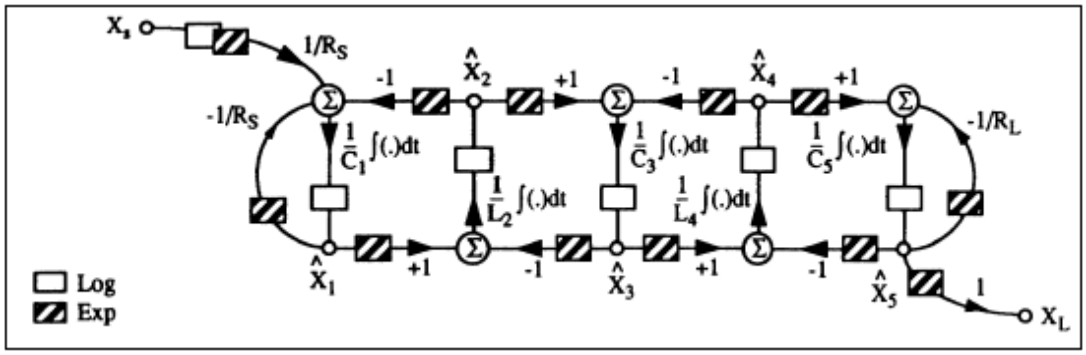

Figure 4.5 Log-domain signal flow graph of fifth order Chebyshev filter.

Here the important point is the conversion of the unknown variables of V_1, V_3, V_5, I_2, V_S, V_L and I_4 as $\widehat{X_1}$, $\widehat{X_3}$, $\widehat{X_5}$, $\widehat{X_2}$, $\widehat{X_S}$, $\widehat{X_L}$, $\widehat{X_4}$, respectively.

The signal flow chart given above helps to constitute a real circuitry. Realization of LOG and EXP circuits that are given in previous chapter should be used. There are also some simplifications like input and output stage. Each node at the circuit should be parallel to SFG. For example $\widehat{X_3}$ is equal to a positive EXP circuit which is coming from node $\widehat{X_2}$, a negative EXP circuit which is coming from node $\widehat{X_4}$, and a derivation component which is a capacitor. If each node is constructed due to this idea, a log-domain circuit given in Figure 4.6 (Perry & Roberts, 1996) is determined. Another important point is the capacitor values that would be used in the log-domain.

The scaling factor $I_0/2V_T$ is necessary to maintain the equivalence between the integrator and original LC ladder component values.

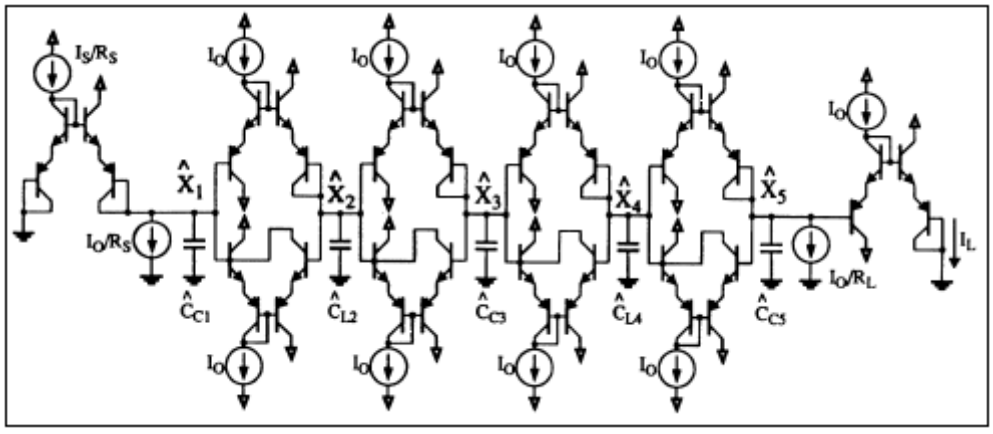

Figure 4.6 Log-domain resultant circuit equivalent to fifth-order Chebyshev filter.

4.3 Modelling A 6th-Order Bandpass Filter by Using Log-Domain Synthesis

The electrical characteristics of an SAW filter can be modelled by a circuit that is shown in Figure 4.7. This circuit is designed as sixth-order Chebyshev filter.

The capacitors and inductors used in the design are given as C_1=41.0421nF, L_1=0.425nH, C_2=0.3821nF, L_2=45.654nH, C_3=41.0421nF, and L_3=0.425nH. ORCAD simulation results are given in Figure 4.8.

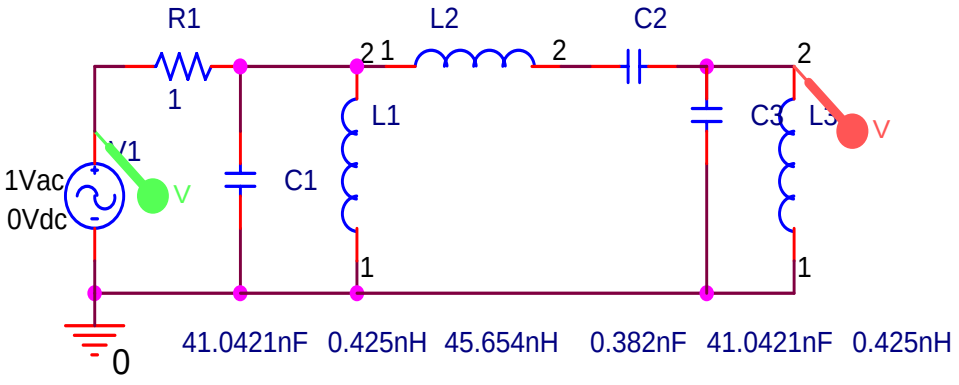

Figure 4.7 An SAW filter model.

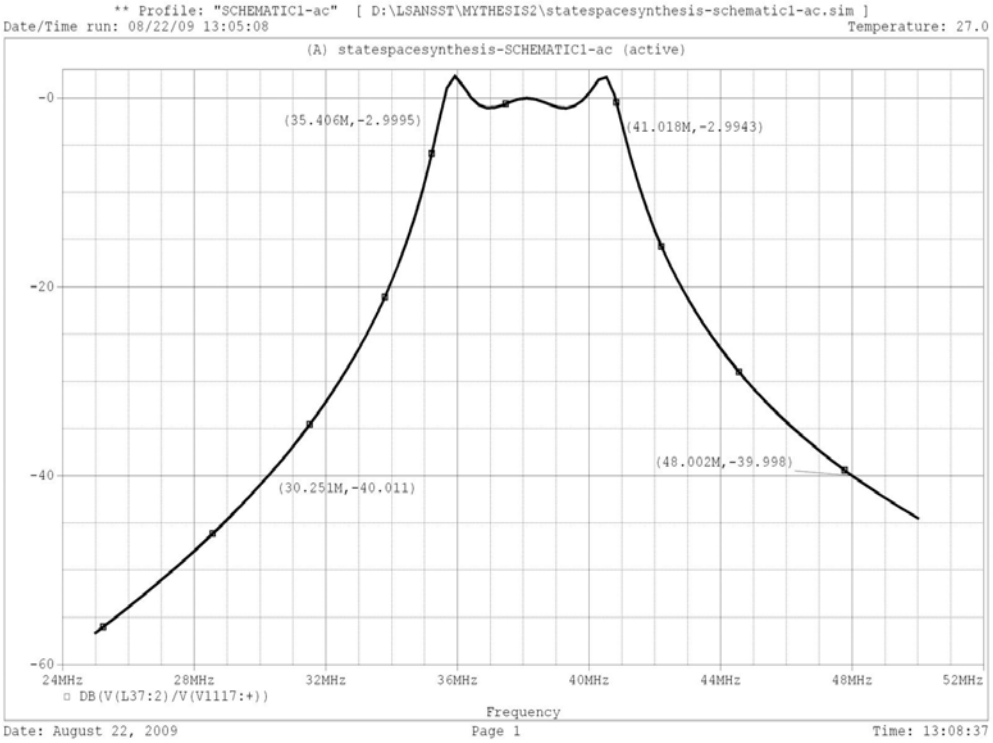

Figure 4.8 Gain response of modelled SAW filter.

The second step is specifying the SFG of the circuit by using nodal analysis. A six order Chebyshev band-pass filter can be represented as shown in Figure 4.9. There are three voltage variables V_1, V_2, V_3 and three current variables I_4, I_5, I_6.

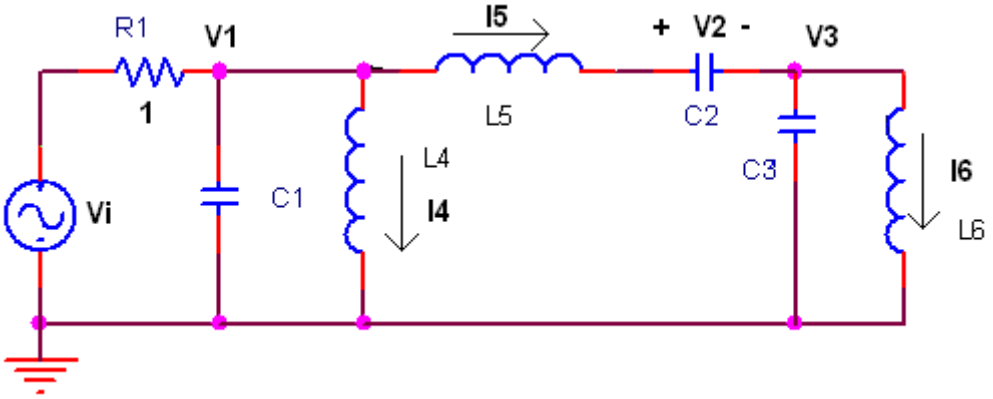

Figure 4.9 Nodal analyses.

Six equations, which are derived from Figure 4.9 with respect to Kirchhoff's voltage law and Kirchhoff's current law, are given below.

$$V_1 = \frac{1}{c_1}\int \left(\frac{V_i - V_1}{1} - I_4 - I_5\right) dt$$

$$I_4 = \frac{1}{L_4}\int (V_1) dt$$

$$V_2 = \frac{1}{c_2}\int (I_5) dt$$

$$I_5 = \frac{1}{L_5}\int (V_1 - V_2 - V_3)\, dt$$

$$V_3 = \frac{1}{c_3}\int \left(I_5 - I_6 - \frac{V_3}{1}\right) dt$$

$$I_6 = \frac{1}{L_6}\int (V_3) dt$$

This set of equations completely characterizes the chosen LC ladder circuit. In order to adjust the gain of filter, scaling factor can be written as shown below.

$$V_{out} = 2V_3$$

The set of equations can be represented as shown in Figure 4.10. This is the linear SFG of the LC ladder circuit.

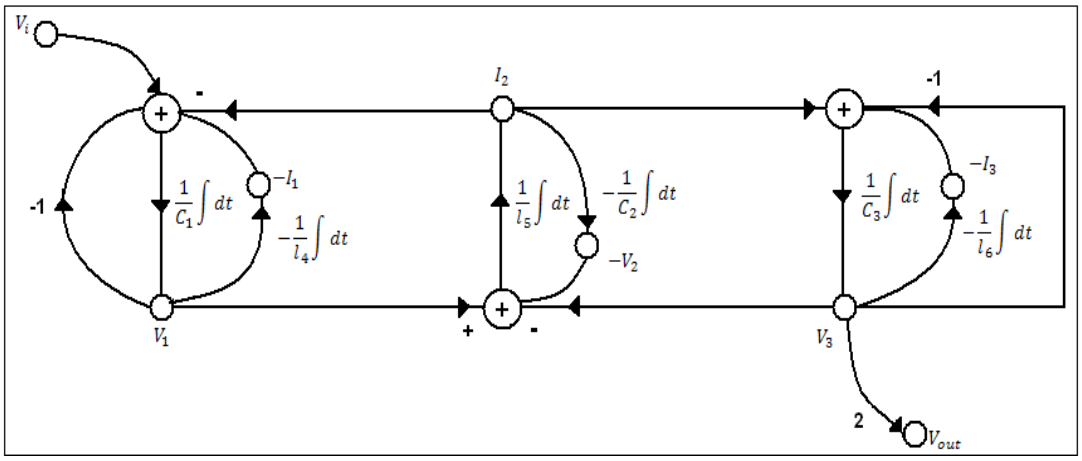

Figure 4.10 Linear SFG drawn with respect to node equations.

Next step is the mapping of variables and introducing to logarithmic domain. After the mapping shown below is made, the log-domain SFG, which is shown in Figure 4.11, is achieved.

$V_i \leftrightarrow X_i$ $V_1 \leftrightarrow X_1$ $-I_4 \leftrightarrow X_2$ $I_5 \leftrightarrow X_3$

$-V_2 \leftrightarrow X_4$ $V_3 \leftrightarrow X_5$ $-I_6 \leftrightarrow X_6$ $V_{out} \leftrightarrow X_{out}$

Each LOG block is placed after integrator; each EXP block is placed at the input to summer. Finally at the output of the system an EXP block is placed and at the input to the system a LOG block is placed.

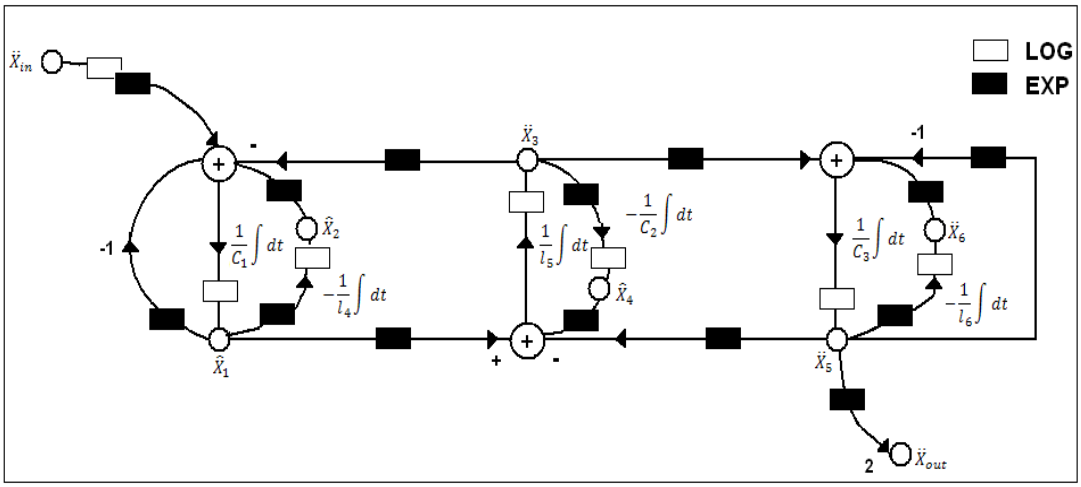

Figure 4.11 SFG converted to Logarithmic domain.

The final circuit can be achieved by replacing each part of the log-domain SFG with its circuit, and eliminating redundant log-cells. The capacitor values that should be used in the circuit are calculated as shown below. Figure 4.12 shows the inverting and non-inverting log domain cells.

$$\{C_1, C_2, \dots, C_6\} = \frac{I_0}{2V_T}\{c_1,\ c_2, c_3, I_4, I_5, I_6\}$$

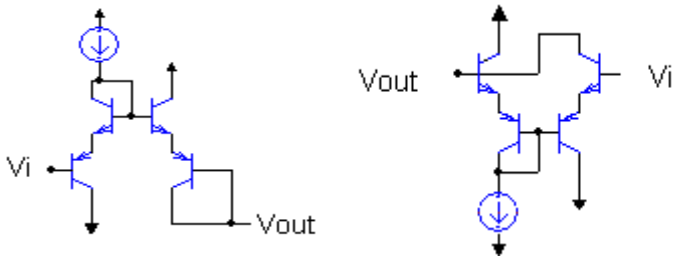

Figure 4.12 Inverting and non-inverting log domain cells.

By using the capacitor and inductor values of LC circuit and formula given above, C_1, C_2… C_6 values are obtained where I_0 and V_T are chosen as 100µA, 25mV, respectively.

The log-domain equivalent capacitor values and the component values that are drawn from are given in Table 4.1.

Table 4.1 LC values in linear domain and equivalent logarithmic domain system

LC ladder circuit	***Log-domain equivalent***
$C_1=41.0421nF$	$C_1=82.1pF$
$L_1=0.425nH$	$C_2=0.85pF$
$L_2=45.654nH$	$C_3=91.31pF$
$C_2=0.3821nF$	$C_4=0.764pF$
$C_3=41.0421nF$	$C_5=82.1pF$
$L_3=0.425nH$	$C_6=0.85pF$

The log-domain equivalent circuit is finalized as shown in Figure 4.13. If we assume ideal elements with no ohmic resistances, zero base current, and perfect diode relationship, the resultant filter will also be ideal.

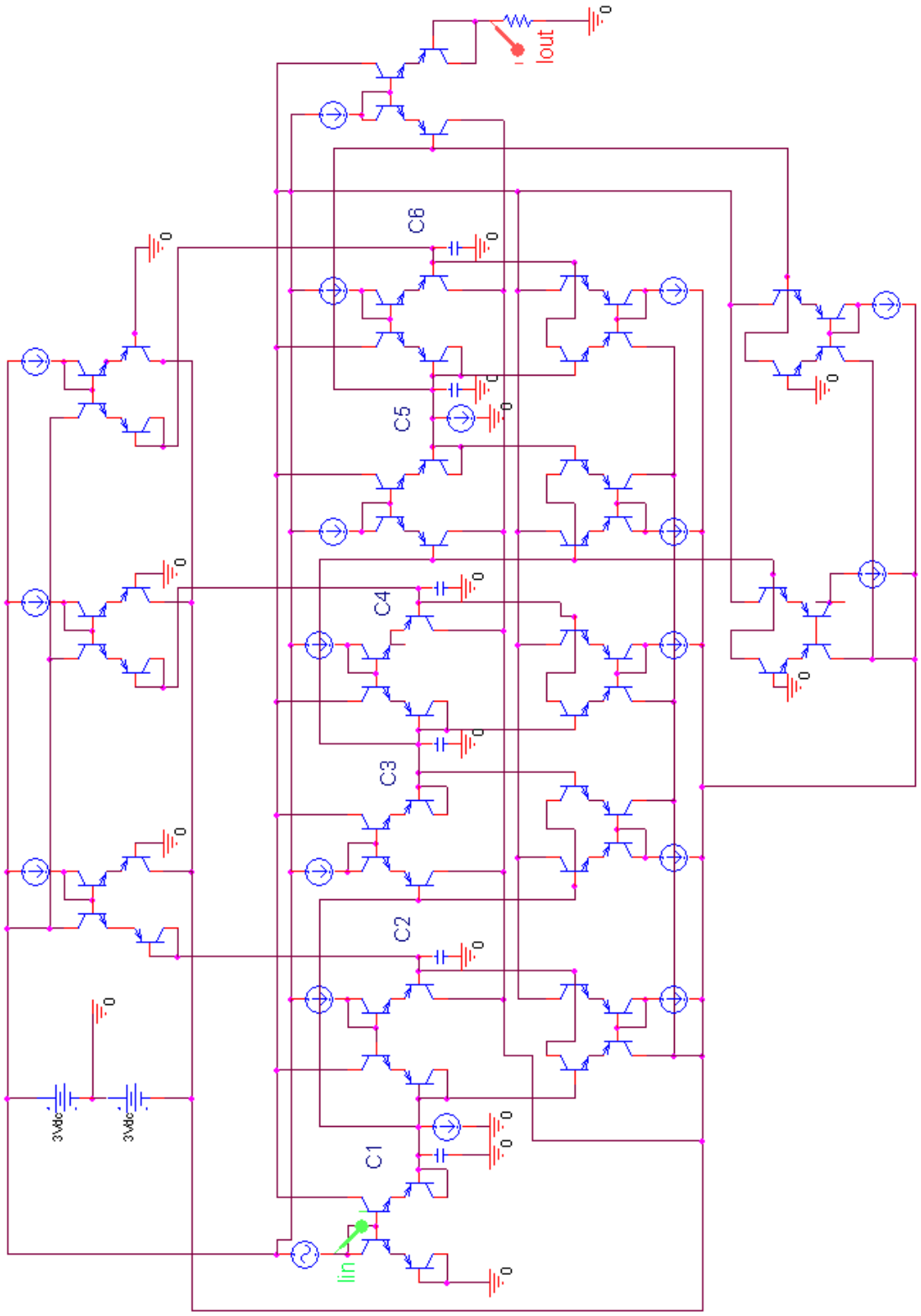

Figure 4.13 Resultant log-domain filter equivalent to model SAW filter.

The proposed resultant circuit is first simulated for ideal transistor parameters (BF=10000) and then for AT&T CBIC-U2 library (APPENDIX A), respectively. The capacitor values are calculated above, the simulation result are shown in Figure 4.14.

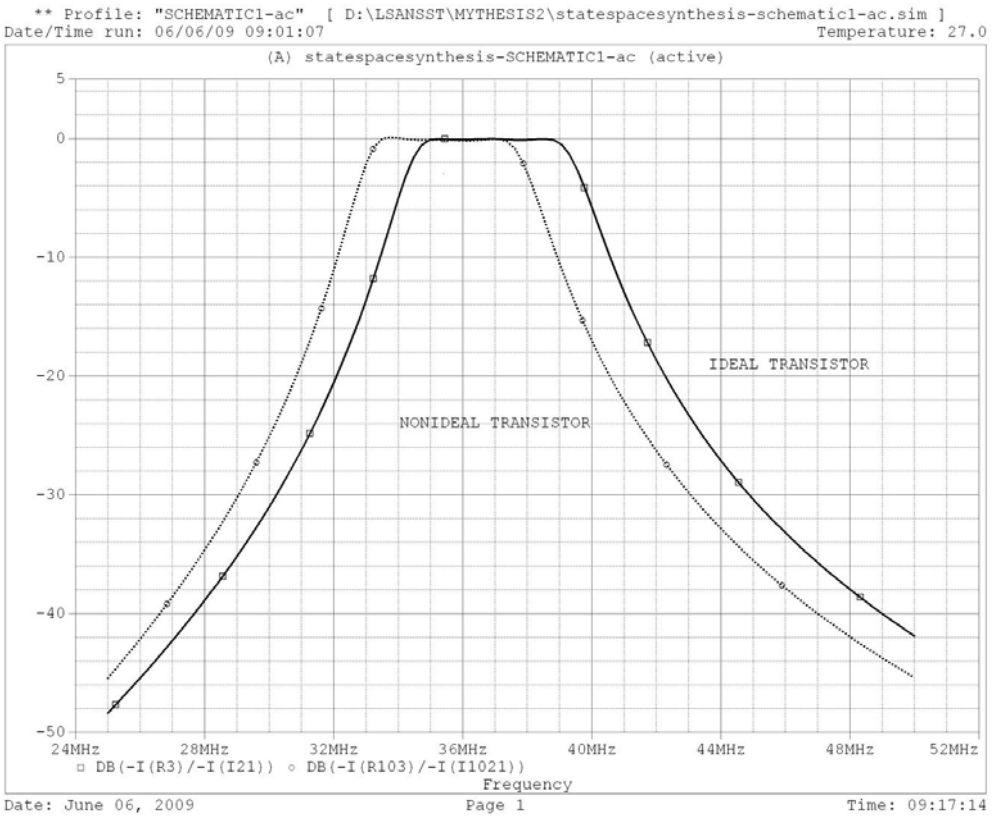

Figure 4.14 Gain responses of ideal and AT&T CBIC-U2 library transistors.

Tunability is another important advantage of a log-domain filtering. For signal flow graph method we are able to shift the frequency response of the filter by increasing or decreasing the current value. Simulation is repeated for 90μA, and 110μA and all results are given in figure 4.15.

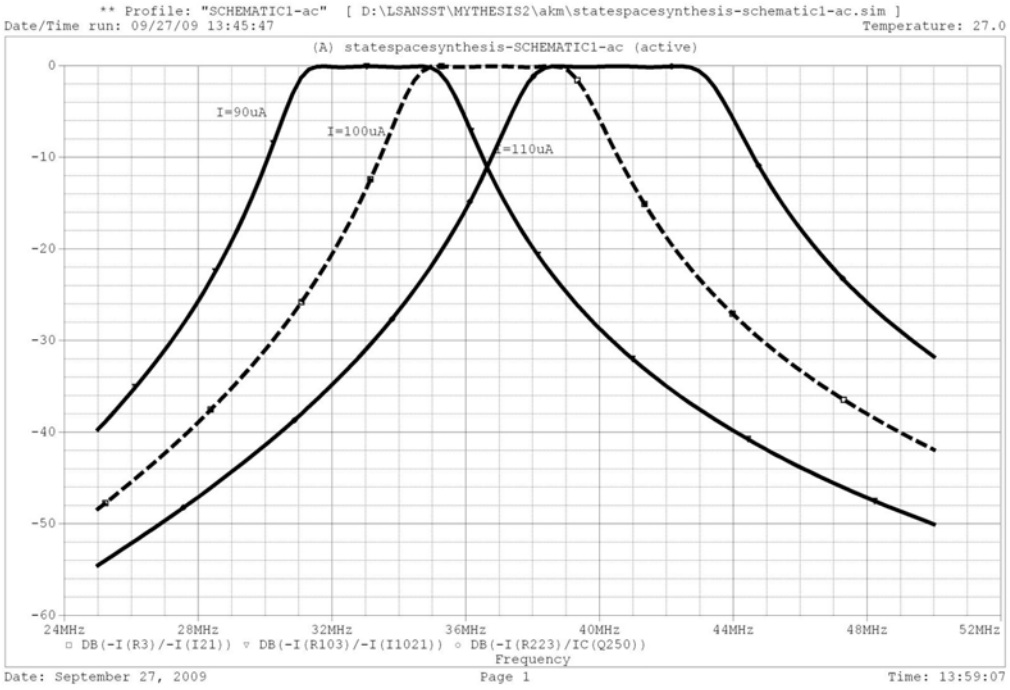

Figure 4.15 Simulation results for I=90μA, 100μA, and 110μA.

CHAPTER FIVE

LOG-DOMAIN FILTER SYNTHESIS BY USING STATE-SPACE SYNTHESIS TECHNIQUE

5.1 Design Steps of The Method

Transforming a linear network into logarithmic domain and get a log-domain network by using state space synthesis method has some design steps which are shown below.

1) Determine an LC ladder circuit that can be used as a reference.
2) Determine KVL and KCL equations of the reference circuit.
3) Generate the transient matrices and write circuit formulation of the reference network by combining and rewriting KVL and KCL equations.
4) Normalize the circuit formulation and stay upper edge of the passband region to 1 rad/sec.
5) Determine A, b, c, and d matrices from transient matrices.
6) Writing State-space formulation with respect to A, b, c, and d matrices.
7) Denormalize the matrices and create current matrices.
8) Place the integrator blocks with respect to matrices.

5.2 The Design of A Third-Order Chebyshev Low Pass Filter

A third order elliptic low-pass LC ladder circuit is given in Figure 5.1 (Roberts, 2002). Capacitor and inductor values are also given as C1= C3=0.2647µF, C2=0.0480µF, L2=0.1197µF. The filter has a cut-off frequency of 1MHz.

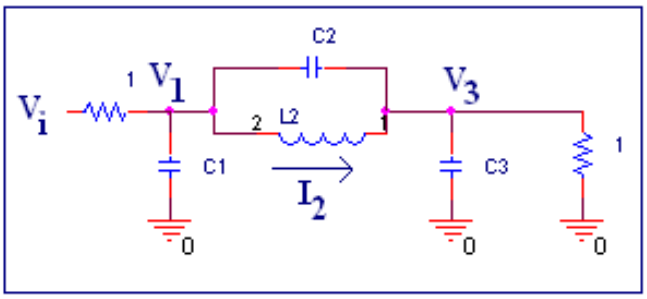

Figure 5.1 A third order elliptic low-pass LC ladder circuit.

After choosing a reference circuit, applying Kirchhoff voltage and current laws is the first step to be done.

$$sC_1V_{C_1} + sC_2(V_{C_1} - V_{C_3}) + I_{L_2} + \frac{V_{C_1} - V_i}{R_S} = 0$$

$$sC_3V_{C_3} - sC_2(V_{C_1} - V_{C_3}) - I_{L_2} + \frac{V_{C_3}}{R_L} = 0$$

$$sL_2I_{L_2} - V_{C_1} + V_{C_3} = 0$$

$$V_{OUT} = V_{C_3}$$

The circuit equations should be combined and rewritten as matrix formation as denoted at third step.

$$s\begin{bmatrix}(C_1+C_2) & 0 & -C_2\\ 0 & L_2 & 0\\ -C_2 & 0 & (C_2+C_3)\end{bmatrix}\begin{bmatrix}V_{C_1}\\ I_{L_2}\\ V_{C_3}\end{bmatrix} + \begin{bmatrix}\left(\frac{1}{R_S}\right) & 1 & 0\\ -1 & 0 & 1\\ 0 & -1 & \left(\frac{1}{R_L}\right)\end{bmatrix}\begin{bmatrix}V_{C_1}\\ I_{L_2}\\ V_{C_3}\end{bmatrix} = \begin{bmatrix}\left(\frac{1}{R_S}\right)\\ 0\\ 0\end{bmatrix}V_i$$

$$V_{OUT} = \begin{bmatrix}0 & 0 & (2\sqrt{\frac{R_S}{R_L}})\end{bmatrix}\begin{bmatrix}V_{C_1}\\ I_{L_2}\\ V_{C_3}\end{bmatrix} + 0$$

Three matrices in the equation above are defined as C, G and W that are:

$$C = \begin{bmatrix} (C_1 + C_2) & 0 & -C_2 \\ 0 & L_2 & 0 \\ -C_2 & 0 & (C_2 + C_3) \end{bmatrix} \quad G = \begin{bmatrix} \left(\frac{1}{R_S}\right) & 1 & 0 \\ -1 & 0 & 1 \\ 0 & -1 & \left(\frac{1}{R_L}\right) \end{bmatrix} \quad W = \begin{bmatrix} \left(\frac{1}{R_S}\right) \\ 0 \\ 0 \end{bmatrix}$$

$$c^T = \begin{bmatrix} 0 & 0 & (2\sqrt{\frac{R_S}{R_L}}) \end{bmatrix} \qquad d = 0$$

There are two ways of applying fourth step. First is normalizing the capacitor and inductor values and other one is normalizing the C matrix which includes capacitor and inductor values.

$$C_{norm} = 2\pi * 1 * 10^6 \begin{bmatrix} (C_1 + C_2) & 0 & -C_2 \\ 0 & L_2 & 0 \\ -C_2 & 0 & (C_2 + C_3) \end{bmatrix}$$

$$= \begin{bmatrix} 1.9648 & 0 & -0.3016 \\ 0 & 0.7521 & 0 \\ -0.3016 & 0 & 1.9648 \end{bmatrix}$$

If we have C, G and W matrices as above, circuit equation can be rewritten in the form,

$$[sC + G]X = WV_i$$

This new form can be rearranged as

$$sX = -C^{-1}GX + C^{-1}WV_i$$

The state space formulation can shortly be represented as

$$sX = AX + bV_i$$

Where the state matrices A and b are respectively given by

$$A = -C^{-1}G \text{ And } b = C^{-1}W$$

Determining A, b, c and d matrices is the fifth step of the method.

$$A = -C^{-1}G = \begin{bmatrix} -0.5213 & -0.4412 & -0.0800 \\ -1.3296 & 0 & -1.3296 \\ -0.0800 & -0.4412 & -0.5213 \end{bmatrix}$$

$$b = C^{-1}W = \begin{bmatrix} 0.5213 \\ 0 \\ 0.08 \end{bmatrix}$$

$$c = \begin{bmatrix} 0 \\ 0 \\ 2 \end{bmatrix} \text{ And d=0}$$

Due to the limitation of log-domain implementations, it is required that non-zero parameters of the b vector should be equal. Unfortunately, this is not the case. To overcome this problem, the transposed state-space system can be employed. Transposed state-space system can easily be converted as below.

$$A^T = (-C^{-1}\,G)^T = \begin{bmatrix} -0.5213 & 1.3297 & -0.0800 \\ -0.4412 & 0 & 0.4412 \\ -0.0800 & -1.3297 & -0.5213 \end{bmatrix}$$

$$b = \begin{bmatrix} 0 \\ 0 \\ 2 \end{bmatrix} \qquad c = \begin{bmatrix} 0.5213 \\ 0 \\ 0.08 \end{bmatrix}$$

Next step is creating the current matrices. Denormalizing operation should also be applied at this step. Thus, a bias current can be defined as below:

$$I_0 = (2V_T C)2\pi f_C$$

Where V_T is thermal voltage f_C is cut-off frequency and $2\pi f_C$ is denormalizing factor. In this example, 10pF capacitor and 100MHz cut-off frequency is chosen. Current matrices are determined as below by these values.

$$A_I = I_0.\begin{bmatrix} -0.5213 & 1.3297 & -0.0800 \\ -0.4412 & 0 & 0.4412 \\ -0.0800 & -1.3297 & -0.5213 \end{bmatrix}$$

$$= \begin{bmatrix} -163.73 & 364.59 & -32.71 \\ -158.78 & 0 & 206.55 \\ -19.33 & -280.28 & -163.73 \end{bmatrix} \mu A$$

$$b_I = b.I_0 = \begin{bmatrix} 0 \\ 0 \\ 628 \end{bmatrix} \mu A$$

$$c_I = c.I_0.\begin{bmatrix} 0.5213 \\ 0 \\ 0.08 \end{bmatrix} = \begin{bmatrix} 251.73 \\ 0 \\ 50.29 \end{bmatrix} \mu A$$

The last step is to constitute log-domain circuit with respect to matrices above. In order to avoid from complexity, square blocks are used. Each block represents a multiple input integrator.

The integrator that will be used in this synthesis method and its symbolic representation are given in figure below.

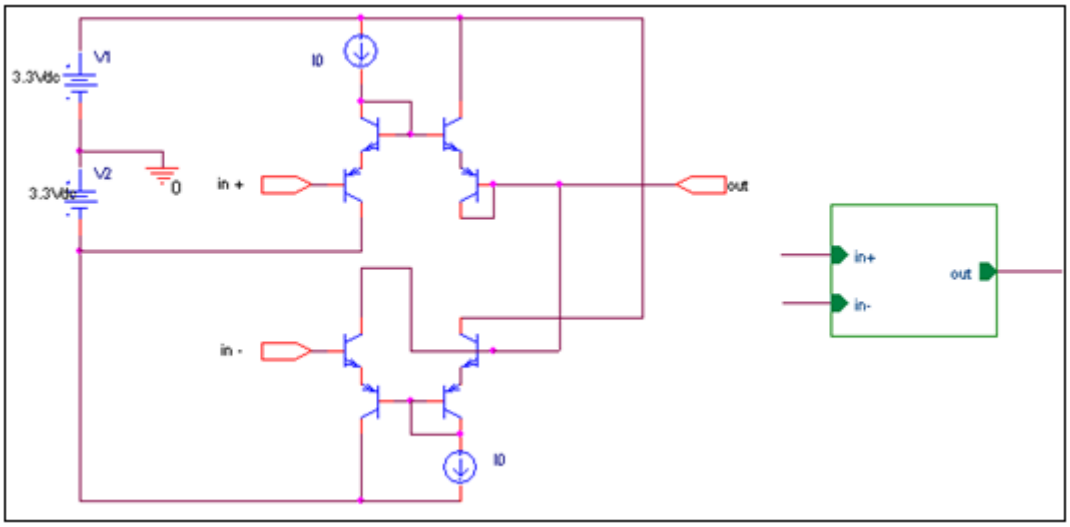

Figure 5.2 Integrator used in the method and its representation.

b_I matrix is used as input of the system, A_I matrix is current filtering section in logarithmic system and c_I is the output matrix where the filtered current is converted to linear system.

There are sub-steps for constituting the log-domain circuit easily.

1) For each element of the A_I matrix, a block is placed.
2) Outputs of the same row elements of the A_I matrix are wired vertically and ended with a 10pF capacitor that is chosen at design step.
3) Inputs of the same column elements of the A_I matrix are wired together with respect to the sign of the element. Positive elements use positive input and negative elements use negative inputs. Other input should be wired to ground.
4) The same numbered columns and rows should be wired.
5) Output of the elements of b_I matrix should be wired with respect to their row number.

6) Input of the elements of c_I matrix should be wired with respect to their row number and their sign.

If the steps given above are applied to current example, the circuit below is obtained.

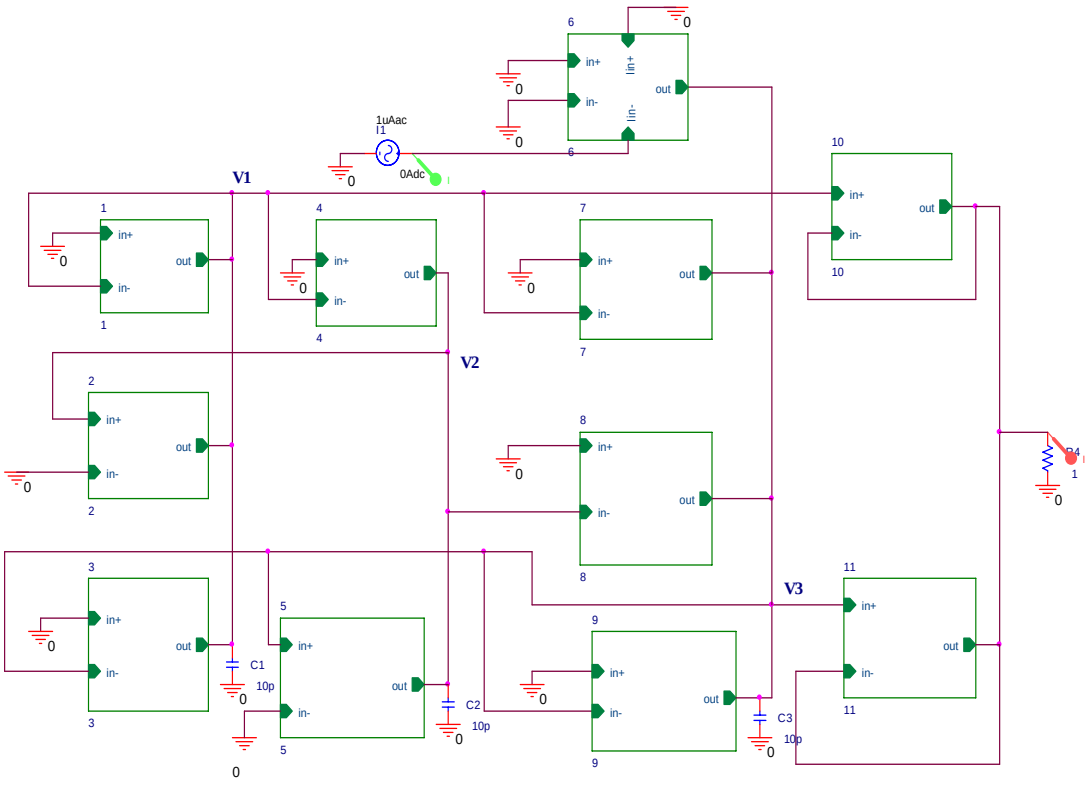

Figure 5.3 Resultant log-domain circuit equivalent to third order Chebyshev filter.

5.3 The Design of a Chebyshev Filter

The sixth-order electrically modelled SAW filter that is given in Chapter 3 is used as a reference LC ladder circuit.

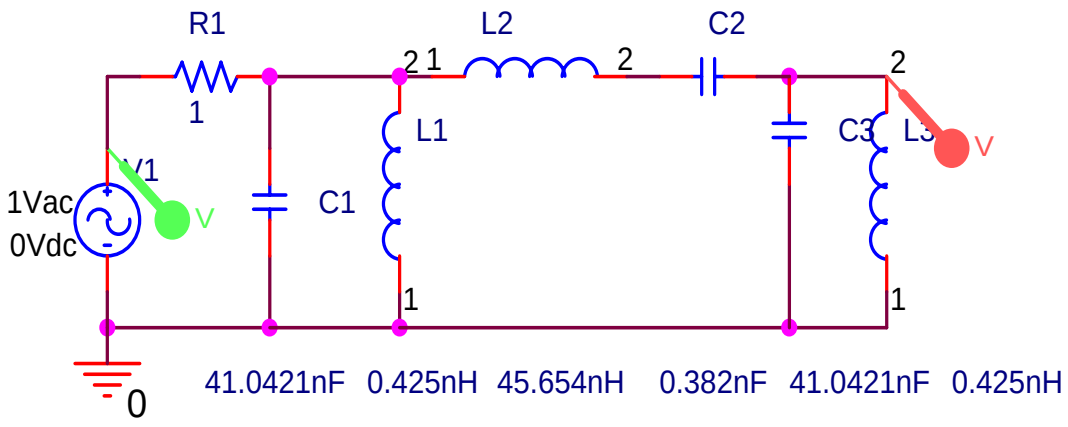

Figure 5.4 Reference SAW filter.

After choosing a reference circuit, applying Kirchhoff voltage and current laws is the first step should be done.

$$\frac{-V_i - V_{C_1}}{R_1} + I_{L_1} + I_{L_2} + \frac{V_{C_1}}{\frac{1}{sC_1}} = 0$$

$$\frac{V_{C_1}}{sL_1} = I_{L_1}$$

$$\frac{V_{C_1} - V_{C_2}}{sL_2} = I_{L_2}$$

$$\frac{V_{C_2} - V_{C_2}}{\frac{1}{sC_2}} = I_{L_2}$$

$$-I_{L_2} + \frac{V_{C_3}}{\frac{1}{sC_3}} + I_{L_3} + \frac{V_{C_3}}{R} = 0$$

$$\frac{V_{C_3}}{sL_3} = I_{L_3}$$

$$y = V_{C_3}$$

If the KVL and KCL equations are arranged,

$$sC_1V_{C_1} + I_{L_1} + I_{L_2} + V_{C_1} = V_{\text{i}}$$

$$sL_1I_{L_1} - V_{C_1} = 0$$

$$sL_2I_{L_2} - V_{C_1} + V_{C_2} = 0$$

$$sC_2V_{C_2} - sC_2V_{C_3} - I_{L_2} = 0$$

$$sC_3V_{C_3} - I_{L_2} + I_{L_3} + V_{C_3} = 0$$

$$sL_3I_{L_3} - V_{C_3} = 0$$

The circuit equations should be combined and rewritten as matrix formation at third step.

$$\text{s}\begin{bmatrix} C_1 & 0 & 0 & 0 & 0 & 0 \\ 0 & L_1 & 0 & 0 & 0 & 0 \\ 0 & 0 & L_2 & 0 & 0 & 0 \\ 0 & 0 & 0 & C_2 & -C_2 & 0 \\ 0 & 0 & 0 & 0 & C_3 & 0 \\ 0 & 0 & 0 & 0 & 0 & L_3 \end{bmatrix}\begin{bmatrix} V_{C_1} \\ I_{L_1} \\ I_{L_2} \\ V_{C_2} \\ V_{C_3} \\ I_{L_3} \end{bmatrix} + \begin{bmatrix} 1 & 1 & 1 & 0 & 0 & 0 \\ -1 & 0 & 0 & 0 & 0 & 0 \\ -1 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & -1 & 0 & 0 & 0 \\ 0 & 0 & -1 & 0 & 1 & 1 \\ 0 & 0 & 0 & 0 & -1 & 0 \end{bmatrix}\begin{bmatrix} V_{C_1} \\ I_{L_1} \\ I_{L_2} \\ V_{C_2} \\ V_{C_3} \\ I_{L_3} \end{bmatrix} = \begin{bmatrix} 1 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} V_i$$

$$y = \begin{bmatrix} 0 & 0 & 0 & 0 & 1 & 0 \end{bmatrix}\begin{bmatrix} V_{C_1} \\ I_{L_1} \\ I_{L_2} \\ V_{C_2} \\ V_{C_3} \\ I_{L_3} \end{bmatrix}$$

C, G, W, c^T, and d matrices with respect to equations above are given below.

$$C = \begin{bmatrix} C_1 & 0 & 0 & 0 & 0 & 0 \\ 0 & L_1 & 0 & 0 & 0 & 0 \\ 0 & 0 & L_2 & 0 & 0 & 0 \\ 0 & 0 & 0 & C_2 & -C_2 & 0 \\ 0 & 0 & 0 & 0 & C_3 & 0 \\ 0 & 0 & 0 & 0 & 0 & L_3 \end{bmatrix} \quad G = \begin{bmatrix} 1 & 1 & 1 & 0 & 0 & 0 \\ -1 & 0 & 0 & 0 & 0 & 0 \\ -1 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & -1 & 0 & 0 & 0 \\ 0 & 0 & -1 & 0 & 1 & 1 \\ 0 & 0 & 0 & 0 & -1 & 0 \end{bmatrix}$$

$$W = \begin{bmatrix} 1 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \qquad c^T = [0 \quad 0 \quad 0 \quad 0 \quad 1 \quad 0]$$

d=0

Next step is normalising the C matrix which includes capacitor and inductor values. Capacitor and inductor values are given below.

C_1=41.0421nF L_1=0.425nH

C_2=0.3821nF L_2=45.654nH

C_3=41.0421nF L_3=0.425nH

$$C_{norm} = 2\pi * 41 * 10^6 \begin{bmatrix} C_1 & 0 & 0 & 0 & 0 & 0 \\ 0 & L_1 & 0 & 0 & 0 & 0 \\ 0 & 0 & L_2 & 0 & 0 & 0 \\ 0 & 0 & 0 & C_2 & -C_2 & 0 \\ 0 & 0 & 0 & 0 & C_3 & 0 \\ 0 & 0 & 0 & 0 & 0 & L_3 \end{bmatrix}$$

$$C_{norm} = \begin{bmatrix} 10.1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0.10 & 0 & 0 & 0 & 0 \\ 0 & 0 & 11.2 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0.09 & -0.09 & 0 \\ 0 & 0 & 0 & 0 & 10.1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0.11 \end{bmatrix}$$

In order to convert the equation to state-space formulation, A, b, c, and d matrices are calculated with respect to equation.

$$A = -C^{-1}G =$$

$$= \begin{bmatrix} -0.0946 & -0.0946 & -0.0946 & 0 & 0 & 0 \\ 9.1337 & 0 & 0 & 0 & 0 & 0 \\ 0.0850 & 0 & 0 & -0.0850 & 0 & 0 \\ 0 & 0 & 10.3099 & 0 & -0.0946 & -0.0946 \\ 0 & 0 & -0.0946 & 0 & -0.0946 & -0.0946 \\ 0 & 0 & 0 & 0 & 9.0275 & 0 \end{bmatrix}$$

$$b = C^{-1}W = \begin{bmatrix} 0.0946 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \qquad c = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 1 \\ 0 \end{bmatrix} \text{ and } \qquad d=0$$

Next step is creating the current matrices. Denormalizing operation should also be applied at this step. Thus, a bias current can be defined as below:

$$I_0 = (2V_T C)2\pi f_C$$

Where V_T is thermal voltage f_C is cut-off frequency and $2\pi f_C$ is denormalizing factor. 20pF capacitor and 40.125MHz cut-off frequency is chosen for this application. Current matrices are determined as below by these values.

$$A_I = A.I_0$$

$$A_I = \begin{bmatrix} -23.85 & -23.85 & -23.85 & 0 & 0 & 0 \\ 2303 & 0 & 0 & 0 & 0 & 0 \\ 21.5 & 0 & 0 & -21.5 & 0 & 0 \\ 0 & 0 & 2600 & 0 & -23.85 & -23.85 \\ 0 & 0 & 23.85 & 0 & -23.85 & -23.85 \\ 0 & 0 & 0 & 0 & 2276 & 0 \end{bmatrix} \mu A$$

$$b_I = b.I_0 = \begin{bmatrix} 23.85 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \mu A \qquad c_I = c.I_0 = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 504 \\ 0 \end{bmatrix} \mu A$$

In order to apply the last step to constitute log-domain circuit with respect to matrices above, sub-steps given at Chapter 5.6 can be followed.

First, for each element of the A_I matrix, a block is placed. Outputs of the same row elements of the A_I matrix are wired vertically and ended with a 20pF capacitor that is chosen at design step.

Inputs of the same column elements of the A_I matrix are wired together with respect to the sign of the element. Positive elements use positive input and negative elements use negative inputs. Other input wired to ground.

The same numbered column and row wires wired and output of the elements of b_I matrix wired with respect to their row number.

Input of the elements of c_I matrix wired with respect to their row number and their sign.

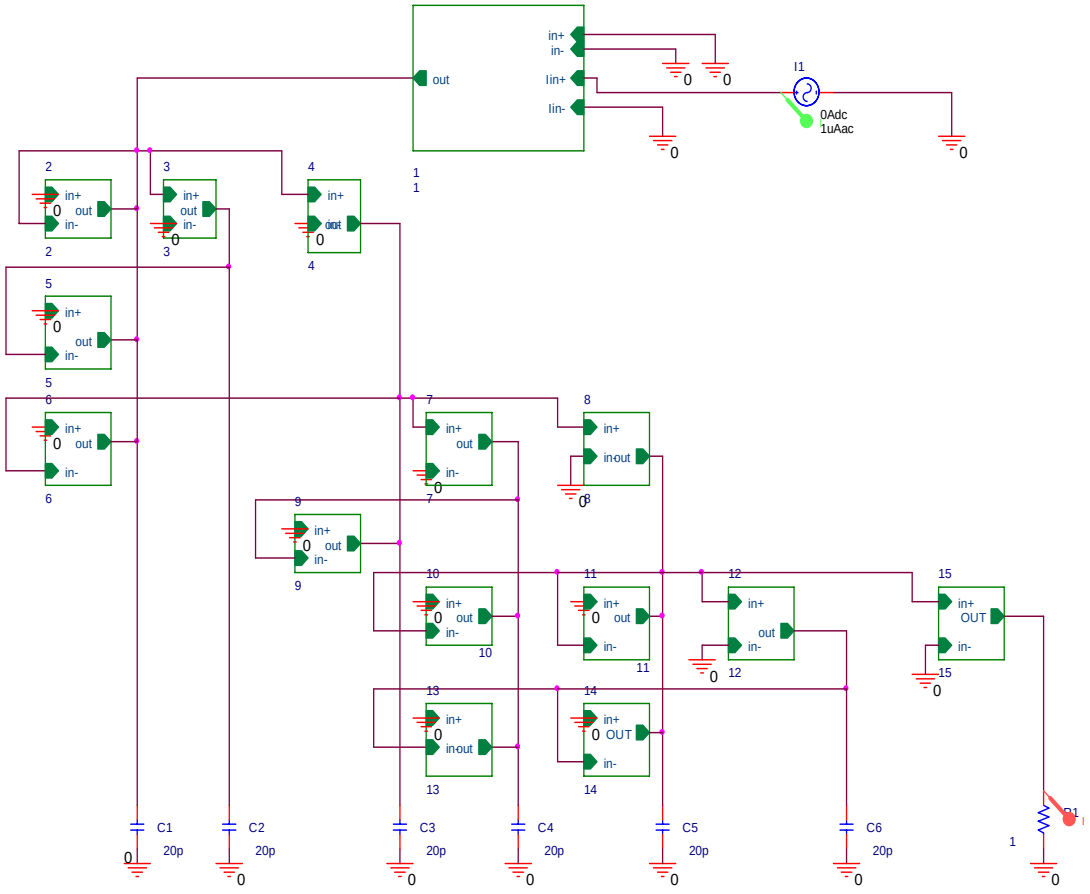

Figure 5.5 Resultant log-domain circuit equivalent to reference SAW filter.

The circuit given in figure 5.5 is the resultant logarithmic domain network and can be proposed as a sixth order SAW filter whose characteristic is given in figure 4.8.

Design of log-domain correspondent of sixth order SAW filter by using state-space synthesis method is completed.

The resultant circuit which is given in figure5.5 is simulated in ORCAD SPICE. The result of AC mode analysis is given as dB in figure 5.6.

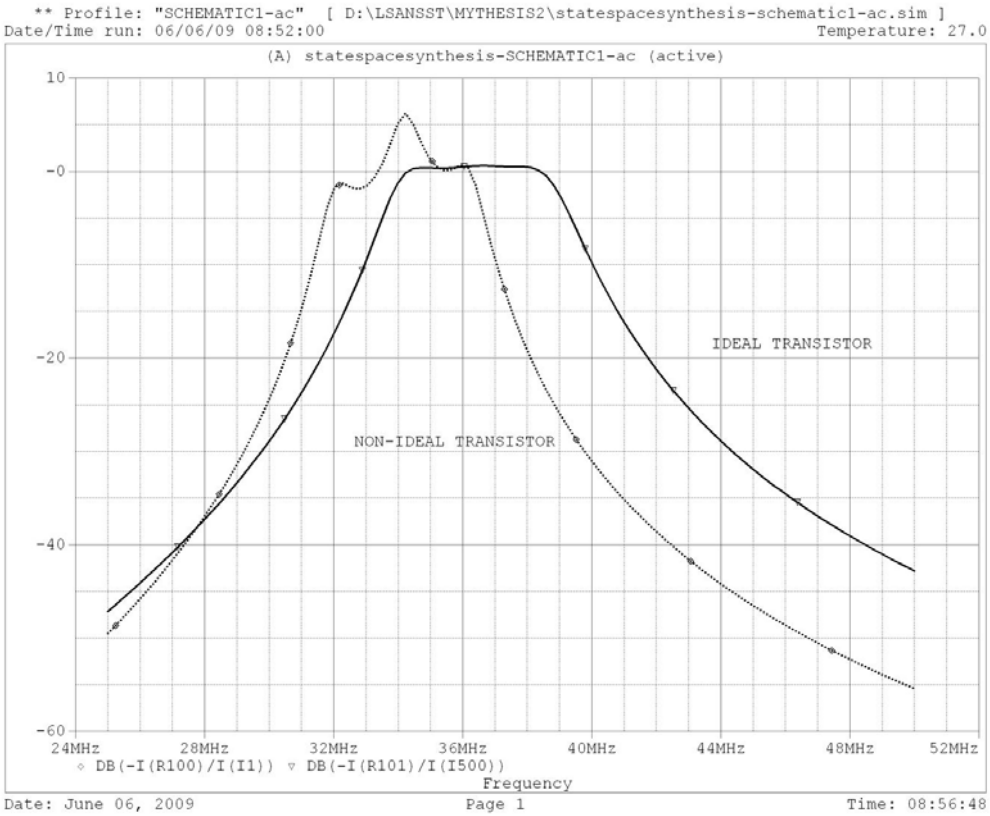

Figure 5.6 Gain response of resultant log-domain circuit.

CHAPTER SIX

COMPARISION OF RESULTS AND CONCLUSIONS

6.1 Comparison of Results

There are two different methods used and simulated by referring to the LC ladder circuit given in figure 4.7.

Reference LC circuit has cut-off frequencies of 35.047 MHz and 41.018 MHz respectively. The 3 dB bandwidth is 5.611MHz. The filter reaches to -40dB stop band attenuation at 30.226 MHz and 48.032 MHz.

Signal flow graph method, which is described in Chapter 4, is applied to reference circuit. The resultant circuit that is shown in figure 4.13 is simulated by using ORCAD SPICE. The simulation is first done for an ideal transistor parameters and then for AT&T transistor library. Both of two simulations are shown in figure 4.14.

Cut-off frequencies of the filter simulated with ideal transistor results are 34.259MHz and 39.609MHz respectively. The 3dB bandwidth is 5.35 MHz. The filter reaches to -40dB stop band attenuation at 27.687 MHz and 48.995 MHz.

Cut-off frequencies of AT&T transistor results are 32.893MHz and 38.008MHz respectively. The 3dB bandwidth is 5.115 MHz. The filter reaches to -40dB stop band attenuation at 26.616 MHz and 46.995 MHz for non-ideal transistors.

State space synthesis method, which is described in Chapter 5, is applied to reference circuit. The resultant circuit that is shown in figure 5.5 is simulated by using ORCAD SPICE. The simulation is first done for an ideal transistor parameters and then for AT&T transistor. Both of two simulations are shown in figure 5.6.

Cut-off frequencies of Ideal transistor results are 33.735MHz and 39.076MHz respectively. The 3dB bandwidth is 5.34 MHz. The filter reaches to -40dB stop band attenuation at 27.242 MHz and 48.469 MHz.

Cut-off frequencies of AT&T library transistor results are 31.894MHz and 36.520 MHz respectively. The 3dB bandwidth is 4.63 MHz. The filter reaches to -40dB stop band attenuation at 27.37 MHz and 42.451 MHz for non-ideal transistors.

If SFG and State space synthesis methods' results for ideal transistors are compared, the 3dB bandwidth performances, which is one of the most important parameters, of both method is approximately the same with LC ladder's bandwidth performance.

Stop band frequencies of SFG method is better than stop band frequencies of state space synthesis method, but the stop band frequency results of both methods (especially low stop band frequencies) should be improved with respect to reference filter.

On the other hand it is obvious to see that the passband ripples of ideal and non-ideal simulation results of SFG method and ideal simulation result of state space synthesis method have better performance than others.

6.2 Conclusion

The main contributions of this study are to synthesise an RF filter by using current mode filtering techniques and realize a model SAW filter by using completely electrical components that is totally different than traditional IF filter designing methods.

Analysis of log-domain circuits were being followed by two different synthesis methods, which are signal flow graph method and state space synthesis method, respectively. Realizing an electrical circuit in a linear system and in a logarithmic system has different advantages and disadvantages on each other. Although analysing and also designing a filter in a linear domain are older and easier, it is shown that log-domain has also systematic analysis and synthesis methods.

The fact that number of components used in a linear type network is less than logarithmic type network. However, a logarithmic network has an important advantage over linear network, which is the suitability for VLSI technologies. An SAW filter should easily be embedded into an IF demodulator or a tuner.

Another important point is the tunability. Characteristic of an active or passive filter is steady and for a slightly offset characteristic, a new design should be done. On the other hand characteristic of a log-domain filter can easily be given an offset on frequency domain by adjusting the external currents or capacitor values. The gain can also be calibrated by the same way. These are excellent features for designers in order to be more flexible.

REFERENCES

Adams, R. W. (1979). Filtering in the log-domain. *63rd AES Conference*, New York.

Baez F., Duster J. S., & Kornegay K. T. (2004). A 1.5V class a 5th order log-domain filter in SiGe technology. *ISCAS 1, 853-856.*

El-Gamal, M., & Roberts, G. W. (1998). Very high-frequency log-domain bandpass filters. *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing* 45 (9), 1188 – 1198.

EPCOS AG.(2009). X6865D, (May, 2009) *http://www.epcos.com/web/generator/Web/Sections/ProductSearch/Hitlist/SAWComponents/Multimedia/IFFiltersVideoApplications/Page,locale=en.html*

Frey, D. R. (2000). Future implications of Log-domain paradigm. *IEEE Proc. – ciruits Devices Syst., 147 (1), 65-72.*

Frey, D. R. (1993). Log-domain filtering: an approach to current-mode filtering. *IEE Proc.-G, Circuits Syst. Devices*, 140 (6), 406-416.

Frey, D. R. (1996). Log-domain filtering for RF applications. *IEEE Journal of Solid State Circuits*, 31 (10), 1468-1475.

Himax Technologies. (2009).*Himax Tuner Hardware Training*. (May, 2009) *http://www.himax.com.tw/en/investor/4Q07_Company_Presentation.pdf*

Kircay, A., & Cam, U. (2006). State-space synthesis of current-mode first-order logdomain filters. *Turkish Journal of Electrical Engineering and Computer Sciences (ELEKTRIK)*, 14 (3), 399-416.

Perry, D., & Roberts, G. W. (1995) Log-domain filters based on LC ladder synthesis. *Proc. ISCAS*, 311-314.

Perry, D., & Roberts, G. W. (1996). The design of log-domain filters based on the operational simulation of lc ladders. *IEEE Transaction on circuits and Systems-2: Analog and Digital Signal Processing, 43(11), 763-774.*

Peters J. J. (02/06/2000). *A History of Television.* (Retrieved May, 2009) http://chem.ch.huji.ac.il/history/tv_history.pdf

Roberts, W. R., & Leung, V. W. (2002). *Design and analysis of integrator-based log-domain filter circuits (1th edition). London: Kluwer Academic Publishers.*

Rukhlenko, A.S. (April 2005). *Lectures and Short Courses.* Retrieved May, 2009, from http://www.intrasaw.com/old/PERSONAL/lectures.html

APPENDICES

APPENDIX A: The SPICE model used for the AT&T CBIC-U2 transistors

(http://www.national.com/models/spice/CL/clc405.cir)

```
.MODEL QOUTN1 NPN
+ IS =2.636E-16 BF =3.239E+02 NF =1.000E+00 VAF=8.457E+01
+ IKF=3.060E-02 ISE=3.674E-17 NE =1.197E+00 BR =3.868E+01
+ NR =1.000E+00 VAR=1.696E+00 IKR=4.928E-02 ISC=2.045E-19
+ NC =1.700E+00 RB =5.467E+01 IRB=0.000E+00 RBM=1.212E+01
+ RE =4.515E-01 RC =1.999E+01 CJE=1.974E-13 VJE=7.973E-01
+ MJE=4.950E-01 TF =1.901E-11 XTF=1.873E+01 VTF=2.825E+00
+ ITF=7.403E-02 CJC=1.883E-13 VJC=8.046E-01 MJC=4.931E-01
+ XCJC=1.57E-01 TR =5.184E-10 CJS=3.540E-13 VJS=5.723E-01
+ MJS=4.105E-01 FC =9.765E-01

.MODEL QOUTP2 PNP
+ IS =1.147E-15 BF =7.165E+01 NF =1.000E+00 VAF=3.439E+01
+ IKF=1.678E-01 ISE=5.690E-15 NE =1.366E+00 BR =1.961E+01
+ NR =1.000E+00 VAR=1.805E+00 IKR=1.178E+00 ISC=3.188E-17
+ NC =1.634E+00 RB =5.323E+01 IRB=0.000E+00 RBM=5.079E+01
+ RE =1.069E+01 RC =3.177E+00 CJE=1.416E-12 VJE=7.975E-01
+ MJE=5.000E-01 TF =3.042E-11 XTF=5.386E+00 VTF=2.713E+00
+ ITF=4.534E-01 CJC=1.918E-12 VJC=7.130E-01 MJC=4.200E-01
+ XCJC=1.76E-01 TR =1.973E-09 CJS=3.054E-12 VJS=6.691E-01
+ MJS=3.950E-01 FC =8.803E-01
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