DOKUZ EYLÜL UNIVERSITY

GRADUATE SCHOOL OF NATURAL AND APPLIED SCIENCES

SMPS BUCK CONVERTER DESIGN FOR PORTABLE DEVICES

by

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March, 2009

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SMPS BUCK CONVERTER DESIGN FOR PORTABLE DEVICES

A Thesis Submitted to the
Graduate School of Natural and Applied Sciences of Dokuz Eylül University
In Partial Fulfillment of the Requirements for the Degree of Master of Science
in Electrical and Electronics Engineering

by

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March, 2009

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M.Sc THESIS EXAMINATION RESULT FORM

We have read the thesis entitled **SMPS BUCK CONVERTER DESIGN FOR PORTABLE DEVICES** completed by **UYSAL ERTEN** under supervision of **ASSOC. PROF. DR. UĞUR ÇAM** and we certify that in our opinion it is fully adequate, in scope and in quality, as a thesis for the degree of Master of Science.

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ACKNOWLEDGEMENTS

I express my deepest gratitude to my advisor Assoc. Prof. Dr. Uğur ÇAM for his guidance and support in every stage of my research. The technique background and the research experience I have gained under his care will be valuable asset to me in the future.

I also want to thank to my administrator, leader and colleagues in VESTEL Digital R&D for their support and help during my thesis research.

Finally, I am grateful to my parents and friends for their patience and never ending support throughout my life.

Uysal ERTEN

SMPS BUCK CONVERTER DESIGN FOR PORTABLE DEVICES

ABSTRACT

This thesis develops estimation and efficiency maximization techniques in Synchronous SMPS Buck Converters. The target applications are voltage regulators for microprocessors used in battery powered systems. Overall system efficiency is a critical design parameter in battery powered systems. It affects both the battery capacity requirement and the end product's run time.

The circuit that delivers power to the microprocessor is usually called a Voltage Regulator Module (VRM). The preferred architecture for this power converter is the buck converter with synchronous rectification. This architecture reduces the ripple both of the output voltage and the input current, allowing for smaller filter components. Because of switching and components used in converters, power losses emerge. Losses that appear in every stage of switching buck converters are investigated. Gate drive optimisation and efficiency maximization techniques are introduced. To obtain higher efficiency at light loads, some control circuits should be used. Pulse Frequency Modulation(PFM) is a control method to stabilize output voltage by improving power supply efficiency at light loads. Besides, some short circuit protection methods are mentioned.

At every stage of thesis, experimental results are presented, showing maximized efficiency even at light load, and optimized gate drive on Intel Montevina Platform Notebook Computer Double Data Rate (DDR) Memory voltage rail.

Keywords : DC-DC converter, synchronous buck converter, efficiency maximization, gate drive optimisation

TAŞINABİLİR CİHAZLAR İÇİN ANAHTARLAMALI GÜÇ KAYNAĞI TASARIMI

ÖZ

Bu tezde, SMPS Senkron Buck dönüştürücünün verimliliğini arttırma teknikleri incelenmiştir. Pille çalışan sistemlerde mikroişlemcileri besleyen gerilim regülatörleri hedef uygulama olarak seçilmiştir. Gerilim regülatörlerinin verimliliği pil ömrünü ve pil kapasitesini belirleyen temel etkendir.

Mikroişlemcilerin güç gereksinimlerini karşılamak için oluşturulan devreler gerilim regülatör modülü (VRM) olarak isimlendirilir. Bu devrelerde çoğunlukla kullanılan DC-DC dönüştürücüler senkron çalışan Buck tipi doğrultuculardır. Buck doğrultucu temel olarak giriş akımındaki ve çıkış gerilimindeki dalgalanmayı en alt seviyede tutarak daha küçük filtreleme elemanları kullanılmasını sağlar. Bu devre elemanları ve anahtarlama sebebiyle oluşan kayıplar incelenmiştir. MOSFET geçit sürme ve doğrultucu verimliliğini arttırma teknikleri anlatılmıştır. Düşük akımlarda daha yüksek verimlilik elde etmek için bazı kontrol devreleri kullanılmaktadır. Bunların en önemlisi darbe frekans modülasyonu ile kontroldür. Ayrıca, bazı kısa devre koruma teknikleri anlatılmıştır.

MOSFET geçit sürme ve doğrultucu verimliliğini arttırma teknikleri uygulanmış deneysel çalışma Intel Montevina Platformu dizüstü bilgisayarı üzerinde çift-veri-oran (DDR) hafızası gerilim hattı kullanılarak tezin her aşamasında yapılmıştır.

Anahtar Sözcükler : DC-DC çeviriciler, senkron buck çeviriciler, verimlilik arttırma, kapı sürme optimizasyonu

CONTENTS

Page

CHAPTER ONE
INTRODUCTION

For over 40 years the semiconductor industry has been evolving steadily following Moore's Law, which states that the number of transistors on a chip roughly doubles every two years. The trend was first observed in 1965 and it is predicted to continue at least until 2020. The implications of this trend are striking. As the size of transistors decreases, their speed increases and more functionality can be incorporated on a single chip at a reduced cost. As a consequence, digital integrated circuits (ICs) have improved dramatically our standard of living. Semiconductors have become a $200 billion industry and the foundation for the trillion-dollar electronics industry.

At the forefront of this revolution are the highly integrated digital processing ICs, especially general-purpose microprocessors. These devices have a tremendous computing power at a low cost. Portable devices are some of the applications powered by microprocessors. The increasing number of transistors and speed of operation creates an increase in the power consumption of the devices. As size is also reduced, the ability to dissipate the heat generated in the power ICs feeding microprocessors is diminished. Consequently, temperatures inside the chip can get close to the thermal limits of silicon. ICs working close to thermal limits can heat up the whole platform. This is one of the reasons why power consumption needs to be efficient. Another important reason is the growing concern on the efficient use of energy resources in the planet, with initiatives like “Energy Star" in the United States. (Eirea G., 2006)

The circuit that delivers the power to the microprocessor is usually called a Voltage Regulator Module (VRM). The preferred architecture for this power converter is the buck converter with synchronous rectification. This architecture reduces the ripple both of the output voltage and the input current, allowing for smaller filter components. Because of switching and components used in converters, power losses emerge. Overall system efficiency is a critical design parameter in

battery powered systems. It affects both the battery capacity requirement and the end product's run time.

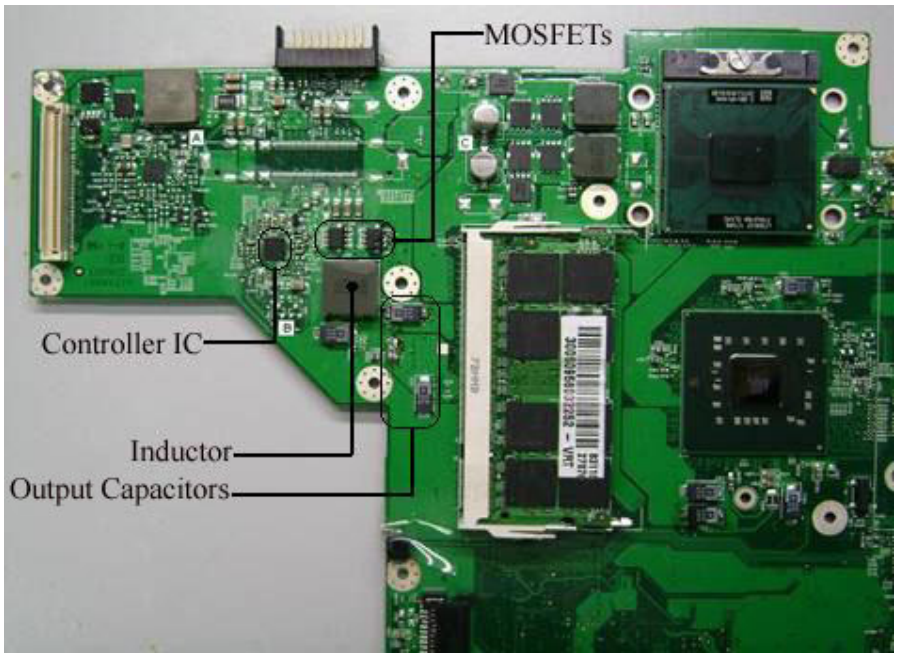

Figure 1.1 INTEL Montevina Platform (A – Battery Charger VRM, B - DDR VRM, C – CPU VRM)

Delivering power to big and complex digital ICs is becoming a challenge not only for notebooks, but also in all portable systems. In portable systems, power has to be delivered to racks and boards in a room. This creates the need to a careful design of the whole power delivery architecture. System consists of seperate voltage rails feeding Double Data Rate (DDR) memory, chipset, Central Processor Unit (CPU) and battery charger. Every rail needs to be optimized for better performance and efficiency. Charger, DDR memory and CPU VRMs are shown in Figure 1.1, also DDR VRM schematics diagram is given in Appendix A which is examined as an application circuit.

Content of the thesis can be summarized briefly as follows;

Chapter two introduces asynchronous and synchronous buck converter topology. Continuous and discontinous operation modes related to the inductor current of buck

converter is mentioned. Formulation of inductor current is given. Block diagram of application circuit is given under synchronous buck converter topology.

Chapter three is dedicated to gate drive optimization. First, gate drive techniques are introduced and shoot trough in synchronous buck converter is examined. Reasons of shoot trough and prevention methods are explained by gate drive optimization. Application circuit gate drives are optimized due to methods mentioned in this chapter.

Chapter four describes the synchronous buck circuit efficiency and losses. In this chapter efficiency definition is done in synchronous buck converters. Losses are explained in every stage of buck converter and in every component composing buck converter. Maximized efficiency of the application circuit is presented.

Chapter five contains pulse frequency modulation control for buck converters. Pulse Frequency Modulation (PFM) is a control method to stabilize output voltage by improving power supply efficiency at light loads compared to Pulse Width Modulation(PWM). Experimantal work is done to demonstrate the rate of change in efficiency.

Chapter six summerizes power circuit protection methods existing in literature. Maximum current limiting, current foldback, hiccup-mode protection methods are introduced and compared to each other. Application circuit protection method is classified with respect to short circuit behaviour.

Chapter seven is concerned with conclusions.

CHAPTER TWO
BUCK CIRCUIT TOPOLOGY

At the forefront of this thesis research, examining simple buck circuit topology and comprehend its dynamcs will be helpfull to concentrate on further topics.

As in linear power supply, the aim of buck converter is providing a lower output voltage. The main difference is increased efficiency. Buck circuit can be classified into two groups with respect to low side conducting device; asynchronous and synchronous Buck Converter.

2.1 Asynchronous Buck Converter

Asynchronous Buck Converter is shown in Figure 2.1. High side switch of the converter is Q_1. It is controlled by periodic pulses to define on and off conditions. When the switch is on, current flows through the inductor. Due to current flow, energy is stored in the inductor. During off state, the stored energy discharges through load. Inductor current specifies mode of the converter. “Discontinuos mode is the situation that inductor current reaches zero and stays zero for a short time. But when the current does not stay in zero, this is called continuos mode.” (Turan B., 2007) The output capacitors reduce ripple of the load voltage whereas diode, D_1, is used to specify path of the current.

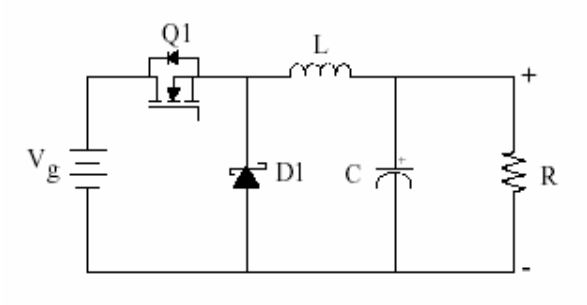

Figure 2.1 Asynchronous Buck Converter topology

Assume, the voltage across output capacitor and load is constant, we can identify the voltage across inductor as;

$$V_L = V_{in} - V_o = L\frac{diL(t)}{dt} \quad (2\text{-}1)$$

When Q_1 is conducting, diode is in reverse biased condition. During conduction period, inductor current increases. This period can be defined as fallows;

$$\int_0^{t_{on}} diL(t) = \int_0^{t_{on}} \frac{V_{in} - V_o}{L} t_{on} \quad (2\text{-}2)$$

$$i_{L(ton)} - i_{L(o)} = \frac{V_{in} - V_o}{L} t_{on} \quad (2\text{-}3)$$

Energy in each component is same at the beginning of one period and at the end of that period, because of steady state condition. Inductor current specifies stored energy. This causes inductor current to be same at the begining and at the end of period;

$$i_{L(O)} = i_{L(T)} \quad (2\text{-}4)$$

$$i_{L(O)} = i_{L(t_{on})} - \frac{V_{in} - V_o}{L} t_{on} \quad (2\text{-}5)$$

$$i_{L(T)} = i_{L(t_{on})} - \frac{-V_o}{L}(T - t_{on}) \quad (2\text{-}6)$$

$$\frac{V_{in} - V_o}{L} t_{on} = \frac{V_o}{L}(T - t_{on}) \quad (2\text{-}7)$$

Turan (2007) describes duty cycle as the ratio of on time to period of one cycle ($D = \frac{t_{on}}{T}$). If DT is put instead of t_{on} in equation 2-7, input-output relationship is expressed as;

$$V_{in}.D = V_o \quad (2\text{-}8)$$

$$D = \frac{V_o}{V_{in}} \qquad (2\text{-}9)$$

Output voltage, duty cycle, and input voltage relation is as given by equation 2-9. Duty cycle can not be bigger than 1, hence output voltage is smaller than input voltage.

2.2 Synchronous Buck Converter

For portable devices and point of load applications, that requires higher efficiency due to battery life restriction; D_1 in Figure 2.1 can be changed to a switching device such as Metal Oxide Semiconductor Field Effect Transistor (MOSFET). This topology is called Synchronous Buck Converter Topology (Figure 2.2). High side and low side switches are working synchronously. By changing D_1 to a switching device, power loss caused by forward voltage drop over diode is prevented. As a result efficiency will be higher.

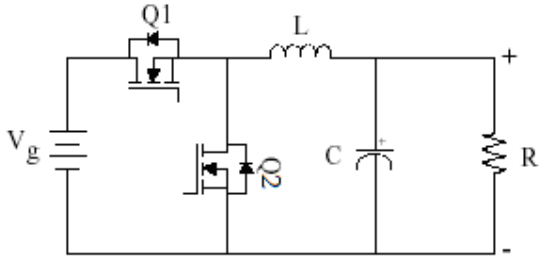

Figure 2.2 Synchronous Buck Converter Topology

In the application examined in this thesis, Synchrouns Buck Converter topology is used to increase efficiency. Application Buck circuit is composed from two switching devices, instead of using diode, D_1 in Figure 2.1. Buck circuit used in application circuit is shown in Appendix A.

Block diagram of Intel Montevina Platform Notebook Computer Double Data Rate (DDR) Memory Voltage rail is given in Figure 2.3. It is a Synchronous Buck

Converter topology. DC power source is typically battery voltage for notebook computers. In application, input voltage is 12.6V. Two MOSFETs are used as switchers. Due to switching periods, storage element such as inductor is used. Inductor stores magnetic energy and then maintain the stored energy to output. Output filter reduces ripple voltage and smooths output voltage. Also, capacitors composing output filter are charge sources at transient load instants. Feedback loop exists to obtain exact DC voltage level. Switching and output voltage level is tracked by controller IC.

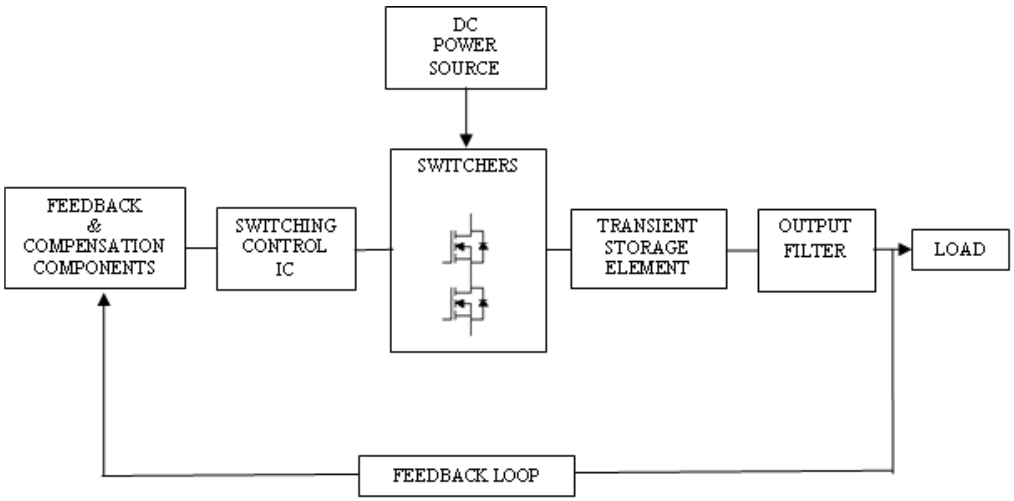

Figure 2.3 Block Diagram of Montevina Notebook PC DDR Memory Voltage Regulator

CHAPTER THREE
SHOOT TROUGH IN SYNCHRONOUS BUCK CONVERTERS

Scynchronous buck topology is in widespread use in mobile solutions. Today's converters supply ultimate low voltages and high currents for CPU's, memories and chipsets.

"Shoot through is defined as the condition when both MOSFETs are either fully or partially turned on, prividing a path from input DC source to ground." (Klein J., 2003) This low resistance path causes excessive current flow over switchers. Hazardous damages because of high current and loss of efficiency may happen. In addition, circuit components sustained to high current overheat themselves and the whole system.

Shoot through problem is introduced in two sections. First part includes gate drive techniques in literature and root cause of the problem. Second part is dedicated to possible solutions of the problem by selecting appropriate MOSFET for the application, and gate drive optimization.

3.1 Gate Drive Control Techniques and Induced Turn-on Problem

Shoot trough is a serious problem for DC-DC converters having Synchronous Buck topology. At controllers of synchronous buck converter, some gate drive control techniques are used to prevent shoot through.

3.1.1 Gate Drive Control Techniques

Two major control technique is in widespread use in controller industry. Fixed dead time and adaptive gate drive topology is introduced.

3.1.1.1 Fixed Dead Time. High side MOSFET is turned off, then a fixed delay is provided before lowside is turned on. Fixed dead time technique is simple and effective, but suffers from lack of flexibility if a wide range of MOSFET gate capacitances are to be used with a given controller. For a fixed long dead-time causes high conduction losses and too short dead time can cause shoot-through. Typically fixed dead-time is situated on the too long side to allow high gate-source capacitance (C_{GS}) to fully discharge before turning on the low side MOSFET.

3.1.1.2 Adaptive Gate Drive. Adaptive gate drive circuit traces gate source voltage (V_{GS}) of driven MOSFET and determines exact time to turn on the complemantary MOSFET. Adaptive gate drive technique is the shortest dead time preventing shoot through. Short dead time increases efficiency and battery life. Portable application power supply circuits have Adaptive Gate Drive technique for effective solution. Figure 3.1 illustrates typical adaptive gate drive circuit. (Klein J., 2003) There is a comparator tracing gate voltage levels and after adding a delay, it fires a new shot for the complemantary MOSFET.

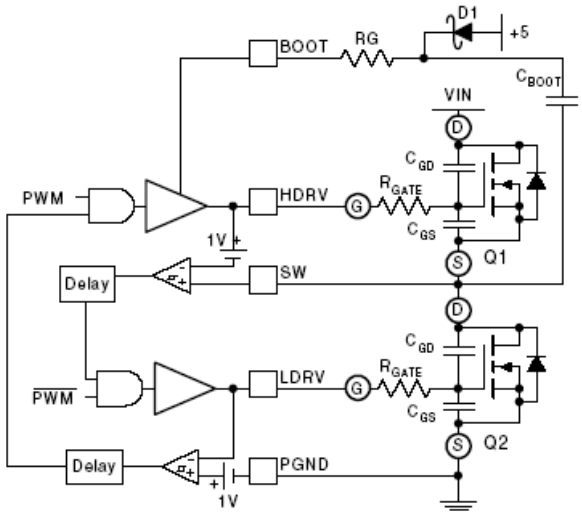

Figure 3.1 Typical Adpative Gate Drive Circuit

3.1.2 Cdv/dt Induced Turn-On

Fixed dead time and adaptive gate drive techniques may not be the solution to shoot trough. Also, observing shoot through is very difficult because shoot through current appears only for a few nS. An undesired inductance at current probe can affect current waveform. Shoot trough arises with loss of efficiency and heat on components over current path.

A simplified MOSFET Model is illustrated in Figure 3.2 to describe $C\frac{dv}{dt}$ induced turn-on. (Wu T., 2004)

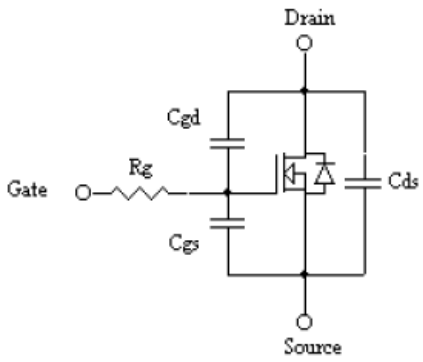

Figure 3.2 Simplified MOSFET Model

C_{gs} is the gate-to-source capacitance, C_{gd} is the gate-to-drain capacitance, C_{ds}, R_g are drain-to-source capacitance and internal gate resistance respectively.

Because of turn on delay of Q_1, input voltage does not appear immadeately at drain of Q_2 during the switching period of Q_1. The imposed voltage over C_{gd} induces a current. This induced current generates a voltage drop across internal gate resistance R_g of Q_2 and external gate resistance R_{ext}, charging the C_{gs} of Q_2. (Figure 3.3)

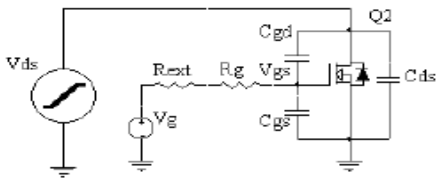

Figure 3.3 Model circuit of Cdv/dt induced turn-on

The amplitude of induced voltage on Q_2 is proportional to C_{gd}, C_{gs}, total gate resistance and $\frac{dv}{dt}$. If amplitude of induced voltage exceeds treshold voltage of MOSFET, Q_2 turns on while Q_1 is on. In this situation shoot-trough current will flow from input to ground over Q_1 and Q_2. Q_2 carries shoot-through current while Q_1 carries both shoot-through and load current. As a result shoot-through manifests itself as a reduced efficiency, increased MOSFET temperatures, high electromagnetic interferance and ringing.

The $C\frac{dv}{dt}$ induced turn-on can be simulated as a periodic function of voltage applied to drain pin of Q_2. Equivalent circuit of Figure 3.3 is derived as Figure 3.4. The equivalent circuit is valid during rising edge of the drain voltage.

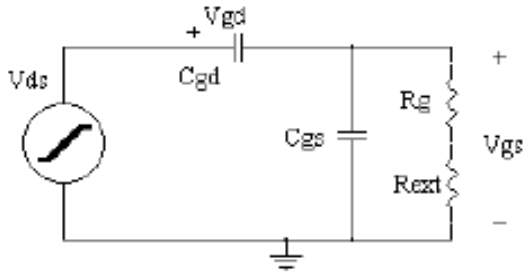

Figure 3.4 Equivalent Circuit of Figure 3.3

Loop equations can be written as fallows;

$$V_{ds} = V_{gd} + V_{gs} \qquad (3\text{-}1)$$

$$C_{gd}\frac{dV_{gd}}{dt}=C_{gs}\frac{dV_{gs}}{dt}+\frac{V_{gs}}{R_t} \tag{3-2}$$

Rt is the sum of R_{ext} and R_g. V_{gd}, V_{ds}, and V_{gs} are gate-to-drain voltage, drain-to-source voltage and gate-to-source voltage respectively.

$$C_{gd}\frac{d(V_{ds}-V_{gs})}{dt}=C_{gs}+\frac{dV_{gs}}{dt}+\frac{V_{gs}}{R_t} \tag{3-3}$$

$$C_{gd}\frac{dV_{ds}}{dt}=(C_{gs}+C_{gd})\frac{dV_{gs}}{dt}+\frac{V_{gs}}{R_t} \tag{3-4}$$

Q_2 drain voltage is a periodic function and can be defined as;

$$V_{ds}=\begin{cases}\frac{V_m}{T_m}\times t,\ if\ 0\le t\le T_m\\ V_m,\ if\ T_m\le t\le T_{on}\\ \\ 0,\ if\ T_{on}\le t\le T_s\end{cases} \tag{3-5}$$

Tm is the time when V_{ds} reaches its maximum value of V_m, T_s is switching period, T_{on} is on time of Q_1. $\frac{dv}{dt}$ of drain voltage of Q_2 is constant during the rising period.

$$\frac{dV_{ds}}{dt}=\frac{V_m}{T_m},\ 0\le t\le T_m \tag{3-6}$$

$$C_{gd}\times\frac{V_m}{T_m}=(C_{gs}+C_{gd})\frac{dV_{gs}}{dt}+\frac{V_{gs}}{R_t} \tag{3-7}$$

Linear differential equation (3-7) can be solved for $V_{gs}=V_{th}$ to find out $C\frac{dv}{dt}$ induced voltage at gate terminal of Q_2.

$$V_{gs} = R_t \times C_{gd} \times \frac{V_m}{T_m} \times \left\{ 1 - e^{\frac{-t}{R_t \times (C_{gd}+C_{gs})}} \right\} \qquad (3\text{-}8)$$

Equation (3-8) shows that peak gate voltage induced is determined by C_{gd}, C_{gs}, and $\frac{dv}{dt}$ slope on drain. Increasing $\frac{dv}{dt}$ of the voltage applied to drain, results higher induced voltage. Maximum induced voltage appears at t= T_m.

$$V_{gs,\max} = R_t \times C_{gd} \times \frac{V_m}{T_m} \times \left\{ 1 - e^{\frac{-T_m}{R_t \times (C_{gd}+C_{gs})}} \right\} \qquad (3\text{-}9)$$

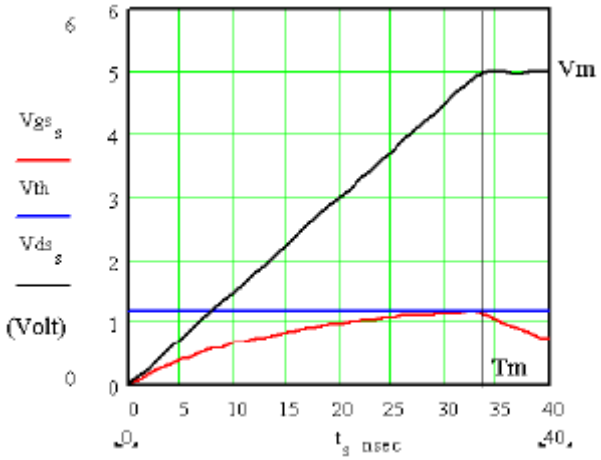

Figure 3.5 Minimum required dv/dt for Vgs>Vth

For the case;

$$T_m << R_t \times (C_{gd} + C_{gs}) \qquad (3\text{-}10)$$

Equation can be simplified to;

$$V_{gs,\max} = R_t \times C_{gd} \times \frac{V_m}{T_m} \times \left\{ 1 - e^{\frac{-T_m}{R_t \times (C_{gd+C_{gs}}}} \right\} \quad (3\text{-}11)$$

$$\cong R_t \times C_{gd} \times \frac{V_m}{T_m} \times \left\{ 1 - 1 + \frac{T_m}{R_t \times (C_{gd} + C_{gs})} \right\} \quad (3\text{-}12)$$

$$\cong R_t \times C_{gd} \times \frac{V_m}{T_m} \times \frac{T_m}{R_t \times (C_{gd} + C_{gs})} \quad (3\text{-}13)$$

$$\cong \frac{C_{gd}}{C_{gd} + C_{gs}} \times V_m \quad (3\text{-}14)$$

Before the drain voltage of Q_2 reaches V_m, its gate voltage can not be greater than the treshold voltage. The related waveforms are illustrated at Figure 3.5. If applied V_{ds} slew rate on Q_2 is greater than V_m/T_m (Figure 3.5) then V_{gs} will be over the treshold voltage and MOSFET will be turned on due to induced voltage.

3.1.2.1 Cdv/dt Induced Turn-On In Application Circuit. Measuring $C\frac{dv}{dt}$ induced voltage needs extra care and attention. Suitable laboratory setup for the application should be established. Laboratory setup to examine application circuit for this thesis research is shown in Figure 3.6.

Scope shots of application circuit are given at Figure 3.7 through Figure 3.9. High side gate signal, low side gate signal and output voltage waveforms are seen in Figure 3.7. Closer analysis of low side gate drive signal (Figure 3.8) assists to estimate $C\frac{dv}{dt}$ induced turn-on. Magnitude of voltage peaks on low-side gate drive signal is critical at high-side gate rising edge instants. This $C\frac{dv}{dt}$ induced voltage

(Figure 3.9) should not exceed 1V for most of the applications. Internal comperator inside the controller IC tracks low side gate signal to fall below 1V and fires a new high side gate shot. $C\frac{dv}{dt}$ induced voltage exceeding 1V may stir tracking logic. Also $C\frac{dv}{dt}$ induced voltage should be far below gate threshold voltage of MOSFET. At Figure 3.8, $C\frac{dv}{dt}$ induced voltage is 0,89V. Level of induced voltage is adjacent to 1V comparison voltage. $C\frac{dv}{dt}$ induced voltage needs to be reduced. Some methods to reduce induced voltage will be mentioned at "3.2.2 Gate Drive Optimization" section.

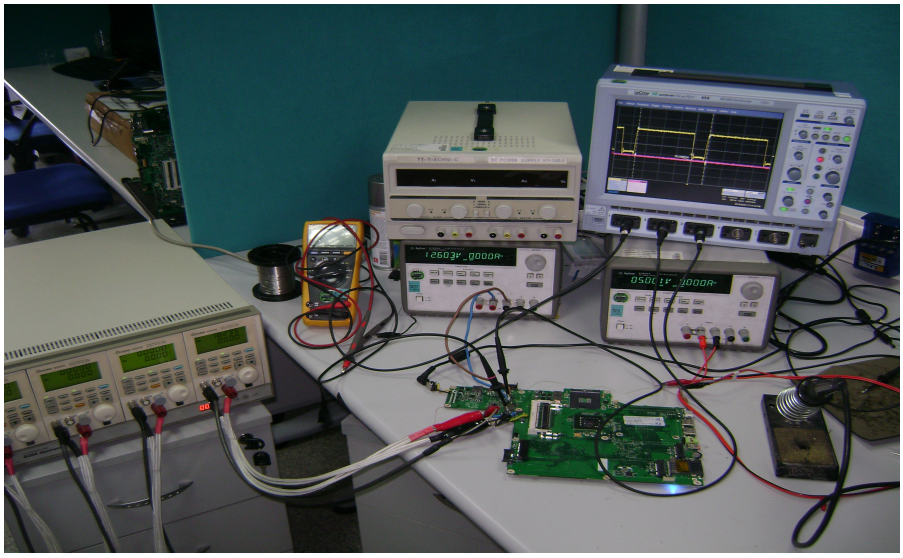

Figure 3.6 Laboratory Setup of Application Circuit

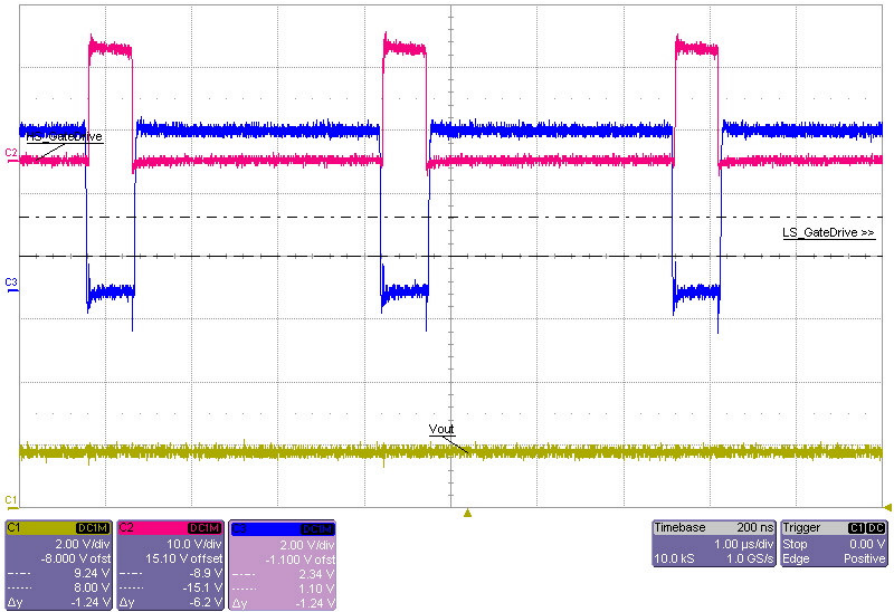

Figure 3.7 High side gate signal, low side gate signal and output voltage waveforms

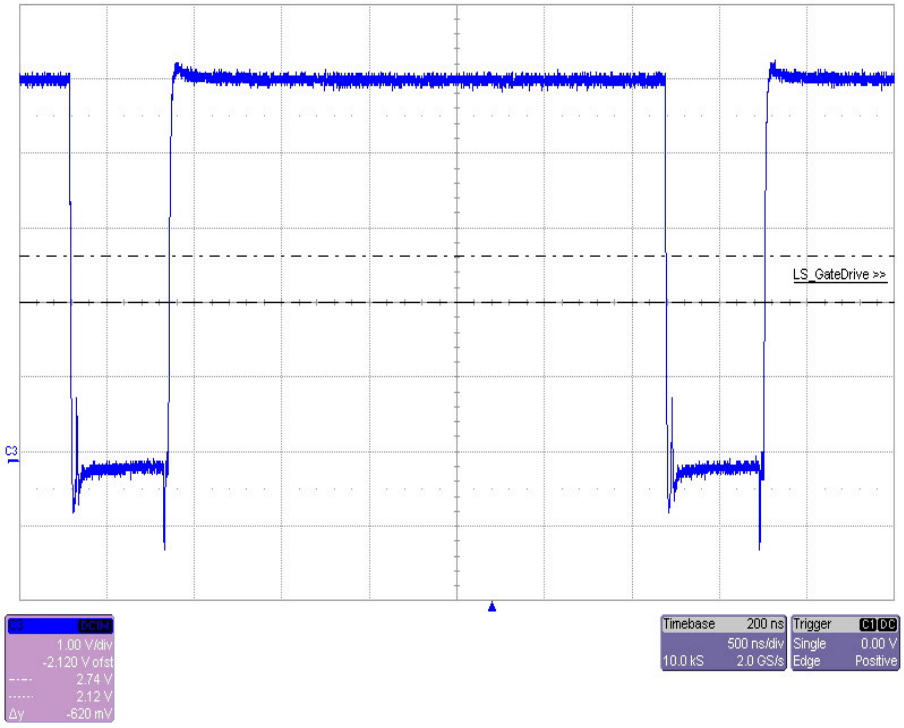

Figure 3.8 Low-Side gate drive signal

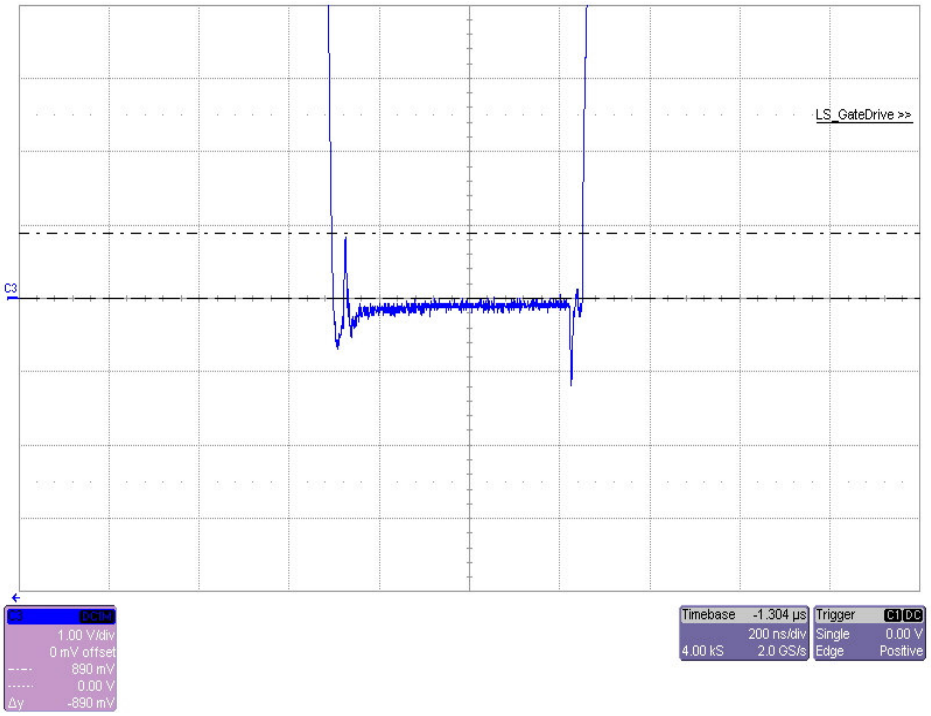

Figure 3.9 $C\frac{dv}{dt}$ induced voltage

3.2 Solutions to Shoot Trough Problem

Possible solutions to shoot trough problem can be identified in two sections. Selecting appropriate MOSFET for the application and gate drive optimization prevents shoot trough and excessive current flow.

3.2.1 Effect of MOSFET on Shoot Trough

Different MOSFET based solutions can be implemented at design stage to prevent $\frac{dv}{dt}$ induced turn on problem. Turn-on threshold voltage level, gate-to-drain and gate-to-source capacitances of MOSFET have incontrovertible effect over $\frac{dv}{dt}$ induced turn on problem. First, threshold voltage of MOSFET could be higher, but this increases R_{dson} of the MOSFET. As a result, R_{dson} based losses is going to be augmented.

Another solution is to decrease C_{gd} and increase C_{gs}. That could be implemented at design stage of MOSFET. Increasing C_{gs} causes to lengthen charging time and reduces peak induced voltage at gate of Q_2. Choosing MOSFETs that have lower C_{gd} and C_{gs} capacitances still may not be the solution. The key point is to choose Q_2 MOSFET, based on $\frac{Q_{gd}}{Q_{gs1}}$ ratio. Q_{gs1} is gate-to-source charge before gate voltage reaches treshold voltage. As mentioned, lowering drain-to-source capacitance, C_{ds}, or enlarging gate-to-source capacitance, C_{gs}, is going to reduce $C\frac{dv}{dt}$ induced voltage. (Wu T., 2004) However, $C\frac{dv}{dt}$ induced turn-on at Q_2 also depends on drain-source voltage (V_{ds}) and threshold voltage, Vth. It then makes sense to use gate charges instead of gate capacitances to evaluate Q_2 device. When V_{ds} reaches input voltage, it should be smaller than total charge on C_{gs} at V_{th} level so that Q_2 is not going to be turned on.

$$C_{gd} \times V_{gd} \le C_{gs} \times V_{gs} \tag{3-15}$$

The maximum charge stored in C_{gd} is equal to C_{gd} capacitance times voltage difference between Cgd terminals $(V_{ds} - V_{th})$ when V_{ds} reaches input voltage.

$$C_{gd} \times (V_{ds} - V_{th}) \le C_{gs} \times V_{th} \tag{3-16}$$

$$\frac{Q_{gd}}{Q_{gs1}} = \frac{C_{gd} \times (V_{ds} - V_{th})}{C_{gs} \times V_{th}} \le 1 \tag{3-17}$$

According to the equation (3-17), $\frac{Q_{gd}}{Q_{gs1}}$ should not be greater than 1 to prevent $C\frac{dv}{dt}$ induced turn on. (Mappus S., 2005) It is obvious that, increasing input voltage results in higher charge ratio. As a result $C\frac{dv}{dt}$ induced turn on problems are more severe in notebook dc-dc power supplies than in desktop supplies. Input voltage level

for laptop synchronous switching regulators varies between 5V to 24V, while desktops' are mainly 5V.

3.2.1.1 Effect Of MOSFET on Shoot Through In Application Circuit. In application circuit, low side MOSFET that has $\frac{Q_{gd}}{Q_{gs1}}$ ratio of 1.25 is used. Resultant $C\frac{dv}{dt}$ induced voltage is 0.89V shown in Figure 3.9. To demonstrate the effect of different MOSFETs over $C\frac{dv}{dt}$ induced voltage; low side MOSFET gate drive scope shot is taken with another MOSFET which has $\frac{Q_{gd}}{Q_{gs1}}$ ratio of 1.306. Gate drive signal of changed MOSFET is shown in Figure 3.10. Closer look at the induced voltage is shown in Figure 3.11. Value of induced voltage is 1.74V.

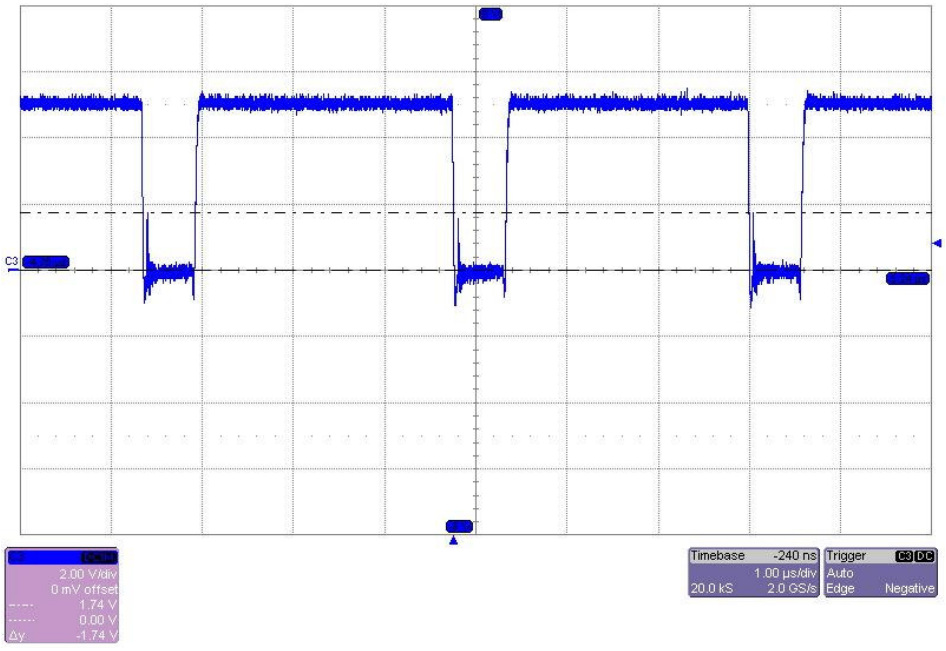

Figure 3.10 Gate drive signal for the MOSFET that have $\frac{Q_{gd}}{Q_{gs1}}$ ratio of 1.306.

It is not always possible to find a MOSFET with $\frac{Q_{gd}}{Q_{gs1}}$ ratio smaller than 1 that suits the application. In this situation, taking measurements of induced voltage and analysis of scope shots are useful to decide. After than, decision can be made easily with results as in application circuit examined in this thesis. First MOSFET with $\frac{Q_{gd}}{Q_{gs1}}$ ratio of 1.25 have reduced induced voltage level even $\frac{Q_{gd}}{Q_{gs1}}$ bigger than 1.

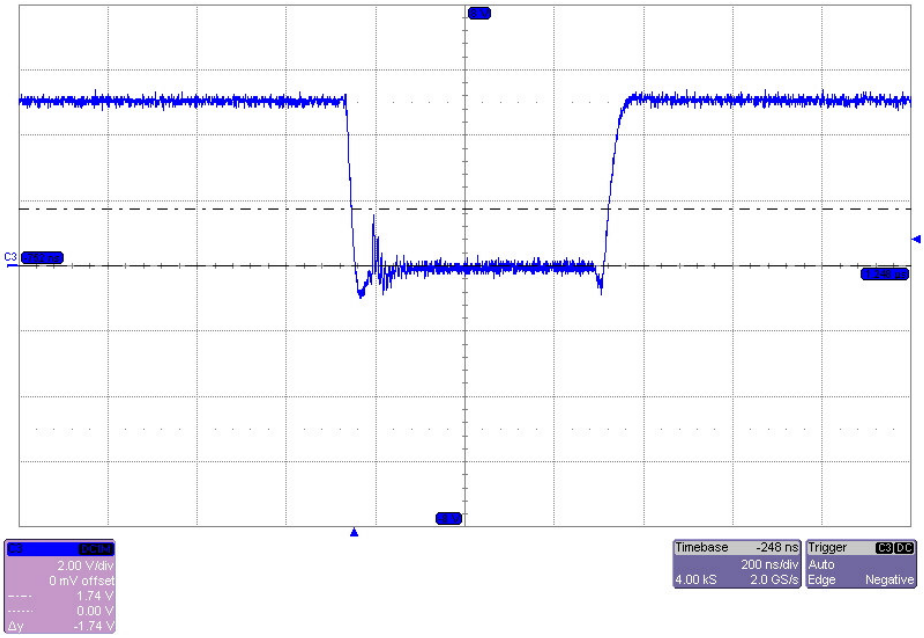

Figure 3.11 $C\frac{dv}{dt}$ induced voltage for the MOSFET that have $\frac{Q_{gd}}{Q_{gs1}}$ ratio of 1.306.

3.2.2 Gate Drive Optimization

Choosing appropriate MOSFET with $\frac{Q_{gd}}{Q_{gs1}}\langle 1$ ratio may not be enough to prevent shoot-through or in real world, it is not easy to find a MOSFET with $\frac{Q_{gd}}{Q_{gs1}}\langle 1$ ratio

that is suitable for your application. Reducing switching speed of Q_1 MOSFET can be implemented by adding an external gate resistor R_{rise} (Figure 3.12).

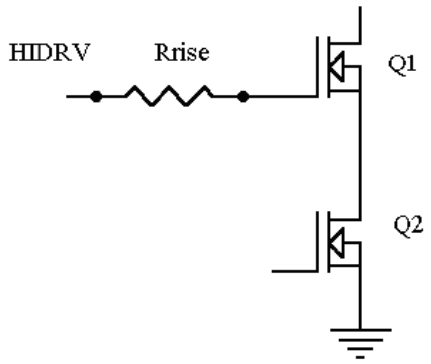

Figure 3.12 Optimized Gate Drive

Optimization of gate resistor is important because target is to minimize switching losses while reducing $\frac{dv}{dt}$ induced voltage at Q_2. Recommended value of the resistor is 4.7 Ohms. (Fairchild, 1998) Adding high valued gate resistor to Q_1 will increase turn-on time (t_r) and switching losses by product of t_r. Also, adding this gate resistance increases turn-off time (t_f), causing loss of dead time with correspondingly conduction overlap of Q_1 and Q_2. As a result, conduction overlap creates a huge shoot trough current.

When Q_1 is turned on, gate voltage is applied through external gate resistance, MOSFET's internal gate resistance controls turn on speed of Q_1. During turn off, gate capacitance of Q_1 discharges through external gate resistor to the gate driver.

To conclude, $C\frac{dv}{dt}$ induced turn on in a synchronous regulator is caused by abrupt rising edge of drain voltage at synchronous MOSFET Q_2. Due to undesired shoot-trough currents flowing into both Q_1 and Q_2, efficiency decreases. Reducing $\frac{Q_{gd}}{Q_{gs1}}$ ratio and increasing treshold voltage level of MOSFETs can be possible

solutions to $C\frac{dv}{dt}$ induced shoot trough. Also, applying gate resistance to Q_1 could be possible solution at the design stage of the synchronous regulator.

3.2.2.1 Gate Drive Optimization Of Application Circuit. In application circuit, potential shoot through hazard is obvious with respect to induced voltage level of 0.89V at Figure 3.9. Reducing $C\frac{dv}{dt}$ induced voltage needs extra attention and knowledge. First, adding a parallel capacitor to low side mosfet gate-source capacitance (C_{GS}) is reasonable start. Input capacitance (C_{ISS}) of low side MOSFET is 4000 pF. Adding 4700 pF capacitor is convenient to decrease $\frac{Q_{gd}}{Q_{gs1}}$ ratio. This parallel capacitor reduces the induced voltage by decreasing $\frac{Q_{gd}}{Q_{gs1}}$ ratio without lowering efficiency. As a major point, low side losses consist of $R_{DS(ON)}$ losses regarding 4.2.2 Low Side MOSFET Losses section. Figure 3.13 illustrates the resulting low side gate drive signal with a parallel capacitor. Induced voltage is reduced from 0,89V to 0,62V.

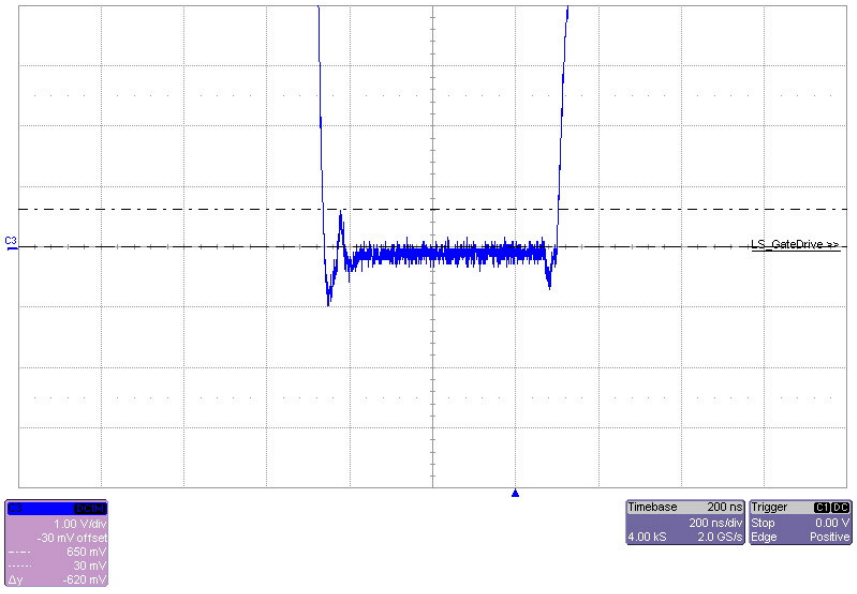

Figure 3.13 Low side gate drive signal with parallel capacitor to low side C_{GS} added

Potential shoot through hazard still occurs bacause induced voltage is not so far below 1V. Addition of 4,7 Ω series resistance to high side gate drive way causes slower rise of gate signal. Increasing turn-on time for the high side MOSFET decreases efficiency. High side gate drive signal without series resistance is seen at Figure 3.14. Oscillation on rising edge of high side gate signal is obvious because of high switching speed. Turn-on time is short without series resistor. Gate drive voltage have overshoot and undershoot composing oscillation.

If Figure 3.14 is compared to Figure 3.15 increased turn-on time is realizable. Oscillation on rising edge of gate drive signal is prevented. Rising edge of gate signal is more smooth at Figure 3.14 compared to Figure 3.15.

Figure 3.14 High side gate drive signal without series resistance

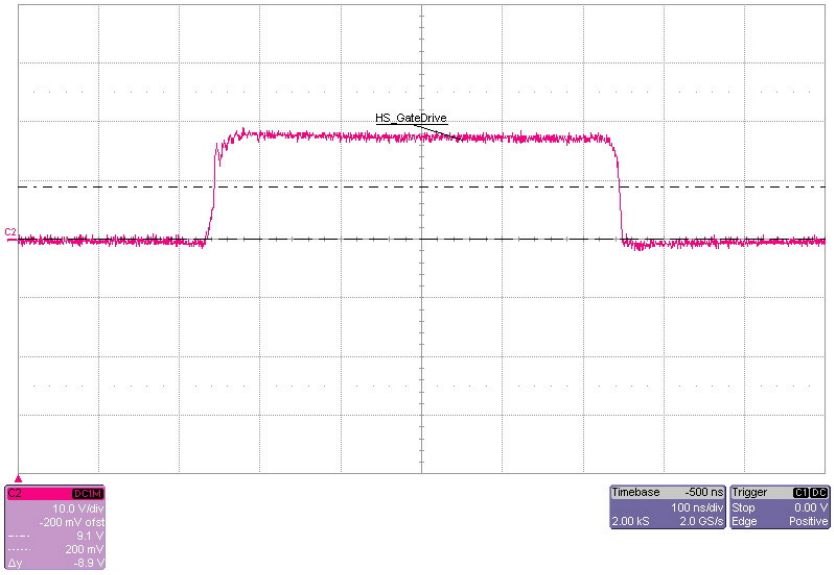

Figure 3.15 High side gate drive signal with 4,7 Ohm series resistance

As a result, induced voltage is diminished to 0,46V (Figure 16). Magnitude of induced voltage leaves enough gap to prevent $C\frac{dv}{dt}$ induced turn-on. Placed resistor have minimal effect on efficiency but prevents shoot trough. Accurate evaluation of Buck Converter assists to achieve better performance and efficiency while maintaning safe operation. Resultant gate drive signals are shown in Figure 3.17.

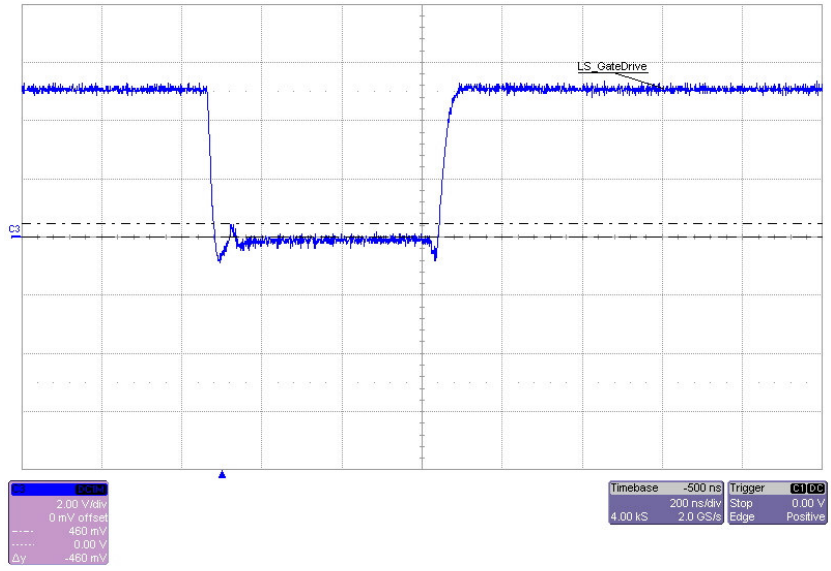

Figure 3.16 Low side gate drive signal with 4,7 Ohm series resistance

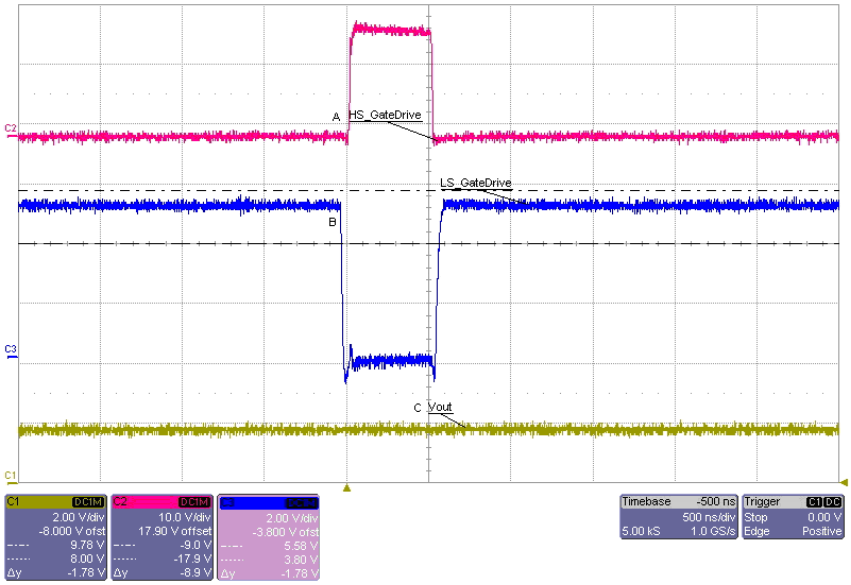

Figure 3.17 Optimized gate drive signals. A, B, C are high-side gate drive, low-side gate drive and output voltage waveforms respectively.

CHAPTER FOUR

SYNCHRONOUS BUCK CONVERTER EFFICIENCY AND LOSSES

After gate drive optimization of Synchronous Buck Converter, next step is to maximize efficiency. In this chapter, definition of efficiency will be given for voltage regulators having Synchronous Buck Converter topology. Effects of efficiency over total system dynamics will be mentioned.

Efficiency and losses are interdependent concepts. Losses arise over components forming voltage regulator and decrease efficiency. Importance of component selection to minimize losses will be explained.

4.1 Synchronous Buck Converter Efficiency

Voltage Regulator Modules (VRM) for battery powered portable devices convert, manage, and distribute power. They supply power to graphic cards, processor chips, and memories. How much of the input power is transferred to output defines battery run time and total system temperature. Efficiency is the ratio of output power to input power and can not exceed one hundred percent. Wikipedia (n.d.) formulise efficiency as;

$$Efficiency = \frac{P_{OUTPUT}}{P_{INPUT}} \tag{4-1}$$

P_{OUTPUT} is the ouput power and P_{INPUT} is the input power.

For Synchronous Buck Converters, input power is the product of input voltage and current. Also output power is the product of output voltage and current. In ideal world, there is no loss of power during dc-dc conversion, but because of component non-idealities losses occur. Losses appear during switching and conduction over MOSFETs, inductor and other power components. The amount of losses define

efficiency of the converter. Losses arising in every stage of Buck Converter will be mentioned in “4.2 Synchronous Buck Converter Losses” section.

Efficiency of every independent converter block determines the total system efficiency. Efficient system makes best use of the resources available, so battery is the only resource for a portable device. Total system efficiency specifies battery run time of the portable device. Battery life is a critical parameter both for designers and end-users.

Regarding battery life, efficiency has a incontrovertible effect over total system temperature. Power losses on each component arises as heat. Dissipation of this heat is a serious problem for a limited volume portable device. Additional active cooling has to be used to decrease temperature of the whole system. Also, existing cooling fan may need to be run faster causing additional power consumption.

4.2 Synchronous Buck Converter Losses

Synchronous Buck converter circuit is very popular to provide high current, low voltage applications such as CPUs, chipsets, peripherals. Typically used to convert from 19V, 12V or 5V to related voltage levels. Several Buck converters create voltage rails of the whole system. Each individual Buck converter losses define overall system loss.

The majority of losses during conversion is due to losses over power components. MOSFET switches, inductor and output capacitors are forming power components. Figure 4.1 illustrates a synchronous Buck converter output stage and power components. Q_1 is the high side, Q_2 is the low side MOSFET. L_1 is the inductor and output voltage is shown over output capacitor. Each component have typical loss characteristic and will be mentioned.

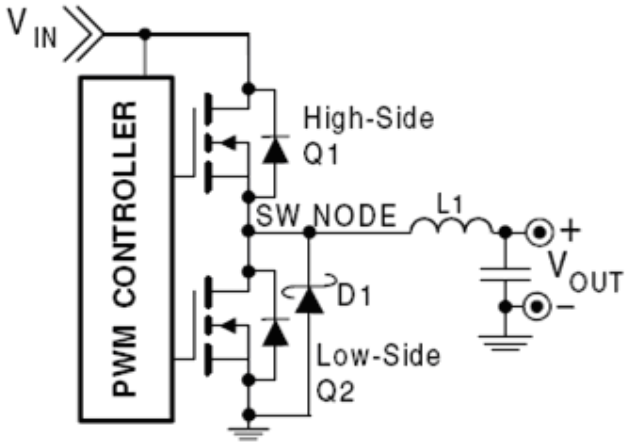

Figure 4.1 Synchronous Buck Output Stage

4.2.1 High-Side MOSFET Losses

The power loss of MOSFET is combination of switching losses and MOSFET's conduction losses. For low duty cycles (12V input, 1.8V output) switching losses tend to dominate.

$$P_{MOSFET} = P_{SW} + P_{COND} \tag{4-2}$$

4.2.1.1 High-Side Conduction Losses. High-Side conduction losses appears during conduction of MOSFET. It is straightforward conduction losses are I^2R losses in MOSFET times MOSFET's duty cycle:

$$P_{COND} = I_{OUT}{}^2 \times R_{DS(ON)} \times \frac{V_{OUT}}{V_{IN}} \tag{4-3}$$

$R_{DS(ON)}$ is drain source on resistance of the MOSFET. $R_{DS(ON)}$ is directly proportional to the temperature.

V_{OUT} is output voltage of synchronous buck converter, V_{IN} is input voltage of synchronous buck converter.

For DC-DC converters, choosing the appropriate component have a key role to define efficiency ratings. High side MOSFET $R_{DS(ON)}$ of my application circuit is 14.4 $m\Omega$. Calculated conduction loss for 5 Ampere average load current is 0.051 W. Calculated conduction loss for my application circuit is pretty low to have high efficiency ratings. Resultant efficiency table for my application circuit will be represented in fallowing sections.

4.2.1.2 High-Side Switching Losses. Switching period is broken up into 5 sections (t_1-t_5) as shown in Figure 4.3. Top drawing in Figure 4.3 voltage across MOSFET and current through it. Bottom timing represents V_{gs} as a function of time. Related curves assumes gate is being driven with a constant current.

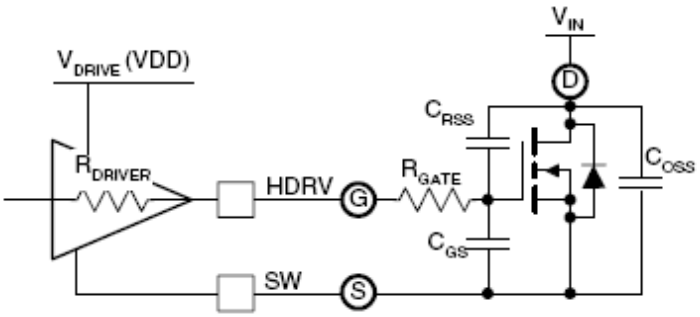

Figure 4.2 Drive Equivalent Circuit

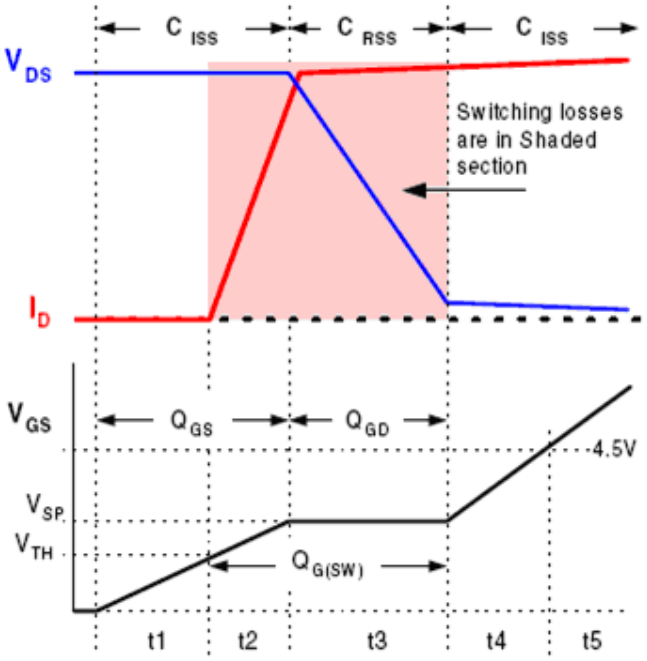

Figure 4.3 High-Side Switching losses and Q_G

Switching interval begins when high-side MOSFET driver turns on and starts to supply current to gate of Q_1. There are no switching losses until V_{GS} reaches the MOSFET's V_{TH}, therefore $P_{t1}=0$.

When V_{GS} reaches V_{TH}, input capacitance (C_{ISS}) is being charged and I_D (MOSFET's drain current) is rising linearly until it reaches current in L_1 (I_L) which is presumed to be I_{OUT}. During this period (t_2) MOSFET is carrying the whole input voltage across it. Energy over MOSFET during t_1 is;

$$E_{t2} = t_2 \times \left\{ \frac{V_{IN} \times I_{OUT}}{2} \right\} \qquad (4\text{-}4)$$

Next period is t_3. At this point, Q_1 is sustaining entire I_{OUT}, V_{DS} begins to fall and current charges C_{GD}. During t_3 current is constant but voltage decreases from V_{IN} to 0, therefore;

$$E_{t3} = t_3 \times \left\{ \frac{V_{IN} \times I_{OUT}}{2} \right\} \quad (4\text{-}5)$$

During t_4 and t_5, MOSFET enhances channel to obtain its rated $R_{DS(ON)}$ at a rated V_{GS}. Losses during t_4 and t_5 are very small compared to remaining two periods (t_2 and t_3). MOSFET is simultaneously carrying voltage and conducting current. Therefor losses during t_4 and t_5 will be ignored for the analysis.

As a result, switching loss for any given edge is power occurs in each switching interval, multiplied by duty cycle of switching interval.

$$P_{SW} = \left\{ \frac{V_{IN} \times I_{OUT}}{2} \right\} \times (t_2 + t_3) \times F_{SW} \quad (4\text{-}6)$$

Duration of t_2 and t_3 will be determined by how long it takes gate driver to deliver all charge required.

$$t_x = \frac{Q_{G(x)}}{I_{DRIVER}} \quad (4\text{-}7)$$

T_3 is longer than t_2, switching happens at the voltage level "V_{SP}". V_{SP} is called switching point or switching voltage. Generally, V_{SP} can be approximated using the fallowing equation;

$$V_{SP} \approx V_{TH} + \frac{I_{OUT}}{G_M} \quad (4\text{-}8)$$

G_M is MOSFET's transconductance and V_{TH} is typical gate treshold voltage.

After defining V_{SP}, Klein (2006) determines gate current by Ohm's Low on the circuit at Figure 4.2.

$$I_{DRIVER(L\text{-}H)} = \frac{V_{DD} - V_{SP}}{R_{DRIVER(PULL\text{-}UP)} + R_{GATE}} \quad (4\text{-}9)$$

$$I_{DRIVER(H\text{-}L)} = \frac{V_{SP}}{R_{DRIVER(PULL\text{-}DOWN)} + R_{GATE}} \quad (4\text{-}10)$$

V_{GS} change during t_2 is from V_{TH} to V_{SP}. Approximating this as V_{SP} simplifies calculation considerably and introduces no significant error. This approximation allows to use the $Q_{G(SW)}$ term to represent the gate charge for a MOSFET to move through switching interval. $Q_{G(SW)}$ can be approximated by;

$$Q_{G(SW)} \approx Q_{GD} + \frac{Q_{GS}}{2} \quad (4\text{-}11)$$

So switching times therefore are:

$$t_{S(L\text{-}H)} = \frac{Q_{G(SW)}}{I_{DRIVER(L\text{-}H)}} \quad (4\text{-}12)$$

$$t_{S(H\text{-}L)} = \frac{Q_{G(SW)}}{I_{DRIVER(H\text{-}L)}} \quad (4\text{-}13)$$

Finally switching losses can be summarized as:

$$P_{SW} = \left\{ \frac{V_{IN} \times I_{OUT}}{2} \right\} \times F_{SW} \times \left(t_{S(L-H)} + t_{S(H-L)} \right) \quad (4\text{-}14)$$

In application circuit, high side MOSFET has fallowing switching timings;

$t_{S(L-H)}$= 8 nS (4-15)

$t_{S(H-L)}$=12 nS (4-16)

Calculated switching loss is 0.189 W. This small amount of loss is a result of choosing appropriate MOSFET for the application having short turn-on and turn-off values.

4.2.2 Low Side MOSFET Losses

Low side losses are combination of both conduction and switching losses.

$$P_{LS} = P_{SW} + P_{COND} \tag{4-17}$$

Switching losses could be neglected because Q_2 switches on and off with only diode drop across it, For completeness, switching losses are included in this thesis.

4.2.2.1 Low Side Conduction Losses. Conduction losses dominates low side losses. Low side losses can be named as $R_{DS(ON)}$ losses.

Klein (2006) described conduction losses for Q_2 as;

$$P_{COND} = (1 - D) \times {I_{OUT}}^2 \times R_{DS(ON)} \tag{4-18}$$

$R_{DS(ON)}$ is on resistance of MOSFET at predicted operating junction temperature. D is duty cycle of the converter.

$$D = \frac{V_{OUT}}{V_{IN}} \tag{4-19}$$

Low side MOSFET have 5 $m\Omega$ $R_{DS(ON)}$ in application circuit. Calculated conduction loss is 107 mW. As the conduction losses minimized, total circuitry runs in a cooler space having better thermal and electrical performance.

4.2.2.2 Low-side Switching Losses. Low side switching losses are negligable compared to low side conduction losses. For completeness of my research thesis they are included.

Low side switching losses can be calculated with a similar manner to high side switching losses. Instead of V_{IN}, schottky diode drop (V_F) will be used.

$$P_{SW(LS)} \approx \left\{ t_2 \times V_F + t_3 \times \frac{V_F + I_{OUT} \times 1.1 \times R_{DS(ON)}}{2} \right\} \times I_{OUT} \times F_{SW} \qquad (4\text{-}20)$$

The voltage collapse for Q_2 is caused by $R_{DS(ON)}$ going from $\frac{0.6}{I_{OUT}} @ V_{GS} = V_{SP}$ to 90% of V_{SPEC} (in Figure 4.4), gate voltage for the highest specified $R_{DS(ON)}$. At 90% of V_{SPEC}, $R_{DS(ON)}$ is typically 110% of the specified $R_{DS(ON)}$.

For low-side rising edge transition times (t_2 and t_3 in Figure 4.4) can be calculated from RC equations. (Klein J.,2006)

$$t_{2R} = K_{2R}(R_{DRIVER} + R_{GATE})C_{ISS} \qquad (4\text{-}21)$$

Where;

$$K_{2R} = \ln\left\{ \frac{V_{DRIVE}}{V_{DRIVE} - V_{SP}} \right\} - \ln\left\{ \frac{V_{DRIVE}}{V_{DRIVE} - V_{TH}} \right\} \qquad (4\text{-}22)$$

$$t_{3R} = K_{3R}(R_{DRIVER} + R_{GATE})C_{ISS} \qquad (4\text{-}23)$$

Where;

$$K_{3R} = \ln\left\{ \frac{V_{DRIVE}}{V_{DRIVE} - 0.9V_{SPEC}} \right\} - \ln\left\{ \frac{V_{DRIVE}}{V_{DRIVE} - V_{SP}} \right\} \qquad (4\text{-}24)$$

Where C_{ISS} is MOSFET's input capacitance (C_{GS}+C_{GD}) when V_{DS} is near 0V.

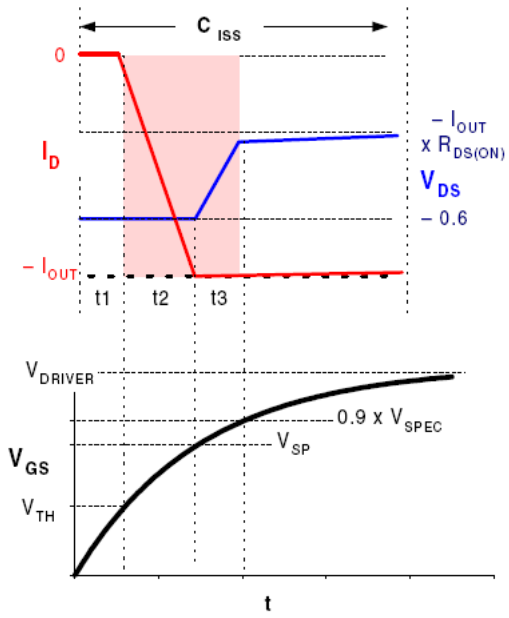

Figure 4.4 Low-Side turn-on switching loss waveforms

Turn off losses are same with turn on losses but in reverse manner. Switching waveforms are presented in Figure 4.5.

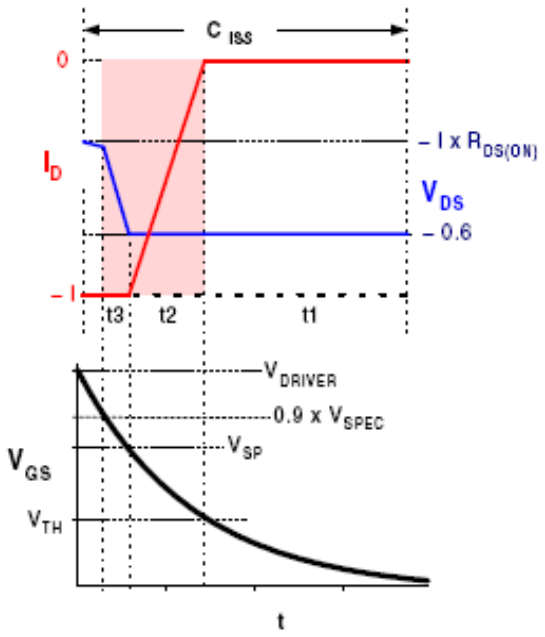

Figure 4.5 Low-Side turn-off switching loss waveforms

For low side, falling edge transition times (t_3 and t_2 in Figure 4.5) can be calculated from RC equations:

$$t_{3F} = K_{3F}\left(R_{DRIVER} + R_{GATE}\right)C_{ISS} \tag{4-25}$$

$$K_{3F} = \ln\left(\frac{0.9V_{SPEC}}{V_{SP}}\right) \tag{4-26}$$

$$t_{2F} = \ln\left(R_{DRIVER} + R_{GATE}\right)C_{ISS} \tag{4-27}$$

Where;

$$K_{2F} = \ln\left(\frac{V_{SP}}{V_{TH}}\right) \tag{4-28}$$

4.2.3 Dead-Time Losses

Dead-time is period that both MOSFETs are off. During this interval body diode or parallel schottky diode is in forward conduction. Power loss can be formulised as fallows;

$$P_{DIODE} = t_{DEADTIME} \times F_{SW} \times V_F \times I_{OUT} \quad (4\text{-}29)$$

Where $t_{DEADTIME}=t_{DEADTIME(R)} + t_{DEADTIME(F)}$, which is deadtimes associated before SW Node at Figure 4.1 rises, after Q_2 turns off, and after SW Node falls, before Q_2 turns on, respectively.

Diode will be in conduction for $t_{DEADTIME(F)}$ starting from falling of switch node, until low-side MOSFET reaches treshold. This period consists of two portions:

$t_{DELAY(F)}$: Driver's built in delay time from closing high-side MOSFET gate until beginning of low-side MOSFET turn-on.

t_{TH}: Required time to charge low-side MOSFET's gate to treshold voltage (V_{TH}). T_{TH} can be approximated by;

$$t_{TH} \approx \frac{Q_{GS}}{2 \times I_{LDRV}} \quad (4\text{-}30)$$

Approximation is prior to until reaching treshold, gate voltage is low enough that low-side driver curent (I_{LDRV}) can be approximated with a constant current of;

$$I_{LDRV} \approx \frac{V_{DRIVER} - \left(\frac{V_{TH}}{2}\right)}{R_{GATE} + R_{DRIVER}} \quad (4\text{-}31)$$

Typically;

$$Q_{G(TH)} \approx \frac{Q_{GS}}{2} \tag{4-32}$$

Diodes total on-time on falling edge is then:

$$t_{DEADTIME(F)} \approx t_{DELAY(F)} + \frac{Q_{GS}(R_{GATE} + R_{DRIVER})}{\left(V_{DRIVER} - \frac{V_{TH}}{2}\right)} \tag{4-33}$$

Rising edge delay, $t_{DELAY(R)}$, is much longer to allow low side MOSFET's gate to discharge completely. $t_{DELAY(R)}$ should be longer since charge is coupled during rising edge of SW node. Peak of resultant voltage spike at low-side gate is sum of the amplitude of injected spike and voltage level gate has discharged when the SW node begins to rise. Longer rising edge delays should be necessary because resulting voltage spike might be over threshold voltage of low-side MOSFET. If so turning on both MOSFETs occurs and shoot through losses arises. Shoot through and some prevention methods is mentioned in Chapter Three Shoot Through in Synchronous Buck Converters.

In application circuit, dead time losses are minimized by using schottky diode injected into low side MOSFET. Comparison between using body diode and paralell schottky diode is mentioned in "4.2.6.3 External Schottky" section. Dead time is approximately 30 nS. Dead time is long enough to maintain switching and short enough to prevent efficiency loss.

4.2.4 Inductor Losses

Inductance is the main parameter that provides desired circuit function and is the first parameter to be calculated in most design procedures. Inductance is calculated to provide a certain minimum amount of energy storage (or volt-microsecond capacity) and to reduce output current ripple. Using less than calculated inductance causes

increased ac ripple on dc output. Using much greater or much less inductance may force converter to change between continuous and discontinuous modes of operation.

For a buck converter, inductor current equals to load current. As the whole load current flows through inductor, it has a nonnegligible role over efficiency point of view. DC resistance and AC resistance values define losses of the inductor.

4.2.4.1 DC Resistance Losses. DC resistance (DCR) is simply a measure of wire used in inductor. It is based on wire diameter and length. DCR varies with temperature in the same manner as resistivity of winding material. (Crane L., 2005) It is important that DCR rating makes note of ambient temperature. DCR versus temperature graph of a typical inductor is shown in Figure 4.6. Also, temperature of inductor varies as load current flows through. Heating inductor results increase of DCR and DCR based losses.

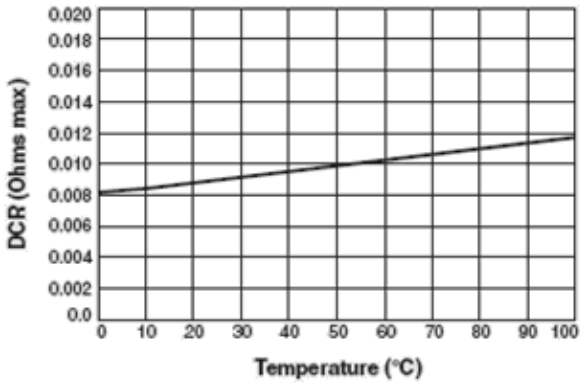

Figure 4.6 Expected DCR at 25°C.

DC resistance losses can be formulised as follows;

$$DCR\ Losses = I_{dc}^2 \times R_{DCR} \tag{4-34}$$

Size of the inductor is inversely proportional to the DC resistance. As the size of inductor is to be minimized, DCR rating will be maximized. Typically reducing DCR

means having to use larger wire and probably a larger overall size. So optimizing DCR selection is a tradeoff of power efficiency, allowable voltage drop across inductor, and size.

In application circuit, DCR of inductor is 3 $m\Omega$ at $40^{\circ}C$. Resultant DCR loss over inductor is 75 mW at 5 Ampere load current. Power loss over inductor is considerably low. Inductor runs cool and DCR does not varies with temperature and increase overall system temperature.

4.2.4.2 AC Resistance Losses. Resistance of most inductor windings increases with operating frequency due to skin effect. If ac or ripple current is relatively small compared to average or dc current then DCR gives a good measure of resistive loss to be expected. Skin effect varies with wire diameter and frequency, so to include this data would require a full frequency curve for each inductor.

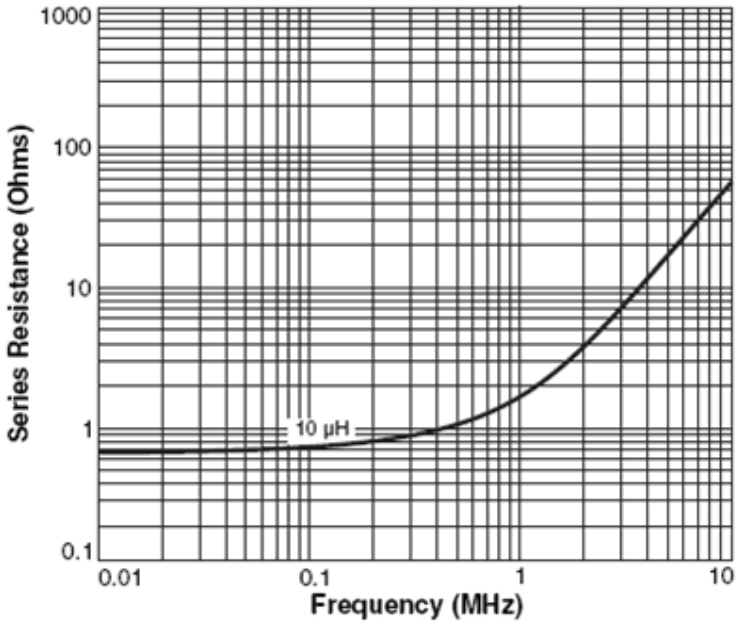

Figure 4.7 Series Resistance (AC Resistance+DC Resistance) versus Frequency Curve

AC resistance losses can be formulised as follows;

$$AC\ Losses = I_{(p-p)rms} \times R_{AC} \tag{4-35}$$

$$I_{(p-p)rms} = \frac{I_{p-p}}{\sqrt{3}} \tag{4-36}$$

Where $I_{(p-p)rms}$ and I_{p-p} are peak to peak rms ripple current and peak to peak ripple current respectively.

AC Resistance is not typically a concern unless either operating frequency or ac component of current is large with respect to dc component. For most applications working below 500 kHz, it is not necessary. As can be seen from Figure 4.7, ac resistance does not become comparable to dc resistance at frequencies below 200 kHz. Even above that frequency ac resistance will not be an issue if ac current is not large compared to dc component.

4.2.5 Capacitor Losses

Changing topology in ICs and other semiconductors, it is easy to think capacitors as a design constant. While many capacitors look similar to their duplicates of a few years ago, capacitor technology has continued to evolve. Nowadays capacitors are more reliable, offer higher capacitance densities and more mounting options. (Gebbia M., 2001) One of the parameters that has recently come under closer investigation by designers is equivalent series resistance (ESR). Stated in ohms and referenced to specific frequencies. ESR is easier to define than it is to specify.

Equivalent circuit of a capacitor is made up of three basic characteristics as shown in Figure 4.8, impedance, equivalent series resistance and equivalent series inductance (Z, ESR and ESL) are frequency dependant variables. During capacitor losses part of my thesis, there will be one additional component called capacitive reactance (Xc).

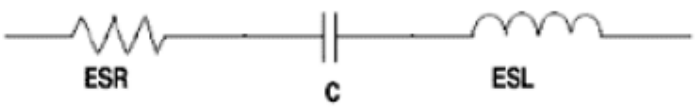

Figure 4.8 Capacitor equivalent circuit.

ESR is the electrical resistances in series with capacitor plates including resistance of metal leads, plates and connections between them. Expressed mathematically as

$$ESR = \frac{D.F}{(2\pi fC)} = D.F \times X_C \tag{4-37}$$

Where D.F. = dissipation factor, f = frequency, C = capacitance and X_c = capacitive reactance. X_c is defined as $\frac{1}{(2\pi fC)}$.

Z is impedance of the capacitor. It is expressed mathematically as

$$Z = \sqrt{(ESR)^2 + (ESL - X_c)^2} \tag{4-38}$$

ESL, equivalent series inductance is sum of all inductive components within a capacitor and expressed mathematically as

$$ESL = 2 \times \pi \times f \times L \tag{4-39}$$

Where F is frequency and L is inductance.

It is important to note, ESR will change to a lower value as frequency increases. Behavior of ESR, ESL, Z and X_c characteristics with frequency is illustrated in Figure 4.9. (Gebbia M., 2001) Since all capacitors behave in a similar manner, ESR can be lowered by either using a higher capacitance value or by using a capacitor

with a lower D.F.. Lowering ESR by using a higher capacitance value is quite obvious, and no explanation is needed. Lowering of ESR by use of a dielectric that has a lower D.F. is more illustrative.

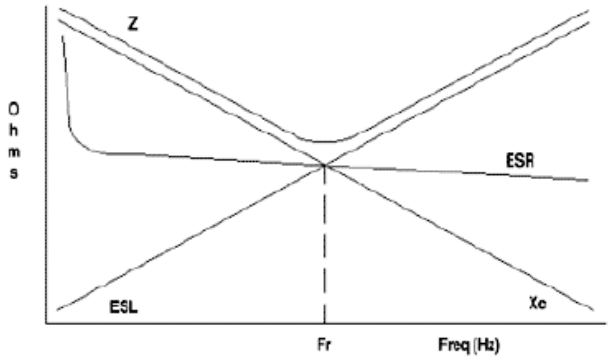

Figure 4.9 Frequency response characteristics of a capacitor where Fr is self resonance frequency.

Two types of circuits are more severely affected by ESR than others; those using high frequencies or high currents. Circuits which don't have either condition can tolerate much higher levels of ESR. This is the main reason why low ESR and low impedance capacitors are used extensively in switching power supplies to maintain performance of power supplies. Power loss due to ESR over a capacitor is;

$$P_{LOSS} = I^2 \times ESR \tag{4-40}$$

Capacitors having high ESR will self-heat due to power loss and can not regulate current properly. Obviously self-heating will reduce operating life of capacitors, switching power supply performance and life will be reduced. Additionally, low impedance capacitors have higher ripple current ratings than standard capacitors, thus reducing the number of capacitors is needed and helping to reduce size of switcher circuitry.

In application circuit, two 330 uF polymer capacitors with 9 $m\Omega$ ESR rating is used. Because of efficiency and limited space constraint polymer capacitors are

widely utilized in portable applications. Polymer capacitors have high capacitance and ESL values maintaining low ESR rating. They are placed to supply huge amount of charge at transient load demands.

In addition to polymer capacitors, there are four ceramic capacitors in application circuit. Ceramic capacitors have low capacitance value, low ESR and low ESL ratings. They are used to filter output voltage ripple and placed with polymer capacitors to minimize output ripple. Total ESR rating with each ceramic and polymer capacitors placed in paralel is 1.6 $m\Omega$. Calculated ESR loss for 5 Ampere output current is 40 mW. Operating life of capacitors and switching power supply performance is increased due to reduced power loss.

4.2.6 Additional Small Losses

There are some additional small losses compared to the mentioned losses above. Their impact on total efficiency is low, but they can be significant because of where dissipation occurs. Those losses mentioned in order of importance.

4.2.6.1 Power To Charge The Gate. PGATE is the power required from V_{DD} supply to drive a MOSFET gate including both rising and falling edges.

$$P_{GATE} = Q_G \times V_{DD} \times F_{SW} \tag{4-41}$$

It is distributed between driver resistance R_{DRIVER}, gate resistance R_{GATE} and external resitor R_{EXT}. Dissipation for rising and falling edges are as fallows respectively;

$$P_{DR(L\text{-}H)} = \frac{P_{GATE} \times R_{DRIVER(PULL\text{-}UP)}}{2(R_{TOTAL})} \tag{4-42}$$

Where;

$$R_{TOTAL} = R_{DRIVER} + R_{GATE} + R_{DAMPING} \quad (4\text{-}43)$$

$$P_{DR(H\text{-}L)} = \frac{P_{GATE} \times R_{DRIVER(PULL\text{-}DOWN)}}{2(R_{TOTAL})} \quad (4\text{-}44)$$

Gate charge losses can not be calculated or estimated at application circuit due to the nature of components are not ideal. Also, printed circuit board (PCB) trace resistance is so small compared to driver and damping resistor values. Turn-on and turn-off period of MOSFET varies when external damping resistor is used.

4.2.6.2 Power To Charge Output Capacitance Of MOSFET. Power to charge output capacitor of a MOSFET can be formulised as;

$$P_{COSS} \approx \frac{C_{OSS} \times V_{IN}{}^2 \times F_{SW}}{2} \quad (4\text{-}45)$$

Where C_{OSS} is output capacitance of MOSFET(C_{DS}+C_{DG}).

In application circuit, C_{OSS} is 323 pF. Calculated power loss to charge output capacitance is 7.691 mW. Magnitude of loss is minor compared to switching or conduction losses. Obviously, it is a negligible loss.

4.2.6.3 External Schottky. Notebook and battery powered applications have high efficiency constraint to maximize battery life time. External schottky diode can be placed parallel to low side MOSFET. During dead time, return current flows through external schottky instead of MOSFET body diode. Schottky diodes have smaller capacitance than body diode ouput capacitance.

If an external schottky is used across Q_2, schottky capacitance needs to be charged during high-side MOSFET's turn-on:

$$P_{C(SCHOTTKY)} = \frac{C_{SCHOTTKY} \times V_{IN}{}^{2} \times F_{SW}}{2} \quad (4\text{-}46)$$

If schottky diode is not used reverse recover power for Q_2 body diode of MOSFET is:

$$P_{QRR} = Q_{RR} \times V_{IN} \times F_{SW} \quad (4\text{-}47)$$

Q_{RR} is body diode's reverse recovery charge. MOSFET could have an integrated body diode. In this situation the Q_{RR} is actually Q_{oss} (Output charge Q_{oss} is sum of Q_{GD} and Q_{GS}).

Regarding external schottky, resultant efficiency ratings might be higher up to 3 percent. In application circuit, low side MOSFET have internal schottky diode parallel to body diode. There is no extra PCB trace inductance with internal schottky diode. Also external component count is reduced due to limited space.

4.3 Efficiency Of Application Circuit

Efficiency is a critical parameter that has to be considered during power supply desing. Chain of decisions and choosing proper components suitable for the application influence resultant efficiency.

Selection of MOSFETs for low and high side differs from each other. Low side MOSFET should have small $R_{DS(ON)}$, because conduction losses are dominant for low side. Turn on and tun off time is not a constrict for low side. Switching behaviour is significant for high side MOSFET. Turn on and turn off time should be short to decrease switching losses.

Inductors with low DC Resistance (DCR) have incontrovertible effect over efficiency. Having low DCR means smaller loss over inductor and cooler run for

power circuitry. As the volume of inductor increases, DCR decreases. Volume constrain of portable devices forces designers to select inductors close to limits. Inductor selection should be done due to efficiency and volume criteria.

Capacitors having low ESR results better performance. In application circuit, there are two poscaps to supply charge for transient load demands and four ceramic capacitors for ripple reduction. Lower ESR capacitors have smaller loss, cooler run and higher ripple capability.

In application circuit, maximization of efficiency is considered from start to end. Component selection and gate driver performance is optimized and explained in every stage of my research thesis. Shoot through which decreases efficiency is prevented at “Chapter Three Shoot Trough In Synchronous Buck Converters”. Application circuit efficiency measurement is done at 300 kHz switching frequency and can be seen in Table 4.1 and Figure 4.10. Average efficiency for the entire load range is %93,85.

In application circuit, efficiency measurement should be done carefully. There should be no quiescent current to the rest of the circuit. Power shorts are used to prevent quiescent current in the application circuit. They are placed at the input and output of the mosfets, and also at the battery voltage rail feeding controller IC to maintain complete isolation. While getting efficiency measurements these power shorts are opened, but during normal operation they are shorted.

To conclude, overall efficiency is pretty high to maintain longer battery life. Chain of decisions, proper component selection and gate drive optimization result increased efficiency ratings.

Table 4.1 Efficiency table of the application circuit

Efficiency & Load Regulation					
Vin	**Iin**	**Vout**	**Iout**	**Effi.**	**Notes**
12.6	0	1.83	0	0	
12.6	0.031	1.828	0.204	0.954715822	
12.6	0.062	1.8275	0.4	0.935739887	
12.6	0.095	1.8275	0.601	0.917566834	
12.6	0.126	1.8275	0.804	0.925491308	
12.6	0.158	1.8265	1.014	0.930314949	
12.6	0.195	1.82	1.254	0.928888889	
12.6	0.234	1.814	1.51	0.929025912	
12.6	0.262	1.81	1.706	0.935375015	
12.6	0.31	1.805	2.006	0.926991807	
12.6	0.348	1.805	2.261	0.930739144	
12.6	0.383	1.805	2.501	0.935452153	**Fs=300kHz L=1.5uH**
12.6	0.42	1.805	2.756	0.940018896	
12.6	0.458	1.805	3.012	0.942098149	
12.6	0.527	1.801	3.508	0.95146351	
12.6	0.601	1.8005	4.001	0.951298167	
12.6	0.678	1.8	4.512	0.950695322	
12.6	0.753	1.7995	5.008	0.949840427	
12.6	0.828	1.799	5.503	0.948920424	
12.6	0.906	1.7985	6.012	0.94717597	
12.6	1.059	1.797	7.003	0.943117271	
12.6	1.216	1.7955	8.009	0.938554688	
12.6	1.372	1.7945	9	0.934246147	

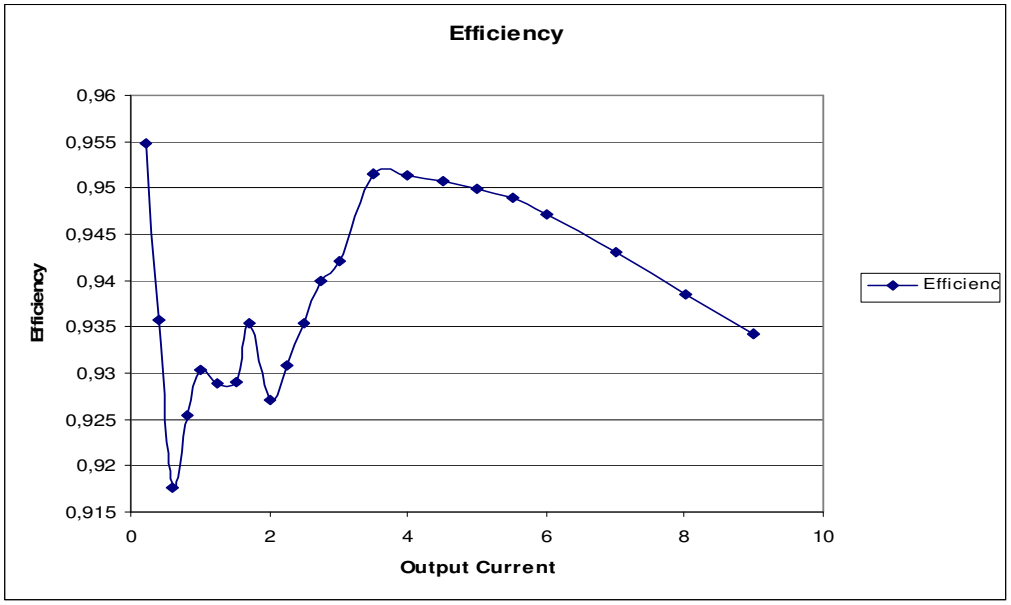

Figure 4.10 Efficiency graph of the application circuit

CHAPTER FIVE

PULSE FREQUENCY MODULATION

Overall system efficiency is a critical design parameter in battery powered systems. It affects both battery capacity requirement and end product's run time. Most battery powered systems take advantage of a power supply feature called pulse frequency modulation (PFM) to improve power supply efficiency at light loads.

5.1 Pulse Frequency Modulation

"Pulse frequency modulation (PFM) is a control method to stabilise output voltage by modulating switching pulse output frequency while pulse width is constant." (Torex, 2004) This method is also referred to as burst mode and power save mode (PSM). There is one primary advantage that PFM has over traditional PWM schemes: it reduces power dissipation of converter at light loads. To compare with PFM control, PWM control can be defined as a method to stabilise output voltage by modulating pulse width while switching pulse output frequency is constant and can be seen at Figure 5.1.

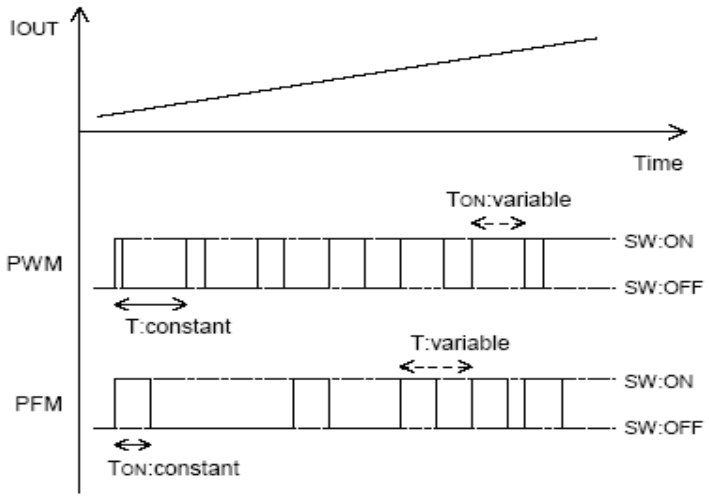

Figure 5.1 PWM control /PFM control timing chart - ON/OFF switching by output current

A switching converter has two types of power losses: static and dynamic. Static losses are constant, regardless of load current. Alternatively, dynamic losses increase with load current. (Day M. & Naik J. 2007) An example of a static loss is quiescent current going into an IC. This current is used to power internal circuitry such as bandgap references, operational amplifiers (opamps), internal clocks. In turn, dynamic losses can be classified by two categories: conduction losses and switching losses. Conduction losses are load dependent and include losses caused by voltage drops across power supply's power MOSFETs and inductor. Higher load currents result in higher conduction losses. A converter also has frequency dependent switching losses that include MOSFETs' turn-on and turn-off losses, gate drive losses that occur at each switching cycle. As name implies, these losses are proportional to switching frequency. Most of them are also dependent on load. Figure 5.2 shows static and dynamic power losses for low-power ICs. This figure shows that dynamic losses are dominant at higher output currents, while static losses are dominant at lower output currents. PFM architecture have benefits to minimize both dynamic and static losses.

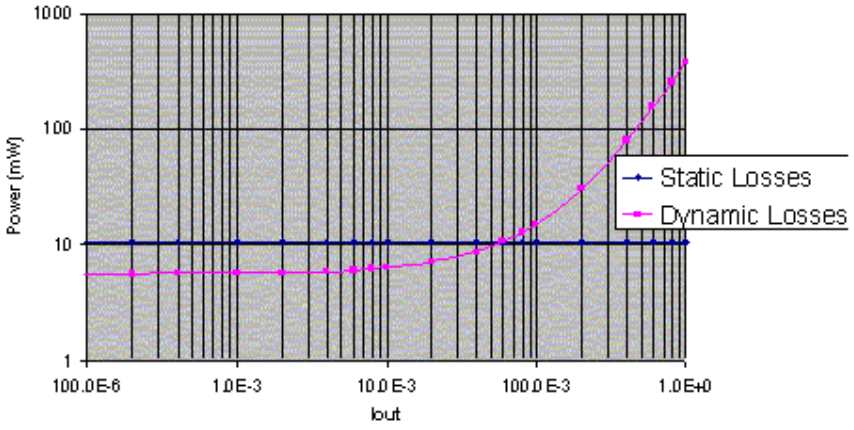

Figure 5.2 Switching converter static and dynamic losses

In an effort to reduce power loss at light loads, many converters operate in "power save" mode. This mode utilizes PFM type of operation at light load currents. This type of operation uses several power saving schemes to maintain high efficiency at light loads. In contrast to PWM mode, in which converter is continuously switching,

PFM mode allows the converter to switch in short bursts. While in PFM mode, converter only switches as necessary to service load and maintain output voltage. When output voltage drops below its set point, IC begins switching. As the IC switches, output voltage rises. This may take one or several switching cycles. Once output rises above regulation threshold, converter stops switching. Output voltage then drops as output capacitor supplies load current. When output voltage drops below threshold, converter starts up and switches again. Significant power savings are achieved when converter is not switching. When not switching, converter significantly reduces its quiescent current by shutting down all unnecessary internal circuitry. Only active internal circuitry is bandgap reference and a comparator to monitor output voltage. With no switching, all switching losses go to zero. Most converters operate in discontinuous conduction mode (DCM) while in PFM mode. Hence inductor current becomes discontinous (Figure 5.3). Drawback of PFM operation is high output voltage ripple due to discontinous inductor current. Inductor peak current can be formulized as:

$$i_L(D_1T_S) = i_{peak} = \frac{V_g - V}{L} D_1 T_S \tag{5-1}$$

Inductor average current is;

$$i_L = \frac{1}{T_S} \int_0^{T_S} i_L(t)dt \tag{5-2}$$

$$i_L = (V_g - V)\frac{D_1 T_S}{2L}(D_1 + D_2) \tag{5-3}$$

Where D is duty cycle of PFM signal and T_S is period of PFM signal. D is changing from 0 to 1.

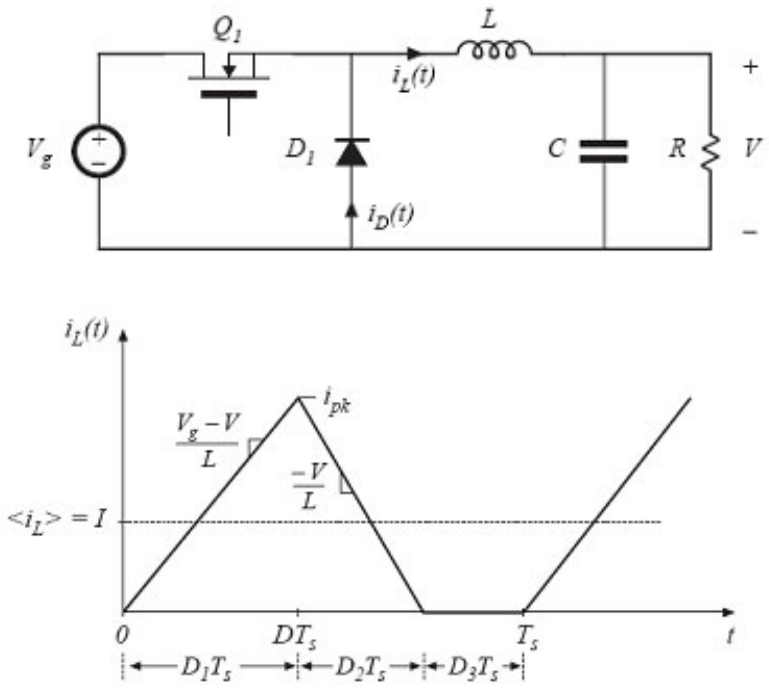

Figure 5.3 Inductor Current and related buck circuit

Figure 5.3 shows inductor curent during PFM mode operation. (Erickson R. W. & Maksimovic D.,2001) PFM keeps inductor current going negative, which would otherwise generate unnecessary conduction losses in both the inductor and power switches. Effect of power saving schemes is significant increase in light load efficiency versus standard PWM operation.

5.2 Efficiency Of Application Circuit Having Pulse Frequency Modulation

Efficiency is measured from the application circuit having Pulse Frequency Modulation (PFM). Results can be seen on Table 5.2. Also, same measurement is done from the application circuit using Pulse Width Modulation (PWM) control technique to observe the rate of change in efficiency. Table 5.1 shows the results with PWM. Efficiency of PWM mode operation (Table 5.1) has an average rating of %77.76 over 0 to 0.35A load range. On the other hand, efficiency of PFM mode operation (Table 5.2) has an average rating of %96.51 over the same load range. In addition to that, PFM mode has a 30 percent increase in efficiency versus PWM

mode at 100mA load current. Point to point efficiency comparison can be seen at Figure 5.4.

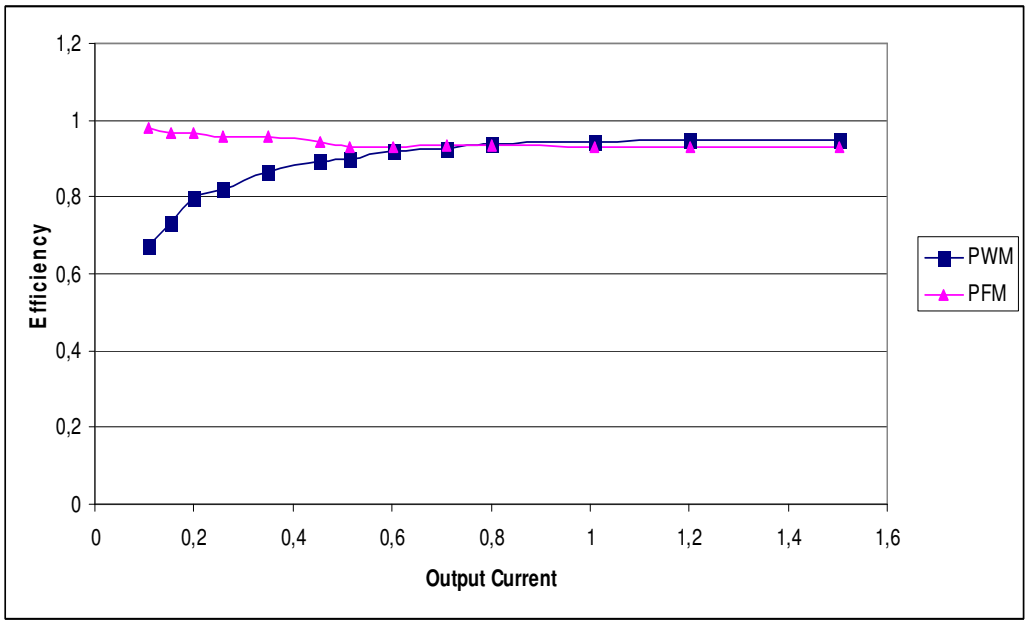

Figure 5.4 Efficiency comparison between PFM and PWM modes performing accurate efficiency measurements

Table 5.1 Efficiency table for PWM mode

Efficiency & Load Regulation					
Vin	**Iin**	**Vout**	**Iout**	**Effi.**	**Notes**
12,6	0,023	1,807	0,108	0,673416	
12,6	0,03	1,807	0,153	0,731405	
12,6	0,036	1,8065	0,2	0,796517	
12,6	0,045	1,8065	0,258	0,822005	
12,6	0,058	1,806	0,35	0,864943	**Fs=300kHz L=1.5uH PWM MODE**
12,6	0,073	1,806	0,455	0,893379	
12,6	0,082	1,806	0,513	0,896707	
12,6	0,094	1,8055	0,603	0,919214	
12,6	0,11	1,8055	0,71	0,924895	
12,6	0,122	1,805	0,8	0,93937	
12,6	0,153	1,8045	1,008	0,943529	
12,6	0,181	1,804	1,201	0,950015	
12,6	0,227	1,803	1,503	0,947454	

Table 5.2 Efficiency table for PFM mode

Efficiency & Load Regulation					
Vin	**Iin**	**Vout**	**Iout**	**Effi.**	**Notes**
12,6	0,016	1,827	0,108	0,97875	**Fs=300kHz L=1.5uH PFM MODE**
12,6	0,023	1,827	0,153	0,964565	
12,6	0,03	1,8265	0,2	0,966402	
12,6	0,039	1,8265	0,258	0,958968	
12,6	0,053	1,8265	0,35	0,957285	
12,6	0,07	1,8255	0,455	0,941726	
12,6	0,08	1,8265	0,513	0,929558	
12,6	0,094	1,826	0,603	0,92965	
12,6	0,11	1,8265	0,71	0,935653	
12,6	0,124	1,826	0,8	0,934972	
12,6	0,157	1,826	1,008	0,930446	
12,6	0,187	1,825	1,201	0,930237	
12,6	0,233	1,8165	1,503	0,929968	

As a result, light load efficiency is critical to extend battery life in portable applications. PFM mode uses several techniques to improve light load efficiency. According to results measured from the application circuit, PFM has %18.75 increase in efficiency over the entire load range starting 0 to 0.35A. Especially, when battery powered system is in standby or sleep condition, load current for different voltage rails decreases. PFM feature have significant advantage in this condition.

Drawback of PFM control is high ripple at output voltage. Switching and electromagnetic noise occurs at the output when MOSFETs are switching. For noise sensitive applications, it is not recommended to use PFM mode. RF applications, combination of signal integrity and low power operation such as personal navigation systems, portable audio devices, digital still cameras, handheld games are sensitive to noise associated with dc power management.

CHAPTER SIX

PROTECTING THE SWITCHER

Voltage Regulator Module works in safe region during normal operation conditions. A sudden transient load effect or fault condition may give hazardous damage to regulator module and the whole circuitry. A short circuited component, burnt IC or over current may cause damage. Excesive current over power components may flow. One of the problems resulting from over current fault is that extreme heat may be generated in power devices, especially on MOSFET's and schottky diodes and temperature of those components may exceed their specified limits. A protection mechanism has to be used to prevent those power devices from being damaged.

6.1 Current Limiting Methods

There are some protection methods in a power supply whose purpose is to protect whole circuitry from being damaged during an over-current fault condition. There are many ways of protecting power supply when it is over-loaded, such as hiccup-mode, maximum current limiting or current foldback methods.

6.1.1 Maximum Current Limiting

In this method, load current is limited to a set maximum value when current demand of load is higher than limit value. As a result, output voltage will drop. Output voltage and load current relationship is shown in Figure 6.1. Power dissipation in power supply is usually higher in current limiting stage than in normal operation, as an example power dissipation at point B, as shown in Figure 6.1, is larger than that at point A. In order to protect power supply, system must be designed to handle worst case thermal dissipation at point C.

Power dissipation can be calculated as fallows;

$$P_h = I_{o,\max} \times V_D \times D \quad (6\text{-}1)$$

Where V_D is Schottky diode forward voltage and D is duty cycle.

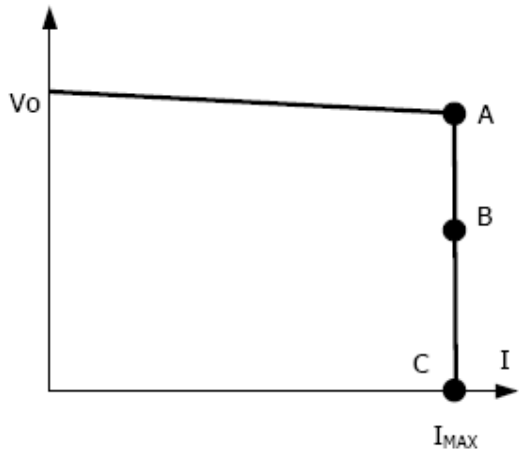

Figure 6.1 I-V curve for a power supply with maximum current limiting

At Maximum Current Limiting, any further increase in load current will cause output voltage to drop. As an extreme case, when output is short-circuited, output voltage will drop to zero. On duty ratio of MOSFET for this case is 0% and on duty ratio for schottky diode is 100%.

6.1.2 Current Foldback

Current foldback protection reduces load current when over-current fault occurs. I-V curve is shown in Figure 6.2. (Microsemi, 1998) Because of current foldback, worst power dissipation is at point A, hence, heat sink in this case is smaller than that in the maximum current limiting case. Heat generated when output short-circuited is;

$$P_h = \frac{1}{3} I_{o,\max} \times V_D \times D \quad (6\text{-}2)$$

Where V_D is Schottky diode forward voltage and D is duty cycle.

The drawback is that it provides less current at start up, hence output rises slower, or power supply may not start up at all if load current during start up is larger than foldback current. To solve this problem, current limit circuitry is off during start up period up to a few hundred miliseconds. When output voltage settles its nominal value, protection circuitry is on again.

As a result, current foldback method reduces output current as output load increases. Assuming foldback current is only 1/3 of the maximum current when output voltage is zero. At over current instant, heat generated over inductor and switching components is lower compared to maximum current limiting method. Current foldback method is not still a perfect solution to protect whole circuitry.

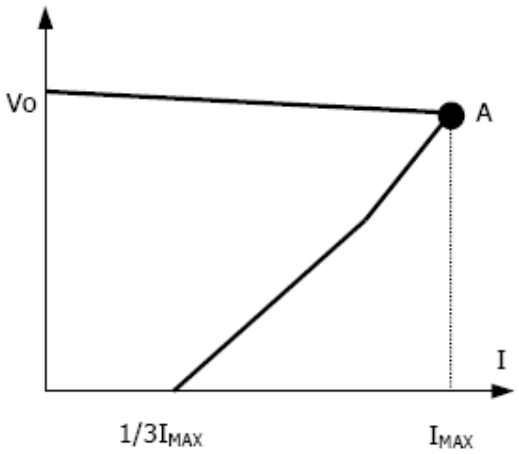

Figure 6.2 I-V curve of a power supply with current foldback

6.1.3 Hiccup-mode Operation

When current sense circuit sees an over-current event, controller shuts off power supply for a given time and then tries to start up the power supply again. If over-load condition has been removed, power supply will start up and operate normally; otherwise, controller will see another over-current event and shut off power supply again, repeating the previous cycle (Figure 6.3). Hiccup operation has none of drawbacks of the other two protection methods, although its circuit is more

complicated because it requires a timing circuit. Excess heat due to overload lasts for only a short duration in hiccup cycle, hence junction temperature of power devices is much lower. Hiccup operation can be done in various ways. For example, one can start hiccup operation any time an overcurrent event is detected; or prohibit hiccup during a designated start-up interval (usually a few milliseconds). Reason for latter operation is that during start-up, power supply needs to provide extra current to charge up output capacitor. Thus current demand during start-up is usually larger than during normal operation and it is easier for an over-current event to occur. If power supply starts to hiccup once there is an over-current, it might never start up successfully.

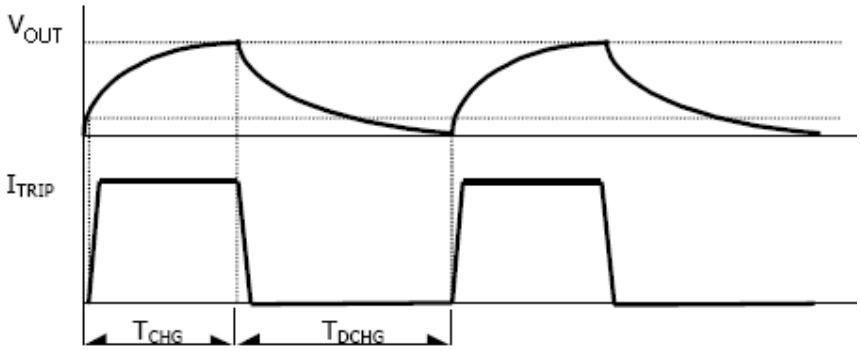

Figure 6.3 The Output capacitor voltage (top) and the inductor current (bottom) waveforms during hiccup operation.

6.2 Protection Behaviour Of Application Circuit

In application circuit, lossless hicc-up mode current limit method is utilized. Drain to source voltage drop of low side MOSFET is monitored. Voltage drop between phase node and ground is sensed and on-resistance of the rectifying MOSFET is used as current sensing element. If magnitude of inductor current is above the current limit treshold, controller does not initiate a new cycle.

Protection behaviour of application circuit is obsorved under short circuit condition. During short circuit, output current increases over the current limit level of regulator. Current limit is the safe operating range that voltage regulator manage to

supply current. Current capability of MOSFETs, saturation current of inductor defines the current limit value for a voltage regulator. In application circuit, output current is limited to 10 A.

Figure 6.4 shows over current behaviour of application circuit. Voltage regulator output is forced to short circuit condition at point A at Figure 6.4. Voltage regulator attempts to supply increased current demand until point B at Figure 6.4. As output current continues to increase, voltage regulator stops switching starting from point B. Output current discharges to zero at point C. Total elapsed time from short circuit instant to discharged inductor current is approximately 100 uS. Short circuit response time is reasonably abbreviated to protect power supply circuit.

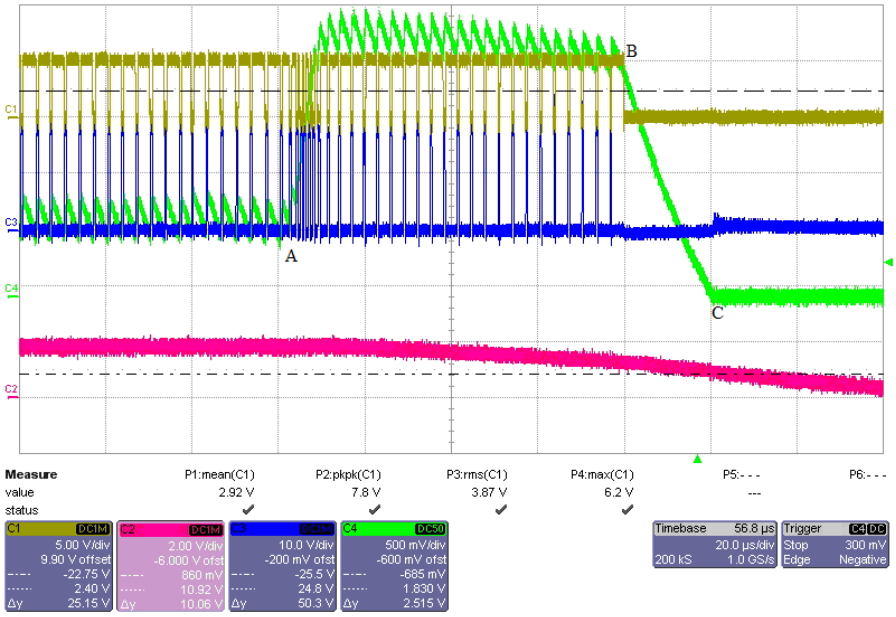

Figure 6.4 Low side gate drive (C1), output voltage (C2), high side gate drive (C3), inductor current (C4) waveforms of Intel Montevina Platform DDR Voltage Rail

CHAPTER SEVEN

CONCLUSION

The aim of my research thesis is to examine voltage regulators having synchronous buck converter topology. They offer many advantageous such as high efficiency, lower power loss and smaller size, though their designs are complicated. Due to abstruse design parameters compared to linear regulators, special techniques need to be used at the design and performance optimization stages. On this occasion, application circuit is built on Intel Montevina Platform Notebook Computer DDR Voltage Rail is used to demonstrate performance optimization techniques.

Application circuit, in synchronous buck converter topology, is formed by controller IC, MOSFETs, inductor, input capacitors, output capacitors and several passive components to control converter dynamics. Components comprising buck converter will lead losses. Choosing the appropriate components influence a key role to minimize losses. Total power loss during DC-DC conversion defines system efficiency, so battery life for portable devices.

Shoot through is a critical design phenomenon for Synchronous Buck Converters. Hazardous damages because of excessive current flow over power components, loss of efficiecny and increase in component temperatures may arise. Effect of various MOSFETs on shoot through having different $\frac{Q_{gd}}{Q_{gs1}}$ ratio is demonstrated. MOSFET with $\frac{Q_{gd}}{Q_{gs1}}$ ratio smaller than 1 or close to 1 fitting the application examined in this thesis is choosen.

One of the parameters to prevent shoot through is to place capacitor parallel to low side gate source capacitance. From application circuit, it is seen that, placing this capacitor reduces $C\frac{dv}{dt}$ induced voltage by %31. In some cases, placing paralel capacitor is not enough to prevent shoot through. Slowing down high side MOSFET

is the further move. Small series resistor value can be placed to high side gate drive way to slow down the MOSFET. This resistor benefits to prevent shoot trough compromising efficiency. Extention of switching interval decreases the efficiency.

Pulse frequency modulation (PFM) is the approved control method to maximize efficiency at light load. PFM has a significant advantage compared to pulse width modulation (PWM). Average efficiency value is increased %30 in PFM. Drawback of the PFM control method is high ripple at output voltage. For noise sensitive applications, it is venturing to use PFM control method in spite of efficiency phenomenon.

To protect power supply circuit from hazardous damages, maximum current limiting, current foldback, hiccup mode protection methods is introduced. In application circuit hiccup mode current protection is used. In hiccup mode, further current increase over current limit settings will lead to shutting off. This behaviour is the safest way to protect converter and rest of the circuit it is supplying power. Any temperature rise and loss of efficiency will occur in this method.

REFERENCES

Brown J. (2006) "Modeling the switching performance of a MOSFET in the high side of a non-isolated Buck Converter Power Electronics" *IEEE Transactions on Volume 21, Jan. 2006 Page(s): 3 – 10*

Chang C. (2004) "Mixed voltage /current mode control of PWM synchronous buck converter" *Power Electronics and Motion Control Conference. The 4th International Volume 3, 14-16 Aug. 2004 Page(s): 1136 - 1139 Vol.3*

Crane L. (2005) *Selecting the Best Inductor for Your DC-DC Converter.* Retrieved October 4, 2007 from http://www.coilcraft.com/pdfs/Doc469_selecting_inductors.pdf

Current and temperatureratings (n.d.) Retrieved February 20, 2008, from http://www.coilcraft.com/pdfs/Doc361_Current&Temp.pdf

Day M. & Naik J. (2007) *A practical guide to low power efficiency measurements.* Retrieved January 5,2008 from www.networksystemsdesignline.com

Dunn J. (2002) Matching *MOSFET Drivers to MOSFETs.* Revised 2002 Retrieved September 28, 2007 from http://www.freeweb.hu/t-t/elokep/pic/download/an799a.pdf

Eirea G. (2006) PHD Thesis: Estimation and Control Techniques in Power Converters

Erickson R. W., & Maksimovic D. (2001) *Fundamentals of Power Electronics* (2nd Ed.) Springer

Fairchild (1998) *Suppressing MOSFET Gate Ringing in Converters: Selection of a Gate Resistor* Retrieved July 24, 2007 from www.fairchildsemi.com

Garcia N. (2005) *Determining Inductor Power Losses* Revised Retrieved December 10, 2008 from http://www.coilcraft.com/pdfs/doc486_InductorLosses.pdf

Gebbia M. (2001) *Low ESR capacitors: Fact or fiction?* Retrieved December 7, 2007 from http://www.ecnmag.com

Huang W. H. ,& Chien C. C.,& Chen H. K.,& Kuo S. Y. (2006) "Highly Efficient Tri-Mode Control of Buck Converters with Load Sensing Technique" *Power Electronics Specialists Conference*, 2006. *IEEE Volume No:37*, *18-22 June 2006 Page(s):1 – 4*

Klein J. (2003) *Shoot-through in Synchronous Buck Converters*. Retrieved January 6,2008 from www.fairchildsemi.com

Klein J. (2006) *Synchronous buck MOSFET loss calculations.* Retrieved May 27, 2008 from www.fairchildsemi.com

Kursun V., & Narendra S. G., & De V. K.,& Friedman E. G. (2003) "Monolithic DC-DC converter analysis and MOSFET gate voltage optimization" *Quality Electronic Design Proceedings. Fourth International Symposium*, *24-26 March 2003 Page(s): 279 – 284*

Kursun V.,& Narendra S. G., & De V. K., & Friedman E.G. (2002) "Efficiency analysis of a high frequency buck converter for on–chip integration with a dual–VDDmicroprocessor" *Solid-State Circuits Conference Proceedings of the 28th European Volume, 24-26 Sept. 2002 Page(s): 743 – 746*

Mappus S. (2005) *DV/DT Immunity improved in synchronous buck converters.* Retrieved January 10,2008, from http://powerelectronics.com

Microsemi (1998) *Hiccup Mode Current Limiting* Retrieved January 20, 2008, from www.microsemi.com/micnotes

Nagaraja H. N., & Kastha D., & Patra A. (2005) "Generalized analysis of integrated magnetic component based low voltage interleaved DC-DC buck converter for efficiency improvement Circuits and Systems" *IEEE International Symposium on Volume , 23-26 May 2005 Page(s): 2485 - 2489 Vol. 3*

Rashid M. H. (1993) *Power electronics, circuits devices, and applications* (2nd edition). New Jersey: Prentice-Hall International, Inc.

Torex (2004) *Fundamental DC/DC Converter* Retrieved April 1, 2008, from http://www.torex.co.jp

Turan B. (2007) M.Sc. Thesis: On the Design of Switch Mode Power Suplly Design

Wikipedia (n.d) *Energy Conversion Efficiency* Retrieved December 2, 2008 from http://en.wikipedia.org/wiki/Energy_conversion_efficiency

Wu T. (2004) *CDV/DT induced turn-on in synchronous buck regulators.* Retrieved November 10, 2007, from www.irf.com/technical-info

APPENDIX A

Schematics of Intel Montevina Platform Notebook Computer Double Data Rate (DDR) Voltage Rail