DOKUZ EYLÜL UNIVERSITY GRADUATE SCHOOL OF NATURAL AND APPLIED SCIENCES

DESIGN AND REALIZATION OF HIGH STABILITY DIELECTRIC RESONATOR OSCILLATOR

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DESIGN AND REALIZATION OF HIGH STABILITY DIELECTRIC RESONATOR RF OSCILLATOR

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M.Sc THESIS EXAMINATION RESULT FORM

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Şebnem SEÇKİN UĞURLU

DESIGN AND REALIZATION OF HIGH STABILITY DIELECTRIC RESONATOR RF OSCILLATOR

ABSTRACT

In this thesis, a 4.25 GHz negative resistance dielectric resonator oscillator simulation and realization are presented. Dielectric resonator oscillators are widely used in many applications of communications systems, military electronics, radars etc.

The dielectric resonator is simulated using 3D full-wave electromagnetic field software, HFSS High Frequency Structure Simulator. MGA-72543 amplifier chip is used to provide negative resistance. The simulation and realization results are discussed.

Keywords: Dielectric resonator, negative resistance, high frequency structure simulator

YÜKSEK KARARLILIKLI DİELEKTRİK RADYO FREKANS OSİLATÖRÜ TASARIM VE GERÇEKLENMESİ

ÖZ

Bu tezde 4.25 GHz negatif direnç, dielektrik rezonatör osilatör benzetim ve gerçeklenmesi sunulmaktadır. Dielektrik rezonatör osilatörler iletişim sistemleri, askeri elektronik ve radarlar gibi pek çok uygulamada geniş, kullanım alanı bulmaktadır.

Dielektrik rezonatör 3-B tam-dalga elektromanyetik alan yazılımı, HFSS - High Frequency Structure Simulator, kullanılarak benzetimi gerçekleştirilmiştir. MGA–72543 yükselteç negatif direnç, olarak kullanılmıştır. Benzetim ve gerçekleme sonuçları tartışılmıştır.

Anahtar Sözcükler: Dielektrik rezonatör, negatif direnç, yüksek frekans yapı benzetimcisi

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CHAPTER ONE INTRODUCTION

The dielectric resonator oscillators (DRO) are known as one of the most suitable devices for generating low-cost microwave signals. Its properties of having low phase noise, small size, high quality factor, temperature and frequency stability, which allow it to have progressively extending area of usage in many applications such as measuring the material properties (Krupka, Derzakowski, Riddle and Baker-Jarvis, 1998), oscillators (Abe, Takayama, Higashisaka and Takamizawa, 1978), antennas (Huang et. al, 2007), filters (Iveland, 1971) that requires low noise profile. Since the sizes of dielectric resonators are small they are mostly preferred in high frequency applications.

Dielectric resonators (DR) are produced in various shapes, for instance cylinder, tubular, spherical and ring. Cylindrical ones are very common because of their ability to fit in many in both integrated and monolithic microwave integrated circuits (MMIC). Depending on the geometrical structure of the resonator there are different mode solutions in the resonator (Kajfez and Guillon, 1986).

Different types of wave propagations may exist in transmission lines and microwave components. Transverse electromagnetic waves (TEM) have no longitudinal components (Harrington, 2001). Transverse electric (TE) waves have the longitudinal magnetic component and transverse magnetic (TM) waves have the longitudinal electric component.

The waveguides can support TE and TM modes. When solving the wave equations of TE and TM waves, infinitely many solution appear because of the periodicity of the solutions. These solutions are called modes and the modes are determined by the cutoff wave number k_{mn} , where m and n refers to the number of dimensional variations. Since the dielectric resonator (Figure 1.1) can be considered as a dielectric waveguide with length L and open at both ends the lowest order of TE mode is the TE₀₁ mode which is dual of the TM₀₁ mode of a circular waveguide (Pozar, 2005). But the longitudinal H field will drop outside of the resonator because of the high permittivity of the resonator. Thus the symbol δ is added to denote the longitudinal variation of H field and the most common mode of a dielectric resonator is denoted as TE_{01 δ}.



Figure 1.1 Typical dielectric resonator shapes

The resonant frequency of the resonator depends on relative permittivity, length and diameter of the resonator. Approximate formulas and more accurate numerical methods can be found in Kajfez and Guillon (1986).

One other important feature of the resonator is that it has high relative permittivity which can go up to 100 (Mongia, Ittibipoon and Cuhaci, 1994) (Leung, Lo, So and Luk, 2002). In the $TE_{01\delta}$ mode, most of the energy (both electric and magnetic) is stored within the cylinder. The rest of the energy radiates in the air. The stored energy enables the dielectric resonator to be employed in microwave circuits by coupling them to the microstrip lines. The distance between the microstrip line and the resonator determines the coupling coefficient, therefore how much of the energy is coupled to the microstrip line. The remaining radiating energy can be prevented mounting the resonator and the substrate in a shielding box of metal. However, mounting the resonator in a shielding box, changes the resonance frequency. This property of the resonator is useful for easy tuning resonator but is also unwanted since it complicates the design procedure.

The resonant frequency of the resonator depends on the geometry, material properties and the coupling schemes. Therefore it requires an analysis of the complete structure. Computer aided design tools using the finite element method are being used increasingly for computing resonance frequency. High frequency finite element method based simulation program HFSS is used for this purpose in this thesis.

The resonant frequency of a dielectric resonator also changes with temperature. Temperature - frequency stabilization of dielectric resonators can be done by means of devices such as diodes (Day, 1971), Gunn diodes (Makino, 1979) and transistors (Abe, Takayama, Higashisaka and Takamizawa, 1978).

In this thesis, the design of a negative-resistance DRO is studied. In the light of this research, a dielectric resonator oscillator operating at 4.25 GHz is designed, simulated and realized. The simulation and the measurement results are presented. The general content of the thesis report can be summarized as follow:

In Chapter 2, general theory of microwave resonators, resonators with the perspective of circuit theory, quality factor and bandwidth of resonator circuits, dielectric resonator materials, models of dielectric resonators and coupling of dielectric resonators are represented. In Chapter 3, surveying the general theory of oscillators, the concepts of oscillation mechanism, S-parameters and design procedures are examined. Then realized negative-resistance DRO design and its simulation results using HFSS and Advanced Design System are presented in Chapter 4. Finally in Chapter 5, the measurement results of the designed and realized DRO are given prior to the conclusions chapter.

CHAPTER TWO DIELECTRIC RESONATOR

2.1 Microwave Resonators

A resonator is a structure that has at least one natural frequency of oscillation which is called the resonant frequency. At this frequency the energy stored in the resonator oscillates which can also be interpreted as the conversion of the energy. In a microwave resonators the electromagnetic waves travel causing a standing wave pattern. The energy is converted from electrical to magnetic energy and vice versa. At the resonant frequency the energy stored in electric field and the energy stored in magnetic field are equal and the device has purely real impedance.

The important characteristics of the microwave resonators are the resonant frequency f_0 , the quality factor Q, which defines the bandwidth of the resonance and the input impedance of the resonator which restricts the impedance matching methods we can use (Das and Das, 2007).

The microwave resonators are used in several applications such as oscillators, filters, frequency meters, tuned amplifiers, measurement systems, tuners (Plourde and Ren, 1981). The choice of resonator depends on the utilization of the circuit. Some types of resonators can be summarized as lumped element resonators, varactor resonators, ceramic resonators, Yttrium iron garnet (YIG) resonators, coaxial resonators, transmission line resonators, cavity resonators, dielectric resonators (Pozar, 2005).

From the circuit theory point of view, microwave resonators can be modeled as series resonant circuit or parallel resonant circuit. The two circuit models are briefly summarized below.

2.1.1 Series Resonant Circuit

A series resonant circuit can be seen in Figure 2.1. The input impedance of the circuit looking into the load



Figure 2.1 A series resonant circuit



Figure 2. 2 The input impedance graphic for a series resonant circuit

and the complex power delivered to the resonator is

$$P_{in} = \frac{1}{2} V I^* = \frac{1}{2} Z_{in} \left| I \right|^2 = \frac{1}{2} Z_{in} \left| \frac{V}{Z_{in}} \right|^2$$

$$= \frac{1}{2} \left| I \right|^2 \left(R + j\omega L + \frac{1}{j\omega C} \right)$$
(2-2)

The power dissipated by the resistor R is,

$$P_{loss} = \frac{1}{2} \left| I \right|^2 R \tag{2-3}$$

The average magnetic energy stored in the inductor L is,

$$W_m = \frac{1}{4} |I|^2 L$$
 (2-4)

The average electric energy stored in the capacitor C is,

$$W_e = \frac{1}{4} |V_C|^2 C = \frac{1}{4} |I|^2 \frac{1}{\omega^2 C}$$
(2-5)

where V_C is the voltage across the capacitor C. The complex power can be recalculated as

$$P_{in} = P_{loss} + 2j\omega (W_m - W_e)$$
(2-6)

which is also known as Poynting's Theorem (Pozar, 2005).

Using (2-6) in (2-2) we can redefine the input impedance Z_{in} as

$$Z_{in} = \frac{2P_{in}}{|I|^2} = \frac{P_{loss} + 2j\omega(W_m - W_e)}{\frac{1}{2}|I|^2}$$
(2-7)

When the average magnetic and electric energies are equal $(W_m=W_e)$ the resonance occurs. From (2-3) and (2-7) the input impedance at the resonance is

$$Z_{in} = R \tag{2-8}$$

It can be seen from (2-8) that input impedance at the resonance is purely real. Also, from (2-4) and (2-5) the resonant frequency ω_0 can be evaluated as

$$\frac{1}{4}|I|^{2}L = \frac{1}{4}|I|^{2}\frac{1}{\omega_{0}^{2}C}$$

$$\omega_{0} = \frac{1}{\sqrt{LC}}$$
(2-9)

2.1.2 Parallel Resonant Circuit



Figure 2.3 Parallel resonant circuit

Parallel RLC resonant circuit can be approached similar to series RLC circuit. The input impedance is

$$Z_{in} = \left(\frac{1}{R} + \frac{1}{j\omega L} + j\omega C\right)^{-1}$$
(2-10)

and the complex power delivered to the resonator is

$$P_{in} = \frac{1}{2} V I^* = \frac{1}{2} Z_{in} \left| I \right|^2 = \frac{1}{2} Z_{in} \left| \frac{V}{Z_{in}} \right|^2$$

$$= \frac{1}{2} \left| V \right|^2 \left(\frac{1}{R} + \frac{j}{\omega L} - j \omega C \right)$$
(2-11)



Figure 2. 4 The input impedance graphic for a parallel resonant circuit

The power dissipated by the resistor R is

$$P_{loss} = \frac{1}{2} \frac{|V|^2}{R}$$
(2-12)

The average magnetic energy stored in the inductor L is,

$$W_m = \frac{1}{4} |I_L|^2 L = \frac{1}{4} |V|^2 \frac{1}{\omega^2 L}$$
(2-13)

where I_L is the current through inductor L. The average electric energy stored in the capacitor C is,

$$W_{e} = \frac{1}{4} \left| V_{C} \right|^{2} C \tag{2-14}$$

The complex power can be evaluated from (2-6) and the input impedance is found as

$$Z_{in} = \frac{2P_{in}}{|I|^2} = \frac{P_{loss} + 2j\omega(W_m - W_e)}{\frac{1}{2}|I|^2}$$
(2-15)

similar to (2-7).

As in series resonance circuit, the resonance occurs when $W_m=W_e$. From (2-12) and (2-15) the input impedance at resonance can be calculated as

$$Z_{in} = R \tag{2-16}$$

The resonant frequency ω_0 can be evaluated as

$$\omega_0 = \frac{1}{\sqrt{LC}} \tag{2-17}$$

2.1.3 Quality factor

An important criterion of performance or quality of a resonator is the quality factor, Q (Kajfez and Guillon, 1986). Quality factor is defined as the ratio of average energy stored and energy loss per cycle.

$$Q = \omega \frac{W_m + W_e}{P_{loss}}$$
(2-18)

For series resonant circuit, at resonance the quality factor can be evaluated as

$$Q = \omega_0 \frac{2W_m}{P_{loss}} = \frac{\omega_0 L}{R} = \frac{1}{\omega_0 RC}$$
(2-19)

and for parallel resonant circuit as

$$Q = \omega_0 \frac{2W_m}{P_{loss}} = \frac{R}{\omega_0 L} = \omega_0 RC$$
(2-20)

which is the reciprocal of (2-19).

The quality factor is defined as a figure of merit for the performance of a resonator. Lower loss implies higher Q. From (2-19) it can be seen for a series resonant circuit increase of Q requires decrease of R. For a parallel resonant case the situation is reverse: Q increases as R increases.

Another approach for estimating quality factor is examining the circuit using differential equation for a simple parallel resonator circuit (Kajfez and Guillon, 1986)

$$i(t) = \frac{d^2 v(t)}{dt^2} + 2\sigma \frac{dv(t)}{dt} + \omega_0^2 t v(t)$$
(2-21)

where σ is the conductivity of the resonator and V(t) is the voltage across the resonator terminals and i(t) is the function of current.

When $\sigma=0$, the resonator is a lossless one. $\sigma>0$ means a resonator with loss. Using Laplace transformation on

$$H(s) = V(s)/I(s) = \frac{1}{s^2 + 2\sigma s + \omega_0^2}$$

$$= \frac{j}{2\omega_L} \left\{ \frac{1}{s + \sigma + j\omega_L} - \frac{1}{s + \sigma - j\omega_L} \right\}$$
(2-22)

where $\omega_L = \sqrt{\omega_0 - \sigma^2}$ is the natural frequency. It can be understood from (2-22) that when $\sigma \neq 0$, the resonant frequency changes. This is called frequency pulling due to loss regarding the loss inside the resonator tank circuit (Kajfez and Guillon, 1986).

The natural response of the differential equation is

$$v(t) = V_0 e^{-\sigma t} \sin \omega_L t \tag{2-23}$$

where V_0 is determined by the initial conditions. The stored energy W is proportional to the average value of $v^2(t)$. Let σ be very small, then

$$W = \frac{1}{2} V_0^2 e^{-2\sigma t}$$
(2-24)

The average power P is

$$P = -\frac{dW}{dt} = 2\sigma W \tag{2-25}$$

Since Q is defined as in (2-18)

$$Q = \omega \frac{W_m + W_e}{P_{loss}} = \frac{\omega_0}{2\sigma}$$
(2-26)

The loss tangent for a dielectric material can be defined as

$$\tan \delta = \frac{\sigma}{\left(\omega \varepsilon_0 \varepsilon_r\right)} \tag{2-27}$$

where ε_0 is the permittivity of vacuum and ε_r is the relative permittivity. Then the dielectric quality factor Q_d , for homogeneous dielectric material (ε is not function of position) can be found as the reciprocal of the loss tangent.

$$Q_{d} = \frac{\omega_{0}W}{P_{d}} = \frac{\omega_{0}\varepsilon \int |E|^{2}dV}{\sigma \int |E|^{2}dV} = \frac{\omega_{0}\varepsilon}{\sigma} = \frac{1}{\tan\delta}$$
(2-28)

2.1.3.1 Loaded and Unloaded Q Factor

We can define different quality factors in a resonant structure. The unloaded Q (Q_u) is defined considering the parameters of the resonant circuit only. However, considering the usage of the resonant circuit, it is known that the resonator is usually loaded with another

circuit which cause a power loss to overall system. If the quality factor due to external load is defined as Q_e , total loaded Q_L of the system is

$$\frac{1}{Q_L} = \frac{1}{Q_e} + \frac{1}{Q_u}$$
(2-29)

2.1.4 Bandwidth

The bandwidth is considered as the half-power fractional bandwidth of the resonator (Collin, 1992). If we consider the behavior of the input impedance of a series resonant circuit near its resonant frequency, we define

$$\omega = \omega_0 + \Delta \omega \tag{2-30}$$

where $\Delta \omega$ is very small. Using (2-1), (2-9) can be rewritten as

$$Z_{in} = R + j\omega L \left(1 - \frac{1}{\omega^2 LC} \right)$$
$$= R + j\omega L \left(\frac{\omega^2 - \omega_0^2}{\omega^2} \right)$$

(2-31)

Let
$$\omega^2 - \omega_0^2 = (\omega - \omega_0)(\omega + \omega_0) = \Delta \omega (2\omega - \Delta \omega) \simeq 2\omega \Delta \omega$$
 for small $\Delta \omega$. (2-31) becomes

$$Z_{in} \simeq R + j2L\Delta\omega \tag{2-32}$$

Substituting (2-19) in (2-32)

$$Z_{in} \simeq R + j \frac{2RW\Delta\omega}{\omega_0}$$
(2-33)

At the frequency which $|Z_{in}|^2 = 2R^2$, the real power delivered to the circuit is one-half or -3 dB below its maximum value that delivered at resonance (Figure 2.5). Since, the bandwidth (BW) is defined is fractional bandwidth

$$\frac{BW}{2} = \frac{\Delta\omega}{\omega_0} \tag{2-34}$$

Substituting (2-26) in (2-33)

$$\left|R + jRQ(BW)\right|^{2} = 2R^{2}$$

$$BW = \frac{1}{Q}$$
(2-35)



Figure 2.5 Bandwidth of a resonator

For both series and parallel resonant circuits (2-10) can be rewritten using (2-31) as (Collin, 1992)

$$Z_{in} \approx \left(\frac{1}{R} + \frac{1 - \Delta \omega}{j\omega_0 L} + j\omega_0 C + j\Delta \omega C\right)^{-1}$$

$$\approx \left(\frac{1}{R} + j\frac{\Delta \omega}{\omega_0^2 L} + j\Delta \omega C\right)^{-1}$$

$$\approx \left(\frac{1}{R} + 2j\Delta \omega C\right)^{-1}$$

$$\approx \frac{R}{1 + 2j\Delta \omega RC} = \frac{R}{1 + 2jW\Delta \omega / \omega_0}$$
(2-36)

The half-power bandwidth occurs when $|Z_{in}|^2 = 2R^2$. Using this in (2-36)

$$BW = \frac{1}{Q} \tag{2-37}$$

which is identical to the series resonant case.

2.2 Dielectric Resonators

2.2.1. Dielectric Materials

Dielectric materials have a very low conductivity. Unlike conductors, electrons in dielectric materials cannot move in the presence of an electric field. Instead, positive charges gather on one side and negative charges gather on the other side of the material which is called polarization.

The dielectric constant (ε_r) is fixed and dielectric loss increases with frequency (f) at microwave frequencies. So $Q_u \times f$ is an important parameter for dielectric materials (Fiedziuszko et al., 2002). Table 2.1 shows different materials and their properties where ε_r is the dielectric constant, Q is the unloaded quality factor, τ_f is the temperature coefficient which is a parameter of the relation between the temperature of medium and the resonance frequency (part per million - ppm) and f_0 is the resonant frequency.

Materials	٤ _r	Q	Q×f (GHz)	$\tau_{\rm f}(\rm ppm/^0C)$	f ₀ (GHz)
MgTiO ₃ -CaTiO ₃	21	8000	55000	+10~-10	7
Ba(Sn,Mg,Ta)O ₃	25	20000	200000	+5~-5	10
Ba(Zn,Ta)O ₃	30	14000	168000	+5~-5	12
Ba(Zr,Zn,Ta)O ₃	30	10000	100000	+5~-5	10
(Ca,Sr,Ba)ZrO ₃	30	4000	44000	5	11
(Zr,Sn)Ti O ₄	38	7000	50000	+5~-5	7
Ba ₂ Ti ₉ O ₂₀	40	8000	32000	+10~-2	3
BaO-PbO-Nd ₂ O ₃ -TiO ₂	90	5000	5000	+10~-10	1

Table 2.1 Dielectric materials for microwave applications (Wakino, 1985)

2.2.2 Dielectric Resonators

It was first presented by R.D. Richtmyer (1939) that "a long dielectric cylinder that bent into a ring and the ends joined together, would guide the waves round and round indefinitely, so that they would be confined to a finite region of space and such an object would act as an electric resonator". But it took a few decades to realize such circuits that contained dielectric resonators.

Dielectric Resonators (DR) combine many advantages. They are small, low-cost, lowloss, temperature stable and have large quality factor (Plourde and Ren, 1981). Their small size makes them substantially available to use in integrated circuits.



Figure 2.6 Dielectric resonators with different sizes.

The electromagnetic fields in a dielectric resonator can be analyzed with various methods. The analysis of dielectric resonators involves finding resonant frequency, field distribution, stored energy and magnetic-dipole moment (Cohn, 1986). The modes for which the axial dimensions of the cavity do not contribute (degenerate modes) were searched by Schlicke (1953). Hybrid modes on dielectric cylinders were investigated by Schlesinger, Diament and Vigants (1960). The frequency equations of modes in anisotropic medias for rectangular parallelepiped were derived by Okaya and Barash (1962).

2.2.2.1 Dielectric Resonator Model

The simplest model of the DR is called "first-order" model (Okaya and Barash, 1965). Figure 2.7 illustrates this model. L is the thickness and a is the radius of the dielectric resonator.



Figure 2.7 First-order model of DR. (Kajfez and Guillon, 1986)

The first-order model of DR shows a great deal of similarity to circular cavity resonator which has perfect magnetic conductor (PMC) walls. Using calculations for hollow resonators, the resonant frequency of the resonator can be evaluated. But since computed results differ up to 20% first-order model is not preferred.

Improvement for the first-order method is done by Cohn (1968) which is called "second-order model". This mode assumes that the dielectric cylinder is contained in a continuous magnetic-wall waveguide similar to first-order model. This is done by removing PCM end caps and changed with hollow waveguides filled with air. The hollow waveguides operate below cut off since they are filled with material having a low dielectric constant. Hence, the modes in waveguides are evanescent and they decay exponentially in the z direction away from each end of the resonator (Figure 2.6). The electric and magnetic fields inside the resonator for TE_{01δ} mode are shown in Figure 2.8.



Figure 2.8 Cylindrical resonator where L<D



Figure 2.9 Distribution of modes in waveguides (Pozar, 2005)

Dielectric resonators can work in the Transverse Electric (TE), Transverse Magnetic (TM) and Hybrid modes (Mazierska and Liu, 2003). The lowest order electric mode and the most widely used mode of circular DR is $TE_{01\delta}$. In this notation 0 and 1 denote the waveguide mode and δ is $2L/\lambda_g < 1$ where λ_g is the guide wavelength of the TE_{01} dielectric waveguide mode. The resonant frequency for a cylindrical dielectric resonator was investigated by Yee (1965). For different dielectric resonator configurations were derived by Pospieszalski (1968). According to Pospieszalski (1968) the resonant frequency, $f_0=c/\lambda_0$, of a cylindrical dielectric resonator can be obtained by solving (2-38) for λ_0 .

$$\beta_d \tan \frac{\beta_d L}{2} = \alpha_a \tag{2-38}$$

where

$$\beta_{d} = 2\pi \sqrt{\frac{\varepsilon_{r}}{\lambda_{0}^{2}} - \frac{0.586}{D^{2}}}$$

$$\alpha_{a} = 2\pi \sqrt{\frac{0.586}{D^{2}} - \frac{1}{\lambda_{0}^{2}}}$$
(2-39)

However, this approximation has drawbacks too because it ignores the fringing fields at the sides of the resonator and results may differ up to 10%. More accurate, rigorous solutions became available in the literature throughout the years (Kajfez and Guillon, 1986). Studies of Itoh and Rudokas (1977), Pospieszalski (1979), Krupka et al. (1998, 2001), Sheen (2007) improved theoretical analysis of the dielectric resonators.

One of the important assumptions of rigorous techniques is that the resonator is in a parallel –plate waveguide or in a cylindrical cavity (Harrington, 1968). These resonators are shielded with perfect electric conductors (PEC). (Figure 2.7)



Figure 2. 10 Dielectric resonator inside a PEC cavity

The rigorous analysis starts with Maxwell Equations with no sources.

$$\nabla \times H = j\omega\varepsilon_{0}\varepsilon_{r}E$$

$$\nabla \times \overline{E} = j\omega\mu_{0}\overline{H}$$

$$\nabla \cdot \overline{H} = 0$$

$$\nabla \cdot \left(\varepsilon_{r}\overline{E}\right) = 0$$
(2-40)

The assumptions here are permeability of the region is μ_0 , permittivity is $\varepsilon = \varepsilon_r \varepsilon_0$ and permittivity can vary with position. Substrate's permittivity is $\varepsilon_r = \varepsilon_{rs}$ and resonator's permittivity is $\varepsilon_r = \varepsilon_{rd}$ and $\varepsilon_r = 1$ in the remaining region bounded by metallic walls which are assumed as PEC.

This type of analysis brings out the fact that solution to this problem is solving an inhomogeneously filled cavity problem. Through years, many approximations have been done to this problem. In radial mode matching method the resonator cross section is divided into parts where ε_r is a piece-wise function of z. The fields are represented as a superposition of fields which individually satisfy the boundary conditions at PEC (Kobayashi, Fukuoka and Yoshida, 1981, Crombach, 1981).

In axial mode matching method, the resonator is divided into regions where ε_r is independent of the axial coordinate (Hong and Jansen, 1982).

Another method of rigorous analysis is differential method (Maystre, Vincent and Mage, 1983). The restriction of this method is that DR must be a structure of revolution with respect to z-axis. However, the permittivity of the dielectric ε_{rd} can be a function of both ρ and z. This method divides the cavity into two regions by an artificial cylindrical surface of radius R. This surface bounds the dielectric and extends from the bottom to the top plate of the shield.

Apart from mode matching methods, finite-element and finite-difference methods are also applied to solve dielectric resonator problem (Gil and Gismero, 1984, Gil and Perez, 1985). Gil et al. used first and higher-order rectangular elements. Using Integral equations is another method. The method is based on the solution of an integral equation, not a differential equation. Proper Green's function must be found in order to apply this method properly (Omar, Schunemann, 1984, 1986).

The increase in the usage of computer aided design programs (CAD), have brought dielectric resonator to a different stage. Mizan, Higgins and Sturzebecher (1993) introduced the usage of 3D EM simulator to analyze the S-parameters of dielectric resonator. Later Mazierska and Liu (2003) presented an investigation determining Q factors and the resonant frequency of a Hakki-Coleman resonator using 3-D EM simulator.

2.2.2.2 Coupling of Dielectric Resonators

If a dielectric resonator is placed nearby of microstrip line on a substrate, magnetic coupling between the resonator and microstrip line occurs. In order to analyze this coupling, lumped circuit models of a resonator coupled to a microstrip line have been developed. Guillon and Garault (1976) suggested the model in Figure 2.9 which has a layout shown in Figure 2.8.



Figure 2.8 Layout of the DR coupled to two microstrip lines



Figure 2.9 Circuit model proposed by Guillon and Garault (1976)

In this model C_L and L_L are equivalent self inductance and capacitance of the microstrip line and C'_r and L'_r are equivalent self inductance and capacitance of the resonator. The coupling between the line and the resonator is defined as L_m . The relation between unloaded and external quality is given as

$$Q_{\mu} = \alpha Q_{\rho} \tag{2-41}$$

where α is the voltage standing wave ratio (VSWR) for undercoupling.

Abe, Takayama, Higashisaka and Takamizawa (1978) suggested an equivalent circuit of a dielectric resonator shown in Figure 2.10



Figure 2.10 Equivalent circuit of dielectric resonant circuit

According to Abe et al. (1978) coupling constant k increases if L which is the distance between the resonator edge and the microstrip line decreases. It is also stated that in order to model the resonator, the distance X_L must be equal to $\lambda_g/2$ where λ_g is the microstrip wavelength. The input impedance can be written as

$$Z = Z_0 \left(1 + \frac{k}{1 + jQ_u \left(\Delta \omega / \Delta \omega_0 \right)} \right)$$
(2-42)

where Q_u is the unloaded quality factor and Z_0 is the characteristic impedance of the microstrip line to which resonator is coupled.

Podcameni, Conrado and Mosso (1981) stated that it is undesirable for a straightforward estimation of unloaded quality factor when k interferences the equation since it both changes the input impedance and the unloaded quality factor simultaneously. The input impedance of the circuit in Figure 2.10 can be rewritten as

$$Z = Z_0 \left(1 + \frac{1}{(1/R) + j\omega C + 1/j\omega L} \right)$$
(2-43)

where R, L and C are normalized quantities. At the resonance frequency ω_0 it is clear that $Z = Z_0(R+1)$.

Komatsu and Murakami (1983) suggested that the dielectric resonator coupled to a microstrip line can be described as a parallel resonance circuit which is magnetically coupled with a microstrip line (Figure 2.11).



Figure 2.11 Parallel resonant equivalent circuit of a dielectric resonator (Komatsu and Murakami, 1983)

Khanna and Garault (1983) present the relations between coupling coefficient (k), reflection and transmission coefficients (S_{11} and S_{21}) of the dielectric resonator. Relations of dissipated power and S parameters as well as unloaded quality factor and the coupling coefficient are also introduced (Khanna and Garault, 1983).

According to Khanna and Garault, the coupling coefficient (k), at the resonance frequency can be formulated as the ratio of the resonator coupled to resistance R to the external resistance

$$k = \frac{R}{R_{ext}} = \frac{R}{2Z_0} = \frac{S_{11_0}}{1 - S_{11_0}} \frac{1 - S_{21_0}}{S_{21_0}} = \frac{S_{11_0}}{S_{21_0}}$$
(2-44)

where S_{11_0} and S_{21_0} are the reflection and transmission coefficients respectively at the resonant frequency.



Figure 2. 11 Magnitudes of $S_{11} \mbox{ and } S_{21}$ near resonant frequency respectively

The coupling coefficient depends on the distance between the resonator and the microstrip line. Also k is related with the quality factors as

$$Q_{u} = Q_{L}(1+k) = kQ_{ex}$$
(2-45)

CHAPTER THREE OSCILLATORS

3.1 Introduction

A microwave oscillator is a device that converts DC power to an AC (RF) waveform. (Pozar, 2005). This property of an oscillator makes it useful for generating signals. Various waveforms can be generated by oscillator such as sinusoidal, square and saw-tooth waveforms.

Oscillator can be simply considered as amplifiers with positive feedback that satisfies the oscillation criterion also called as Barkhausen Criterion. This criterion leads to the fact that oscillation means, in theory, an output voltage (or current) without input voltage (or current).

The simplest forms of oscillators are lumped element RC, LC oscillators which consist of resistors, inductors and capacitors. The first oscillators were vacuum tube oscillators based on the idea of electromagnetic coupling between the input and output of the circuit (Grebennikov, 2007). Armstrong (Armstrong, 1915), Meissner, Hartley (Hartley, 1920) and Colpitts (Colpitss, 1927) oscillators are examples of this type oscillators.

Since the frequency in applications of electronics tends to increase, microwave oscillators have gained importance. Therefore the lumped elements gain different characteristics in higher frequencies, usage of lumped elements are not preferable in microwave frequencies. Distributed elements are used instead of lumped elements. Also the rapid development in semiconductor technology led the design of more stable and low-noise microwave oscillators. Some of the basic oscillator configurations were adapted using transistors.

In this chapter, basic concepts of oscillation mechanism will be explained. Since the Sparameters are the most used characteristic of microwave circuits, fundamental knowledge about S-parameter of N-port devices will be given. Since our dielectric resonator oscillator consists of negative resistance, negative resistance oscillator design will be analyzed and design method for two-port oscillator will be investigated.

3.1.1 Oscillation Mechanism and Positive Feedback Oscillator

The basic principle of an oscillator is forming a closed loop circuit creating a positive feedback as shown in Figure 3.1.



Figure 3.1 Block diagram of an oscillator

 $V_i(j\omega)$ is the input voltage function, $V_o(j\omega)$ is the output voltage function, $A(j\omega)$ is the amplifier gain function and $H(j\omega)$ is the feedback transfer function. The mathematical expression of the oscillator can be derived as:

$$\frac{V_o}{V_i} = \frac{A(j\omega)}{1 - A(j\omega)H(j\omega)}$$
(3-1)

It can be understood from the Equation (3-1) that an active device is needed to supply the gain $A(j\omega)$. Amplifiers are used for this purpose in the oscillator circuits.

The feedback transfer function is defined as:

$$H(j\omega) = K(j\omega)Z(j\omega)$$
(3-2)

where $K=V_{in}/V_{out}$ called voltage feedback coefficient and $Z=V_{out}/I_{out}$ called as the oscillator resonant circuit impedance.

The oscillator is a 1-port device which means it has no input but only output port. This indicates that V_i is zero. This requirement leads to the loop gain equation, which is also known as **Barkhausen criterion**.

$$A(j\omega)H(j\omega) = 1 \text{ or}$$

$$A(j\omega)K(j\omega)Z(j\omega) = 1$$

$$\phi_A + \phi_H = 2k\pi \text{ or}$$

$$\phi_A + \phi_K + \phi_Z = 2k\pi$$

$$k = 0, 1, 2...$$

$$(3-3)$$

Equation (3-3) and (3-4) indicates that oscillation occurs when the magnitude of $A(\omega)H(\omega)$ is equal to 1 and its phase is equal to 0° or 360°. Equation (3-3) is also called *amplitude balance condition* (Grebennikov, 2007). This mode of operation is called the *steady-state operation mode* of an oscillator.



Figure 3.2 Graphic of balance amplitude condition (Grebennikov, 2007)

Figure 3.2 shows the amplitude balance condition. The amplitude dependence and feedback straight line intersection point determines the steady-state oscillation amplitude V_{in}^{0} .

Equation (3-4) is called *phase balance condition* (Grebennikov, 2007). It can be understood that the sum of all phase shifts must be equal to zero or multiples of 2π . One can determine the oscillation frequency using this equation.

3.1.2 S-Parameters

The difficulty of defining voltages and currents for non transverse electromagnetic lines and the fact that practical measurements of microwave devices consist of measuring magnitude and phase of power (not directly voltage or currents) raise the need for a better representation of microwave circuits. This representation which is based on incident, transmitted and reflected waves is defined as the scattering matrix.

Scattering matrix (S-parameters) can be defined for N-port devices as

$$\begin{bmatrix} V_{1}^{-} \\ V_{2}^{-} \\ \vdots \\ V_{N}^{-} \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} & \cdots & S_{1N} \\ S_{21} & & \vdots \\ \vdots & & & \\ S_{N1} & \cdots & S_{NN} \end{bmatrix} \begin{bmatrix} V_{1}^{+} \\ V_{2}^{+} \\ \vdots \\ V_{N}^{+} \end{bmatrix}$$
(3-5)

where

$$S_{ij} = \frac{V_i^-}{V_j^+} \bigg|_{V_k^+ = 0 \text{ for } k \neq j}$$
(3-6)

Equation (3-6) can be interpreted as that S_{ij} is calculated by driving the *j*th port with an incident voltage V_j^+ and measuring the reflected voltage V_j^- from the *i*th port. The important point is that all the other ports except the *j*th port must be terminated in matched loads since all the incident waves on all ports except *j*th port is set to zero. One can observe that, if all other ports are terminated with matched loads, S_{ii} is the reflection coefficient of the *i*th port.
3.1.3 Negative Resistance Oscillator

The series resonant circuit was investigated in Chapter 2. The voltage source in this circuit can be considered as the output of the active device. We can define the current as:

$$L\frac{d^{2}i(t)}{dt^{2}} + R\frac{di(t)}{dt} + \frac{1}{C}i(t) = -\frac{dv(i)}{dt}$$
(3-7)

Considering the steady-state conditions, the derivate on the right hand side of must be equal to zero. Solution to (3-7) can be written as:

$$i(t) = e^{\alpha t} \left(I_1 e^{-j\omega_0 t} + I_2 e^{j\omega_0 t} \right)$$
(3-8)

where $\alpha = -R/2L$ and $\omega_Q = \sqrt{1/(LC) - (R/(2L))^2}$. Since α is a negative quantity, the response of the oscillator circuit will dampen to zero in time. In order to have a successful oscillator circuit the response must be underdamped. This condition can only be achieved with a negative resistance.

Moreover, to get the oscillations started, we require a positive attenuation coefficient, which implies R_1 to be less than -R. (Ludwig and Bretchko, 2000)

Assuredly, the negative resistance does not exist as a circuit element. One can develop a negative resistance by using tunnel diodes, transistors and amplifiers with positive feedback.

3.2 Oscillator Design (S-Parameter Method)

3.2.1 S-parameters of two port network

A common method for designing oscillators is to resonate the input port with a passive high-Q circuit at the desired frequency of resonance. It can be shown that if this is achieved with a load connected on the output port, both ports oscillate and the power is delivered to the load (Vendelin, Pavio and Rohde, 2005). The oscillator can be defined as a two port network as shown in Figure 3.3



Figure 3.3 Oscillator diagram

S-parameters describe the network behavior in terms of incident and reflected voltages at each port. For a two-port network as in Figure 3.4, a and b waves are incident and reflected power waves respectively. The input and output reflection coefficients can be given as



Figure 3.4 Two-port network representation

$$\Gamma_{in} = \Gamma_1 e^{-2\gamma l_1} = \frac{b_1}{a_1}$$
(3-9)

$$\Gamma_1 = \frac{Z_1 - Z_{01}}{Z_1 + Z_{01}} \tag{3-10}$$

$$\Gamma_{out} = \Gamma_2 e^{-2\gamma l_1} = \frac{b_2}{a_2}$$
(3-11)

$$\Gamma_2 = \frac{Z_2 - Z_{02}}{Z_2 + Z_{02}} \tag{3-12}$$

$$\Gamma_L = \frac{a_2}{b_2} \tag{3-13}$$

$$\Gamma_G = \frac{a_1}{b_1} \tag{3-14}$$

where $\gamma = \alpha + j\beta$, designated as propagation constant, α is the attenuation constant and β is the phase constant. The scattering parameters can be defined as

$$b_1 = S_{11}a_1 + S_{12}a_2 \tag{3-15}$$

$$b_2 = S_{21}a_1 + S_{22}a_2 \tag{3-16}$$

Using (3-15) and (3-16) in (3-9) and in (3-11) one can obtain the reflection coefficient looking into input of the two-port device and looking into the output of the two-port device as

$$\Gamma_{1} = \frac{b_{1}}{a_{1}} = S_{11} + \frac{S_{12}S_{21}\Gamma_{L}}{1 - S_{22}\Gamma_{L}} = S_{11}^{'}$$
(3-17)

and

$$\Gamma_2 = \frac{b_2}{a_2} = S_{22} + \frac{S_{12}S_{21}\Gamma_G}{1 - S_{11}\Gamma_G} = S_{22}^{'}$$
(3-18)

3.2.2 Design Steps

To design a dielectric resonator one must resonate the both input and output ports of the chosen active device. We can use the dielectric resonator as a passive high-Q circuit that resonates in the desired oscillation frequency. We try to maximize the reflection coefficients of input and output ports of the active device in order to achieve the oscillation at both ports. Enabling reflection coefficients to be greater than unity leads to a potential unstable system. Thus the design of a two-port oscillator starts with the concept of

stability. By defining the unstable areas of the network, one can derive the conditions for oscillation.

3.2.2.1 Stability

The question of stability can be considered from three points of view (Vendelin, 1982).

- 1. In the Γ_L plane, what values of Γ_L give $\left|S_{11}\right| > 1$
- 2. In the S_{11}^{\dagger} plane, where the $|\Gamma_L| = 1$ circle is
- 3. If $(S_{11})^* = \Gamma_G$ and $(S_{22})^* = \Gamma_L$, the resistors terminating the network are positive.

The conditions for two-port stability, when load terminations has a positive real part, are

$$|S_{11}| < 1$$
 (3-19)

$$S_{22} < 1$$
 (3-20)

If any of (3-19) and (3-20) is not satisfied, the network is characterized as conditionally stable.

It can be noted here that if negative resistance is needed, $|S_{11}| > 1$ and $|S_{22}| > 1$ conditions must be satisfied. The methods for satisfying the above conditions will be examined in further chapters.

Using (3-17) and (3-18) it can be shown that S_{11} and S_{22} is equal to

$$S_{11} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} = \frac{S_{11} - D\Gamma_L}{1 - S_{22}\Gamma_L}$$
(3-21)

$$S_{22}^{'} = S_{22} + \frac{S_{12}S_{21}\Gamma_G}{1 - S_{11}\Gamma_G} = \frac{S_{22} - D\Gamma_G}{1 - S_{11}\Gamma_G}$$
(3-22)

where

$$D = S_{11}S_{22} - S_{12}S_{21} \tag{3-23}$$

For unconditional stability it must be ensured that S_{11} and S_{22} are less then unity for all Γ_L and Γ_G values. Since all the values mentioned above are complex variables they consist of real and imaginary parts.

$$S_{11} = S_{11r} + S_{11i} \tag{3-24}$$

$$S_{22} = S_{22r} + S_{22i} \tag{3-25}$$

$$D = D_r + D_i \tag{3-26}$$

$$\Gamma_L = \Gamma_{Lr} + \Gamma_{Li} \tag{3-27}$$

where S_{11r} , S_{22r} , D_r , Γ_{Lr} are the real and S_{11i} , S_{22i} , D_i , Γ_{Li} are the imaginary parts of the variables.

We can obtain the boundary of stability using (3-19) and (3-20).

$$\left|S_{11} - D\Gamma_{L}\right| < \left|1 - S_{22}\Gamma_{L}\right| \tag{3-28}$$

Substituting (3-24) - (3-27) and squaring both sides, we derive the circle

$$\left(\Gamma_{Lr} - \Gamma_{LrG}\right)^2 + \left(\Gamma_{Li} - \Gamma_{LiG}\right)^2 = r_G^2 \tag{3-29}$$

The center of the circle is

$$C_{G} = \Gamma_{LrG} + j\Gamma_{LiG}$$

$$= \frac{\left(S_{22} - DS_{11}^{*}\right)^{*}}{\left|S_{22}\right|^{2} - \left|D\right|^{2}}$$
(3-30)

And the radius of the circle is

$$r_{G} = \frac{\left|S_{12}S_{21}\right|}{\left|\left|S_{22}\right|^{2} - \left|D\right|^{2}\right|}$$
(3-31)

Inside the circle defined by Equations (3-30) and (3-31) the circle is unstable. For unconditionally stable circuit the following condition must be satisfied:

$$\left|C_{G}\right| - r_{G} > 1 \tag{3-32}$$

leading to

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |D|^2}{2|S_{12}||S_{21}|}$$
(3-33)

K is defined as the stability factor. Stability factor greater than unity means an unconditionally stable circuit. More detailed derivation of (3-33) can be found in Vendelin (1982).

We can sum up the necessary and sufficient conditions for stability as

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |D|^2}{2|S_{12}||S_{21}|} > 1$$
(3-34)

$$\left|S_{12}S_{21}\right| < 1 - \left|S_{11}\right|^2 \tag{3-35}$$

$$\left|S_{12}S_{21}\right| < 1 - \left|S_{22}\right|^2 \tag{3-36}$$

3.2.2.2 Oscillation Conditions

Oscillation conditions can be expressed as

$$k < 1$$
 (3-37)

$$\Gamma_G S'_{11} = 1$$
 (3-38)

$$\Gamma_L S_{22} = 1$$
 (3-39)

The important step of designing an oscillator is to make sure the stability factor, K, is less than unity. This can be achieved by changing the active device's (possibly a transistor) biasing configuration or adding a positive feedback.

It can be shown that if (3-38) is satisfied, (3-39) is also satisfied. This leads us to the fact that if input port is oscillating, output port is oscillating too (Vendelin, Pavio and Rohde, 2005). Assuming that the input port is oscillating, meaning

$$\frac{1}{S_{11}} = \Gamma_G \tag{3-40}$$

Using (3-21)

$$\frac{1}{S_{11}^{'}} = \frac{1 - S_{22}\Gamma_L}{S_{11} - D\Gamma_L} = \Gamma_G$$

$$\Gamma_G S_{11} - D\Gamma_L \Gamma_G = 1 - S_{22}\Gamma_L$$

$$\Gamma_L = \frac{1 - S_{11}\Gamma_G}{S_{22} - D\Gamma_G}$$
(3-41)

Using (3-22)

$$\frac{1}{S_{22}'} = \frac{1 - S_{11}\Gamma_G}{S_{22} - D\Gamma_G}$$
(3-42)

It is clearly shown that (3-41) is equal to (3-42) so

$$\frac{1}{S_{22}} = \Gamma_L \tag{3-43}$$

The two port oscillator design can be summarized as follows (Vendelin, 1982)

- 1. Select an active device (transistor, amplifier) with sufficient gain and output power capability for the frequency of operation.
- 2. Select a topology for *K* to be less than unity. One can add feedback to achieve this condition.

- 3. Select an output load matching circuit that gives the magnitude of S'_{11} greater than unity over the desired frequency range.
- 4. Resonate the input port with a lossless termination so that $\Gamma_G S_{11} = 1$

3. 3 Noise in Oscillators

In theory, output of an oscillator is considered as a pure sinusoidal signal. In practice there can be no such pure sinusoidal but the output of the oscillator can be approached as

$$v(t) = \left[1 + n(t)\right] \cos\left[\omega_0(t) + \phi(t)\right]$$
(3-44)

where n(t) is the noise in amplitude and $\varphi(t)$ is the noise in phase. With a good design approach, noise in amplitude becomes less significant than the noise in phase (Rhea, 1997).

The impact of the phase noise can be clearly seen from (3-44). However, noise is necessary for oscillations to start and compensate the output fluctuations. But there are limitations for the amplitude of the noise especially if the oscillators are used in digital systems.

Noise originates from the random motions of charges or charge carriers in device and materials (Pozar, 2005). These motions can lead up to different noise types which can be summarized as thermal noise, shot noise, flicker noise (1/f noise), plasma noise and quantum noise.

3.3.1 Leeson's Model of Feedback Oscillator

In general, circuit and device noise can perturb both the amplitude and phase of an oscillator's output (Lee and Hajimiri, 2000). A stable oscillator's output can be expressed as

$$v(t) = A\cos(\omega_0 t + \phi(t))$$
(3-45)

It is common to treat $\varphi(t)$ as a zero-mean stationary random process describing deviations of the phase from the ideal. The frequency domain information about

phase or frequency variations is contained in the "power" spectral density $P_{\phi}(\omega_m)$ of the phase $\phi(t)$. ω_m corresponds to the modulation ,video, baseband, or offset frequency associated with the noise-like variations in $\phi(t)$ (Leeson, 1966).

Spectral density of the phase noise can be defined in terms of noise factor of loop amplifier, bandwidth and signal level at oscillator active element input. The input phase noise in 1 Hz bandwidth at any frequency f_0+f_m from the carrier produces a phase deviation can be given by where $2\pi f_m = \omega_m/2\pi$ (Vendelin, Pavio and Rohde, 2005).

$$P_{\phi}(f_m) = \frac{FkTB}{P_{avs}}$$
(3-46)

where F is the noise figure, k is the Boltzmann's constant, T temperature in Kelvin, B bandwidth of the resonator (B=1 for 1 Hz bandwidth) and P_{avs} is the power of the noise at the input of the amplifier.

Close to the carrier frequency, 1/f component (flicker) is added to the noise spectrum frequency so the expression of S_{ϕ} becomes

$$P_{\phi}\left(f_{m}\right) = \frac{FkTB}{P_{avs}} \left(1 + \frac{f_{c}}{f_{m}}\right)$$
(3-47)

where f_c is the flicker frequency.

As explained in the oscillation mechanism, the oscillator can be modeled as an amplifier with a feedback. This relation leads us the fact that the bandwidth of the resonator affects the noise spectrum. At the output of the amplifier, the noise spectrum, $S_{\phi_{out}}$ becomes

$$P_{\phi_{out}}\left(f_{m}\right) = \frac{FkTB}{P_{avs}} \left(1 + \frac{f_{c}}{f_{m}}\right) \left[1 + \frac{1}{f_{m}^{2}} \left(\frac{f_{0}}{2Q_{L}}\right)^{2}\right]$$

where Q_L is the loaded Q factor of resonator, and f_0 is the resonance frequency of the oscillator. And the phase noise at the output of the amplifier is (Leeson, 1966)

$$\mathcal{I}(f_m) = \frac{FkTB}{2P_{avs}} \left[\frac{1}{f_m^3} \frac{f^2 f_c}{4Q_L^2} + \frac{1}{f_m^2} \left(\frac{f}{2Q_L} \right)^2 + \frac{f_c}{f_m} + 1 \right] (dBc / Hz)$$
(3-48)

The Leeson's approach can be reformulated as (Vendelin, Pavio and Rohde, 2005)

$$\mathcal{I}(f_m) = \frac{1}{2} \left[1 + \frac{\omega_0^2}{4\omega_m^2} \left(\frac{P_{i_m}}{\omega_0 W_e} + \frac{1}{Q_u} + \frac{P_{sig}}{\omega_0 W_e} \right)^2 \right] \left(1 + \frac{\omega_c}{\omega_m} \right) \frac{FkT_0}{P_{avs}}$$
(3-49)

phase noise



Figure 3. 5 Oscillator phase noise versus frequency deviation (Lee and Hajimiri, 2000)

where

$$\frac{P_{in}}{\omega_0 W_e} \rightarrow \text{ input power over reactive power}$$
$$\frac{1}{Q_u} \rightarrow \text{ resonator } Q$$
$$\frac{P_{sig}}{\omega_0 W_e} \rightarrow \text{ signal power over reactive power}$$
$$1 + \frac{\omega_c}{\omega_m} \rightarrow \text{ flicker effect}$$
$$\frac{FkT_0}{P_{avs}} \rightarrow \text{ phase perturbation}$$

Equation (3-49) includes important clues of why phase noise appears in the oscillator circuits. One can also find the steps to minimize phase noise effect. Maximizing the reactive power, maximizing the unloaded Q factor, choosing an active device having a low-noise figure, minimizing phase perturbation, coupling the energy from the resonator (like in the dielectric resonator case) and choosing an active device with low flicker noise are some examples of these steps.

CHAPTER FOUR DRO DESIGN AND REALIZATION

4.1 Introduction

The dielectric resonators found large area of usage in the oscillators because of the properties they posses as explained in Chapter 2. Dielectric resonators can both be used in negative resistance (reflection) or feedback type oscillators (Hamilton, 1978). The property of being easily coupled to a microstrip line is another reason to use dielectric resonators on integrated circuits (Day, 1970).

Many types of active devices can be applied to the DRO design. GaAs technology is considered as one of the most suitable transistor for microwave applications because of its good temperature frequency stability and low noise characteristic (Abe, Takayama, Higashisaka and Takamizawa, 1978) (Ishihara, Mori, Sawano and Nakatani, 1980). On the other hand, GaAs MESFET is able to offer better performance than GaAs FET (Tsironis and Lesartre, 1981) (Hilborn, Freundorfer, Show and Keller, 2007).

Considering the advantages of GaAs MESFET, an amplifier chip of GaAs MESFET, MGA72-543 is used as the active device in our circuit. The negative resistance oscillator model is chosen for the design. In the following sections, the design procedure of the DRO will be explained.

4.2 Design Procedure

4.2.1 Dielectric Resonator Simulation

As explained in Chapter 2, the S-Parameter analysis of a dielectric puck coupled to a microstrip line on a substrate is a cumbersome process. High Frequency Structure Simulator, HFSS, is used to compute the S-Parameters of our resonator.

HFSS is a 3D electromagnetic field simulator. With HFSS one can simulate electric and magnetic fields, surface currents, S-parameters, near and far fields of electromagnetic structures. One can form 3-D geometries, define the material properties, the boundary conditions and the necessary excitations for electromagnetic problem of interest.

As discussed in Chapter 2, the placement of the resonator is an important parameter. The width and the length of the microstrip line, as well as the distance of the resonator to the microstrip line must be thoroughly analyzed. The resonator is modeled as parallel RLC resonant circuit an RLC parameters as well as quality factors are calculated from the simulated S-parameter values.

For the microstrip substrate, Taconic TLY 3 CH is used. The substrate has relative dielectric constant of the $2.33 \pm .02$ and substrate height of 0.76 mm. As the dielectric resonator, Trans-Tech 8300 series dielectric resonator is used. The dielectric constant of the resonator is 35.5. It has a radius of The unloaded quality factor of this resonator can be up 15000.

The placement of the resonator can be analyzed using the known equation of input impedance of the transmission line terminated with a load impedance Z_L which is the impedance of the resonator at the resonant frequency. Z_L is known to be very high (ideally open circuit) at the resonance.

$$Z_{in} = Z_0 \frac{Z_L + jZ_0 \tan(\beta l)}{Z_0 + jZ_L \tan(\beta l)}$$

$$\tag{4-1}$$

In order to obtain in impedance equal to Z_L looking into the resonator

$$\tan(\beta l) = 0 \Rightarrow \frac{\sin(\beta l)}{\cos(\beta l)} = 0 \Rightarrow \sin(\beta l) = 0$$

so
$$\beta l = k\pi \text{ k} = 1, 2, 3...$$

where β is the phase constant, *l* is the length of the microstrip line and Z_0 is the characteristic impedance.

It becomes clear that the resonator must be placed in the middle of a $\lambda/2$ microstrip line. The length of the line will be adjusted for oscillations conditions later. Since the dimensions of a microstrip line with the desired characteristic impedance is calculated using the operating frequency, an initial guess of resonant frequency is needed. After that, optimization is necessary to find the optimum microstrip dimension and resonator placement. In order to calculate the proper dimensions of the microstrip line, Advanced Design System Line Calculator is used.

LineCalc le Simulat	ion Options	Help		-	-	
Component			- 536 17 57 56 51 51 15			
Type MLIN	Q		_DEFAULT	<u> </u>		
Substrate	Parameters (3A 2.330 1.000 0.760 24.000 0.018 4.1e7 m t Parameters 4.250		Physical W L Synthesiz Electric Z0 E_Eff	2.230080 25.103400 e a 50.000 180.000	mm v mm v N/A v Analyze	Calculated Results K_Eff = 1.973 A_DB = 0.025 SkinDepth = 0.001
Wall1		mi		Г	N/A -	
Wall2		mil 💌			N/A 💌	
Values are co	onsistent					

Figure 4.1 $\lambda/2$ microstrip line physical parameters.

It can be seen from Figure 4.1 that for our substrate, at 4.25 GHz, the $\lambda/2$ microstrip line must have a width of 2.23 mm and length of 25.10 mm. Figure 4. 2 shows the layout for the DR coupled to the microstrip line. For this layout S-parameters are calculated using high frequency electromagnetic simulation program HFSS v.11.



Figure 4. 2 The layout of the dielectric resonator coupled to a microstrip line

The distance between the dielectric resonator and the microstrip line is chosen as of 1.5 mm. The S-parameters of the simulated dielectric resonator configuration can be seen in Figure 4.3. The resonant frequency is observed as 4.24 GHz. It is clear that near resonant frequency, S_{11} has its maximum value around 0 dB, indicating a full reflection. This means that the oscillator acts like open circuit near resonance.



Figure 4.3 S-parameters of the resonator coupled to the microstrip line



Figure 4.4 Magnitudes of S₁₁ and S₂₁



Figure 4.5 Phases of S_{11} and S_{21}

The magnitudes and phases of S_{11} and S_{22} can be seen in Figure 4.4 and Figure 4.5 respectively. In Figure 4.6 and Figure 4.7 vector electric field and vector magnetic field of the dielectric resonator are shown. The field distribution is consistent with the field distribution of $TE_{01\delta}$ mode of the resonator. It can be seen that the fields are coupled to the microstrip line.



Figure 4.6 The vector electric field of the dielectric resonator coupled to microstrip line at resonant frequency.



Figure 4.7 The vector magnetic field of the dielectric resonator coupled to the microstrip line at resonant frequency.

We can model our dielectric resonator as a parallel RLC resonance circuit using the derived S-parameters. If we measure S_{11_0} and S_{21_0} from Figure 4.4, we can calculate coupling coefficient k as

$$k = \frac{S_{11_0}}{S_{21_0}} = \frac{0.9972}{0.0564} = 17.68 \tag{4-2}$$

4.2.2 Negative Resistance

GaAs PHEMT amplifier MGA-72543 is used as the active device in our design. The amplifier can operate from 0.1 GHz to 6.0 GHz and it has a noise figure of 1.5 dB at 4 GHz.



Figure 4.8 Gate biasing schematic of the MGA-72543 amplifier (MGA 72543 Datasheet, n.d.)



Figure 4.9 Source resistor biasing schematic of the MGA-72543 amplifier (MGA 72543 Datasheet, n.d.)

MGA-72543 can be biased in two ways: Gate bias and source resistor bias. In gate biasing pin 1 and 4 are grounded and a negative bias voltage is applied to gate pin as can be seen from Figure 4.8. This method brings the advantage of directly grounding the pins and reduced instabilities at higher frequencies. Sour resistor method is a simpler way of biasing since no negative voltage is needed at the gate as can be seen from Figure 4.9. Thus source resistor biasing is chosen. Device current I_d is determined by the value of a resistor that will be connected between pin 4 and ground (Figure 4.10). The approximate value of the source resistor can be calculated using

$$R_{bias} = \frac{964}{I_d (mA)} \left(1 - 0.112 \sqrt{I_d} \right)$$
(4-3)



Figure 4.10 Device current versus bias resistor. (MGA 72543 Datasheet, n.d.)

The biasing circuit of the amplifier is designed by modifying the implementation circuit that is given in the datasheet. The device has an Advanced Design System model so it is simulated using Advanced Design System. The operating point is chosen as V_d =3.3V, I_d=22 mA. Also, in order to stabilize DC source, a voltage regulator is used. LM3480, 100 mA voltage regulator is used for this purpose. 3.3V output voltage can be obtained using the circuit in Figure 4.11



Figure 4.11 Voltage regulator for 3.3V output



Figure 4.12 The biasing circuit and the DC solution

The biasing circuit is given in Figure 4.12. The DC solution gives the drain current I_D as 22 mA. The corresponding S-parameters, the load and the stability circles of the circuit is given in Figure 4.13



Figure 4.13 S-parameters of the active device biasing circuit

Use with S_params or Sparams_wNoise Schematic Templates



Figure 4.14 The load and the stability circles of the active device

In order to achieve negative resistance, S_{11} and S_{22} parameters of the active device must be greater than unity. It is even desired to be at least 1.2 for start-up oscillation (Vendelin, Pavio and Rohde, 2005). It can be seen from Figure 4.14 that S_{11} and S_{22} are neither greater than unity nor the stability factor, k is less than unity. In order to achieve these conditions positive feedback must be added.

There are two types of feedback in oscillator circuits: Parallel feedback and series feedback (Vendelin, 1982). Series feedback type oscillator is also called reflection type oscillators. In series feedback resonators, the resonator becomes open circuit at resonant frequency and the power is reflected to the transmission line. Another advantage of series feedback to the parallel feedback is the better phase noise figure. But high power applications need parallel feedback configuration since the coupling from resonator to

transmission line is weak. In our design, the series feedback type is chosen since it is suitable for integrating the negative resistance circuit and the available power is not much of a concern.

The MGA 72543 is a single stage MESFET amplifier. Using this property of the active device, one can obtain the negative resistance by adding a positive feedback element. The feedback element can be added to the source of the FET (Figure 4.15).

If source resistor biasing method is used in order to bias the active device, a DC blocking capacitor should be added before the feedback. Proper length of the microstrip line in order to achieve necessary positive feedback is calculated using Advanced Design System. 47pF of capacitor is used as DC blocking capacitor. The feedback layout can be seen in Figure 4.16.



Figure 4.15 Source feedback FET configuration



Figure 4.16 The negative resistance circuit



Figure 4.17 Magnitude of $S_{11} \mbox{ and } S_{22} \mbox{ and stability factor, } K$



Figure 4.18 Load an source stability circles of the negative resistance.

In Figure 4.17 the magnitudes of S_{11} and S_{22} can be observed. Around the resonant frequency the magnitudes are 2.06 and 2.08 respectively. The stability factor K is -0.398. These values are enough to start the oscillations. If we consider the load and the source stability circles seen in Figure 4.18. Adequate magnitudes are obtained by optimizing the lengths of the transmission lines forming the positive feedback. Using the load and the source stability circles the necessary load and source terminations can be extracted. The real part of the impedance seen looking into the input port of the negative-resistance block can be seen in Figure 4.19 which is negative at the desired frequency.



Figure 4.19 Real part of the impedance seen from the input port of the negative-resistance circuit.

4.2.3 Sensitivity Analysis

Sensitivity analysis in a circuit design, gives information on how circuit components can affect a specific circuit parameter of interest. It is basically the ratio of the rate of change of the circuit parameter to the rate of change of the circuit component. In our case sensitivity analysis of S_{11} , S_{22} , stability factor K and the oscillation frequency with respect to input stub line length, input microstrip line length, output stub line length, feedback microstrip line length, bias microstrip line length, bias resistor value and RF choke inductance value are investigated. The change of S_{11} , S_{22} , stability factor K and the oscillated when the circuit component mentioned above changes 1 percent. The results are given in Figure 4.20, Figure 4.21, Figure 4.22 and Figure 4.23, respectively.



Figure 4.20 Senstivity Analysis of S₁₁



Figure 4.21 Sensitivity Analysis of S₂₂



Figure 4.22 Sensitivity Analysis of stability factor, K



Figure 4.23 Sensitivity Analysis of Oscillation Frequency

According to the figures above, all four parameters are very sensitive to the changes in feedback line length which is an expected situation. The stability factor is also sensitive to the changes in bias resistor. The input matching components input stub and input line length parameters are also effective on oscillator parameters.

4.2.4 Harmonic Balance Analysis

The harmonic balance simulation is a technique for analyzing frequency domain behaviors of non-linear systems. An oscillator can be considered as a nonlinear system which may be represented by a canonical set of differential equations (Ioos and Joseph, 1980). The harmonic balance method tries to find the solution to a steady-state non-linear design by iteratively solving for a set of variables, named as state variables (Vendelin, Pavio and Rohde, 2005). The convergence of the iteration depends on choosing the initial values of state variables and oscillation frequency (Rizzoli, Costanzo and Neri, 1992).

Transient analysis would be so much time consuming because of the dependence of time step to highest frequency present in the system which may not be useful in high frequency non-linear circuits. With the harmonic balance analysis one can calculate the magnitudes and phases of voltages and currents at the output of the oscillator circuit with less simulation time.

For validating our design, Advanced Design System Harmonic Balance Simulation is used. In Figure 4.24 we can see the circuit schematic for harmonic balance simulation purposes.



Figure 4.24 Harmonic balance set-up

The initial value of the oscillation frequency is given as 4 GHz. The simulation is done on a fast computer (Intel Core i7 2.93 GHz, 3 GB RAM, 1 TB HDD), the order of harmonics are chosen as 9. The simulation takes 3.49 seconds. The simulation also calculates the phase noise of the oscillator system.



Figure 4.25 Oscillator output spectrum, oscillation frequency and output waveform of the oscillator simulation done with ADS.



Figure 4.26 Phase noise of the oscillator spectrum

The harmonic balance simulation shows (Figure 4.25) the oscillation frequency as 4.24 GHz and the first harmonic's power as 11.13 dBm. The phase noise relative to the fundamental frequency is about -29.283 dBc.

4.3 The Layout

The layout of the circuit is drawn with Eagle free edition which is depicted in Figure 4.27. The circuit is printed by LPKF ProtoMat S62 which is available in the Printed Circuit Board Laboratory. The capacitors and the inductors are the size of 0805. MGA 72543 is in SOT-73 package. In Figure 4.28 the final board layout can be seen.



Figure 4.27 Layout of the circuit



Dielectric Resonator

4.3 Experimental Results

4.3.1 Output Spectrum

The measurements of the final design is done with Hewlett Packard 8592B spectrum analyzer. The measurement setup can be seen in Figure 4.29 and Figure 4.30. According to this setup, DC source is connected to the DC bias block of the dielectric resonator oscillator. A serial multimeter is connected in order to measure the current I_D which is the device current. The output is connected to the isolator which prevents pulling effect of the spectrum analyzer. The output of the isolator is connected to the spectrum analyzer.



Figure 4.29 Measurement set up



Figure 4.30 Measurement set-up in the Microwave Laboratory

The observed output spectrum of the dielectric resonator can be seen in Figure 4.31. The oscillation frequency is measured as 4.30 GHz. The maximum measured output power is 6.5 dBm which corresponds to 4.47 mW. The second harmonic which is 8.60 GHz and the third harmonic at 12.90 GHz has a power of -45.92 dBm and -13.06 dBm which correspond to 0.26 μ W and 49 μ W, respectively (Figure 4.32 and Figure 4.33).



Figure 4.31 Output spectrum of the dielectric resonator oscillator



Figure 4.32 Power spectrum of the second harmonic of the oscillation frequency.



Figure 4.33 Power spectrum of the third harmonic of the oscillation frequency.

It is necessary to understand whether the oscillation is due to dielectric resonator or not. When the resonator is removed from the circuit the oscillation dampens immediately. When the dielectric resonator is placed the oscillation restarts. It can also be observed that if the dielectric resonator is moved apart from the microstrip line, the resonance frequency changes and the output power reduces. The aluminum chassis needs to be completely closed in order to observe the oscillation.

4.3.2 Phase Noise Analysis

The spectrum analyzer can be used in noise measurements in a simple way. If linear approach is used, the single-sideband noise (\mathcal{I} in dBc/Hz) can be defined as:

$$\mathcal{I}(f_m) = \frac{N(1Hz \text{ BW})}{C}$$
(4-4)

In equation (4-4), N is the power of noise in 1 Hz bandwidth at f_m away from the carrier and C is the power of the carrier. Using a spectrum analyzer, one can calculate \mathcal{I} by reading the carrier power which is the power of oscillation frequency, reading the power at f_m away from the oscillation frequency and calculating the ratio of those two. However, this technique has some drawbacks because of the working principle of the spectrum analyzer (Vendelin, Pavio and Rohde, 2005). The filters and amplifiers at the input of the spectrum analyzer must be taken into as well as the non-existence of 1 Hz bandwidth band pass filters. According to equation (4-4), the noise power must be measured through band pass filter with a bandwidth of 1 Hz. So the measurements must be corrected by reducing the noise power by 10 dB per decade if the internal filter of the spectrum analyzer has a bandwidth larger than 1 Hz.



Figure 4. 34 Oscillator power spectrum (Vendelin, Pavio and Rohde, 2005)

Using these relations the phase noise of the realized DRO is found as in Figure 4.35.



Figure 4.35 Measured phase noise of the realized DRO

CHAPTER FIVE CONCLUSION

The purpose of this thesis is to design and realize a dielectric resonator oscillator operating at 4.2 GHz. Throughout the thesis, microwave resonators were examined. The circuit analysis of series an parallel resonant circuits were studied. The quality factors of resonators were explained for both series and parallel resonant circuits. Then, dielectric materials and dielectric resonators were reviewed. The material properties of dielectric resonators and how they became convenient for oscillator circuits were explained. The researches about the coupling mechanism and its equivalent circuit were revised.

Design of microwave oscillators, the oscillation conditions were discussed and a design procedure from the S-parameters point of view was explained. The negative-resistance oscillator structure was chosen. According to the design steps first, the dielectric resonator which was placed in the middle of a half-wave transmission line was simulated using a 3D electromagnetic field simulator, HFSS. The S-parameters over a range of frequency was exported to Touchstone file format which is a standard file type for most electromagnetic circuit simulators. The amplifier used in the design, MGA-72543, was simulated in order to obtain the DC conditions and small signal parameters using Advanced Design System. Using a single stage amplifier enabled to obtain the device current close to the DC simulations. This ensures that the nearly same S-parameters in the simulation can be obtained when the circuit is realized. The necessary negative-resistance was achieved using a short stub at the source pin of the amplifier which formed positive feedback to the amplifier. The positive feedback enabled the amplifier operate in an unstable mode around the desired oscillation frequency, which is 4.25 GHz in our case. Also harmonic balance analysis was done and the amplitudes of first nine harmonic as well as the output spectrum were derived.

After the final design, the layout of the circuit was drawn using Eagle lite version. The board was printed in the PCB Laboratory of the department. The circuit was mounted in an aluminum chassis. The spectrum of the first three harmonics of the oscillator were measured using the HP 8592B spectrum analyzer. The oscillator operates at 4.3 GHz. The fundamental harmonic of the oscillator is 6.4 dBm. Total harmonic distortion is -20 dBm.
The phase noise measurements gives an overview of the noise performance of the realized DRO despite the drawbacks of the measurement method. -85 dBc/Hz at 10 kHz from the carrier was observed. However, very low noise DRO designs are available in the literature (Lan, Kalokitis, Mykietyn, Hoffman and Sechi, 1986).

As a result, the designed oscillator works with an error of 1.46 percent in terms of oscillation frequency compared to the simulation results. The main reason for this is that the bias conditions were obtained with an error of 1.36 percent in terms of the device current. The difference of harmonic powers between the simulation of the oscillator and the practical one is mainly due to mismatch at the output which occurs as a result of improper soldering of the SMA connector. Also, the chassis should be at the same size of the printed circuit board in order to concentrate the electromagnetic energy inside the chassis. These improvements can be applied in order to obtain more accurate results.

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APPENDICES

TLY

Dimensionally Stable Low Loss Low Moisture Absorption High Peel Strength Uniform & Consistent DK

TLY-5 TYPICAL VALUES							
Property	Test Method	Units	Value	Units	Value		
Dielectric Constant @ 10 GHz	IPC-TM 650 2.5.5.5		2.20		2.20		
Dissipation Factor @ 10 GHz	IPC-TM 650 2.5.5.5		0.0009		0.0009		
Moisture Absorption	IPC-TM 650 2.6.2.1	%	<0.02	%	<0.02		
Dielectric Breakdown	IPC-TM 650 2.5.6	kV	>60	kV	>60		
Volume Resistivity	IPC-TM 650 2.5.17.1	Mohm/cm	10 ⁷	Mohm/cm	10 ⁷		
Surface Resistivity	IPC-TM 650 2.5.17.1	Mohm	107	Mohm	107		
Arc Resistance	IPC-TM 650 2.5.1	seconds	>180	seconds	>180		
Flexural Strength Lengthwise	IPC-TM 650 2.4.4	lbs./in.	>12,000	N/mm ²	>83		
Flexural Strength Crosswise	IPC-TM 650 2.4.4	lbs./in.	>10,000	N/mm ²	>69		
Peel Strength (1oz copper)	IPC-TM 650 2.4.8	lbs./linear in.	12.0	N/mm	2.1		
Thermal Conductivity	ASTM F 433	W/m/K	0.22	W/m/K	0.22		
x-y CTE	ASTM D 3386 (TMA)	ppm/°C	20	ppm/°C	20		
z CTE	ASTM D 3386 (TMA)	ppm/°C	280	ppm/°C	280		
UL-94 Flammability Rating	UL-94		V-0		V-0		









Designation	Dielectric Constant	Dielectric Thickness	Dielectric Thickness
TLY - 5A	2.17 +/02	.0310"	0.78mm
TLY - 5	2.20 +/02	.0050"	0.13mm
TLY - 3	2.33 +/02	.0050"	0.13mm

Standard sheet size is 36" x 48" (914mm x 1220mm). Please contact our Customer Service Department for the availability of other sizes and claddings.

TLY can be ordered with the following electrodeposited copper:

Panels may be ordered cut to size

Designation	Weight	Copper	Copper	Typical Panel Sizes	
	12" x 18"	304mm x 457mm			
СН	1/2 oz./sq. ft.	~ .0007"	~18 μm	16" x 18"	406mm x 457mm
C1		0044		18" x 24"	304mm x 457mm 406mm x 457mm 457mm x 610mm 406mm x 914mm 610mm x 914mm 457mm x 1220mm
	1 oz./sq. ft.	~ .0014"	~ 35 µm	16" x 36"	
C2		0000	70	24" x 36"	406mm x 457mm 457mm x 610mm 406mm x 914mm 610mm x 914mm 457mm x 1220mm
	2 oz./sq. π.	~ .0028*	~ 70 μm	18" x 48"	

An example of our part number is: TLY-5-0100-CH/CH-18" x 24" (TLY-5-0100-CH/CH-457mm x 610mm)

MGA-72543

PHEMT* Low Noise Amplifier with Bypass Switch

Data Sheet

Description

Avago's MGA-72543 is an economical, easy-to-use GaAs MMIC Low Noise Amplifier (LNA), which is designed for an adaptive CDMA receiver LNA and adaptive CDMA transmit driver amplifier.

The MGA-72543 features a minimum noise figure of 1.4dB and 14 dB associated gain from a single stage, feedback FET amplifier. The output is internally matched to 50 Ω . The input is optimally internally matched for lowest noise figure into 50 Ω . The input may be additionally externally matched for low VSWR through the addition of a single series inductor. When set into the bypass mode, both input and output are internally matched to 50 Ω .

The MGA-72543 offers an integrated solution of LNA with adjustable IIP₃. The IIP₃ can be fixed to a desired current level for the receiver's linearity requirements. The LNA has a bypass switch function, which sets the current to zero and provides low insertion loss. The bypass mode also boosts dynamic range when high level signal is being received.

For the CDMA driver amplifier applications, the MGA-72543 provides suitable gain and linearity to meet the ACPR requirements when the handset transmits the highest power. When transmitting lower power, the MGA-72543 can be bypassed, saving the drawing current.

The MGA-72543 is a GaAs MMIC, processed on Avago's cost effective PHEMT (Pseudomorphic High Electron Mobility Transistor). It is housed in the SOT343 (SC70 4-lead) package, and is part of the Avago Technologies CDMAdvantage RF chipset.



Attention: Observe precautions for handling electrostatic sensitive devices. LSU: Machine Model (Class A) ESC Human Body Model (Class O) Refer to Avago Application Note A004R: Bedrostatic Discharge Damoge and Control.

*Pseudomorphic High Electron Mobility Transistor

Features

- Lead-free Option Available
- Operating Frequency: 0.1 GHz~6.0 GHz
- Noise Figure: 1.4 dB at 2 GHz
- Gain: 14 dB at 2 GHz
- Bypass Switch on Chip Loss -2.5 dB (Id < 5 μA) IIP3 = +35 dBm
- Adjustable Input IP3: +2 to +14 dBm
- 2.7 V to 4.2 V Operation
- Very Small Surface Mount Package

Applications

- CDMA (IS-95, J-STD-008) Receiver LNA Transmit Driver Amp
- TDMA (IS-136)Handsets

Surface Mount Package SOT-343 (SC-70)



Pin Connections and Package Marking



Package marking is 3 characters. The last character represents date code. 75

MGA-72543 Absolute Maximum Ratings^[1]

Symbol	Parameter	Units	Absolute Maximum	Operation Maximum
V _d	Maximum Input to Output Voltage	V	5.5	4.2
V _{ref}	Maximum Input to Ground DC Voltage	V	+0.3 -5.5	+0.1 -4.2
l _d	Supply Current	mA	70	60
Pd	Power Dissipation ^[2,3]	mW	300	250
P _{in}	CW RF Input Power	dBm	+20	+13
Tj	Junction Temperature	°C	170	150
TSTG	Storage Temperature	°C	-65 to +150	-40 to +85

Thermal Resistance: [2] $\Theta_{JC} = 200^{\circ}C/W$

Notes:

1. Operation of this device in excess of any of these limits may cause permanent damage. 2. Tease = 25° C.

Simplified Schematic



Functional Block Diagram



MGA-72543 Electrical Specifications

 $T_c = +25^{\circ}C$, $Z_o = 50\Omega$, $I_d = 20$ mA, $V_d = 3V$, unless noted.

Symbol	Parameters and Test Conditions		Units	Min.	Тур.	Max.	σ
Vc[1,3]	$f = 2.0 \text{ GHz}$ $V_d = 3.0 \text{V} (V_{ds} = 2.5 \text{V})$	l _d = 20 mA	V	0.37	0.51	0.65	0.035
NF test ^[1]	$f = 2.0 \text{ GHz}$ $V_d = 3.0 \text{V} (= V_{ds} + \text{Vc})$	l _d = 20 mA	dB		1.5	1.8	0.06
G _a test ^[1]	$f = 2.0 \text{ GHz}$ $V_d = 3.0 \text{V} (= V_{ds} + \text{Vc})$	l _d = 20 mA	dB	13.5	14.4	15.5	0.13
IIP ₃ test ^[1]	$f = 2.04 \text{ GHz}$ $V_d = 3.0 \text{V} (= V_{ds} + \text{Vc})$	l _d = 20 mA	dB	8.5	10.5		0.67
IL test ^[1]	$f = 2.0 \text{ GHz}$ $V_d = 3.0 \text{V} (V_{ds} = 0 \text{V}, V_c = 3 \text{V})$	l _d = 0.0 mA	dB		2.5	3.5	0.01
lg test ^[1]	$f = 2.0 \text{ GHz} \qquad V_d = 3.0 \text{V} (V_{ds} = 0 \text{V}, V_c = 3 \text{V})$	l _d = 0.0 m.A	μA		2.0		2.0
NF _o ^[2]	Minimum Noise Figure As measured in Figure 2 Test Circuit (Γopt computed from s-parameter and noise parameter performance as measured in a 50Ω impedance fixture)	f = 1.0 GHz f = 1.5 GHz f = 2.0 GHz f = 2.5 GHz f = 4.0 GHz f = 6.0 GHz	dB		1.35 1.38 1.42 1.45 1.54 1.70		0.0 4
G _a ^[2]	Associated Gain at Nfo As measured in Figure 2 Test Circuit (Γopt computed from s-parameter and noise parameter performance as measured in a 50Ω impedance fixture)	f = 1.0 GHz f = 1.5 GHz f = 2.0 GHz f = 2.5 GHz f = 4.0 GHz f = 6.0 GHz	dB		14.8 14.2 13.6 13.0 11.2 9.2		0.11
P _{1dB} ^[1]	Output Power at 1 dB Gain Compression As measured in Figure 1 Test Circuit. Frequency = 2.04 GHz	$I_d = 0 \text{ mA}$ $I_d = 5 \text{ mA}$ $I_d = 10 \text{ mA}$ $I_d = 20 \text{ mA}$ $I_d = 40 \text{ mA}$ $I_d = 60 \text{ mA}$	dBm		+15.3 +3.2 +8.3 +11.2 +14.9 +17.1		0.52
IIP ₃ ^[1]	Input Third Order Intercept Point As measured in Figure 1 Test Circuit Frequency = 2.04 GHz	$I_d = 0 \text{ mA}$ $I_d = 5 \text{ mA}$ $I_d = 10 \text{ mA}$ $I_d = 20 \text{ mA}$ $I_d = 40 \text{ mA}$ $I_d = 60 \text{ mA}$	dBm		+35 +3.5 +6.2 +10.5 +12.1 +14.8		0.67
ACP	Adjacent Channel Power Rejection, f = 2 GHZ, offset = 1.25 MHz, Pout = 10 dBm (CDMA modulation scheme) f = 800 MHz, offset = 900 KHz, Pout = 8 dBm As measured in Figure 1 Test Circuit	$I_{d} = 30 \text{ mA}$ $I_{d} = 40 \text{ mA}$ $I_{d} = 20 \text{ mA}$ $I_{d} = 30 \text{ mA}$	dBc		-55 -60 -57 -60		
RL _{in} ^[1]	Input Return Loss as measured in Fig. 1	f = 2.0 GHz	dB		10.2		0.22
RL _{out} [1]	Output Return Loss as measured in Fig. 1	f = 2.0 GHz	dB		19.5		1.1
ISOL ^[1]	Isolation $ S_{12} ^2$ as measured in Fig. 2	f = 2.0 GHz	dB		-23.2		0.16

Notes:
1. Standard Deviation and Typical Data as measured in the test circuit in Figure 1. Data based at least 500 part sample size and 3 wafer lots.
2. Typical data computed from s-parameter and noise parameter data measured in a 50E8 system. Data based on 40 parts from 3 wafer lots.
3. Vc = -Vref test



Figure 1. MGA-72543 Production Test Circuit.



Figure 2. MGA-72543 Test Circuit for S, Noise, and Power Parameters Over Frequency.

MGA-72543 Typical Performance, $T_c = 25^{\circ}C$, $Z_o = 50$, $V_d = 3V$, $I_d = 20$ mA unless stated otherwise. All data as measured in Figure 2 test circuit (Input & Output presented to 50Ω).

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Figure 4. Associated Gain with F min vs. Frequency and Voltage.



Figure 5. Input Third Order Intercept Point vs. Frequency and Voltage.



Figure 6. Minimum Noise Figure vs. Frequency and Temperature.



FREQUENCY (GHz) Figure 7. Associated Gain with F _{min} vs. Frequency and Temperature.



Figure 8. Input Third Order Intercept Point vs. Frequency and Temperature.







Figure 10. LNA off (Switch on) VSWR vs. Frequency.



Figure 11. Insertion Loss (Switch on) vs. Frequency and Temperature.

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MGA-72543 Typical Performance, continued, $T_c = 25^{\circ}C$, $Z_o = 50$, $V_d = 3V$, $I_d = 20$ mA, Frequency = 2 GHz, unless stated otherwise. All data as measured in Figure 2 test circuit (Input & Output presented to 50Ω).

/

80

80

5

1 dB Compression (dBm)

1 dB COMPRESSION (dBm)

NF (dB)

Applications Information: Designing with the MGA-72543 RFIC Amplifier/Bypass Switch

Description

The MGA-72543 is a single-stage, GaAs RFIC amplifier with an

integrated bypass switch. A functional diagram of the MGA-72543 is shown in Figure 1.

The MGA-72543 is designed for receivers and transmitters operating from 100 MHz to 6 GHz with an emphasis on 1.9 GHz CDMA applications. The MGA-72543 combines low noise performance with high linearity to make it especially advantageous for use in receiver front-ends.



Figure 1. MGA-72543 Functional Diagram.

The purpose of the switch feature is to prevent distortion of high signal levels in receiver applications by bypassing the amplifier altogether. The bypass switch can be thought of as a 1-bit digital AGC circuit that not only prevents distortion by bypassing the MGA-72543 amplifier, but also reduces front-end system gain by approximately 16 dB to avoid overdriving subsequent stages in the receiver such as the mixer.

An additional feature of the MGA-72543 is the ability to externally set device current to balance output power capability and high linearity with low DC power consumption. The adjustable current feature of the MGA-72543 allows it to deliver output power levels in excess of +15 dBm (P1dB), thus extending its use to other system applications such as transmitter driver stages.

The MGA-72543 is designed to operate from a +3-volt power supply and is contained in a miniature 4-lead, SOT-343 (SC-70) package to minimize printed circuit board space.

LNA Applications

For low noise amplifier applications, the MGA-72543 is typically biased in the 10 – 20 mA range. Minimum NF occurs at 20 mA as noted in the performance curve of NFmin vs. Id. Biasing at currents significantly less than 10 mA is not recommended since the characteristics of the device began to change very rapidly at lower currents. The MGA-72543 is matched internally for low NF. Over a current range of 10 - 30 mA, the magnitude of É^oopt at 1900 MHz is typically less than 0.25 and additional impedance matching would only net about 0.1 dB improvement in noise figure.

Without external matching, the input return loss for the MGA-72543 is approximately 5 dB at 1900 MHz. If desired, a small amount of NF can be traded off for a significant improvement in input match. For example, the addition of a series inductance of 2.7 to 3.9 nH at the input of the MGA-72543 will improve the input return loss to greater than 10 dB with a sacrifice in NF of only 0.1 dB.

The output of the MGA-72543 is internally matched to provide an output SWR of approximately 2:1 at 1900 MHz. Input and output matches both improve at higher frequencies.

Driver Amplifier Applications

The flexibility of the adjustable current feature makes the MGA-72543 suitable for use in transmitter driver stages. Biasing the amplifier at 40 – 50 mA enables it to deliver an output power at 1-dB gain compression of up to +16 dBm. Power efficiency in the unsaturated driver mode is on the order of 30%. If operated as a saturated amplifier, both output power and efficiency will increase.

Since the MGA-72543 is internally matched for low noise figure, it may be desirable to add external impedance matching at the input to improve the power match for driver applications. Since the reactive part of the input of the device impedance is capacitive, a series inductor at the input is often all that is needed to provide a suitable match for many applications. For 1900 MHz circuits, a series inductance of 3.9 nH will match the input to a return loss of approximately 13 dB.

As in the case of low noise bias levels, the output of the MGA-72543 is already well matched to 50 É∂and no additional matching is needed for most applications.

When used for driver stage applications, the bypass switch feature of the MGA-72543 can be used to shut down the amplifier to conserve supply current during non-transmit periods. Supply current in the bypass state is nominally 2 μ A.

Biasing

Biasing the MGA-72543 is similar to biasing a discrete GaAs FET. Passive biasing of the MGA-72543 may be accomplished by either of two conventional methods, either by biasing the gate or by using a source resistor.

- Gate Bias

Using this method, Pins 1 and 4 of the amplifier are DC grounded and a negative bias voltage is applied to Pin 3 as shown in Figure 2. This method has the advantage of not only DC, but also RF grounding both of the ground pins of the MGA-72543. Direct RF grounding of the device's ground pins results in slightly improved performance while decreasing potential instabilities, especially at higher frequencies. The disadvantage is that a negative supply voltage is required.



Figure 2. Gate Bias Method.

DC access to the input terminal for applying the gate bias voltage can be made through either a RFC or high impedance transmission line as indicated in Figure 2.

The device current, Id, is determined by the voltage at Vref (Pin 3) with respect to ground. A plot of typical Id vs. Vref is shown in Figure 3. Maximum device current (approximately 65 mA) occurs at Vref = 0.



Figure 3. Device Current vs. Vref.

The device current may also be estimated from the fol lowing equation:

Vref = 0.11 VId - 0.96

where d is in mA and Vref is in volts.

The gate bias method would not normally be used unless a negative supply voltage was readily available. For reference, this is the method used in the characterization test circuits shown in Figures 1 and 2 of the MGA-72543 data sheet.

- Source Resistor Bias

The source resistor method is the simplest way of biasing the MGA-72543 using a single, positive supply voltage. This method, shown in Figure 4, places the RF Input (Pin 3) at DC ground and requires both of the device grounds (Pins 1 and 4) to be RF bypassed. Device current, Id, is determined by the value of the source resistance, Rbias, between either Pin 1 or Pin 4 of the MGA-72543 and DC ground. Note: Pins 1 and 4 are connected internally in the RFIC. Maximum device current (approximately 65 mA) occurs for Rbias = 0.



Figure 4. Source Resistor Bias.

A simple method recommended for DC grounding the input terminal is to merely add a resistor from Pin 3 to ground, as shown in Figure 4. The value of the shunt R can be comparatively high since the only voltage drop across it is due to minute leakage currents that in the μ A range. A value of 1 K Ω would adequately DC ground the input while loading the RF signal by only 0.2 dB loss.

A plot of typical Id vs. Rbias is shown in Figure 5.



Figure 5. Device Current vs. R_{bias}.

The approximate value of the external resistor, Rbias, may also be calculated from:

$$Rbias = \frac{964}{Id} (1 \quad 0.112 \sqrt{Id})$$

where Rbias is in ohms and ld is the desired device current in mA.

The source resistor technique is the preferred and most common method of biasing the MGA-72543.

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Adaptive Biasing

For applications in which input power levels vary over a wide range, it may be useful to dynamically adapt the bias of the MGA-72543 to match the signal level. This involves sensing the signal level at some point in the system and automatically adjusting the bias current of the ampli fier accordingly. The advantage of adaptive biasing is conservation of supply current (longer battery life) by using only the amount of current necessary to handle the input signal without distortion.

Adaptive biasing of the MGA-72543 can be accomplished by either analog or digital means. For the analog control case, an active current source (discrete device or IC) is used in lieu of the source bias resistor. For simple digital control, electronic switches can be used to control the value of the source resistor in discrete increments. Both methods of adaptive biasing are depicted in Figure 6.



A DC blocking capacitor at the output of the RFIC isolates the supply voltage from succeeding circuits. If the source resistor method of biasing is used, the RF input terminal of the MGA-72543 is at DC ground potential and a blocking capacitor is not required unless the input is connected directly to a preceding stage that has a DC voltage present.



Figure 7, DC Schematic for Gate Bias.



Figure 8. DC Schematic of Source Resistor Biasing.

Figure 6. Adaptive Bias Control.

Applying the Device Voltage

Common to all methods of biasing, voltage Vd is applied to the MGA-72543 through the RF Output connection (Pin 2). A RF choke is used to isolate the RF signal from the DC supply. The bias line is capacitively bypassed to keep RF from the DC supply lines and prevent resonant dips or peaks in the response of the amplifier. Where practical, it may be cost effective to use a length of high impedance transmission line (preferably $\lambda/4$) in place of the RFC.

When using the gate bias method, the overall device voltage is equal to the sum of Vref at Pin 3 and voltage Vd at Pin 2. As an example, to bias the device at the typical operating voltage of 3 volts, Vd would be set to 2.5 volts for a Vref of -0.5 volts. Figure 7 shows a DC schematic of a gate bias circuit.

Just as for the gate bias method, the overall device voltage for source resistor biasing is equal to Vref + Vd. Since Vref is zero when using a source resistor, Vd is the same as the device operating voltage, typically 3 volts. A source resistor bias circuit is shown in Figure 8.

Biasing for Higher Linearity or Output Power

While the MGA-72543 is designed primarily for use up to 50 mA in +3 volt applications, the output power can be increased by using higher currents and/or higher supply voltages. If higher bias levels are used, appropriate caution should be observed for both the thermal limits and the Absolute Maximum Ratings.

As a guideline for operation at higher bias levels, the Maximum Operating conditions shown in the data sheet table of Absolute Maximum Ratings should be followed. This set of conditions is the maximum combination of bias voltage, bias current, and device temperature that is recommended for reliable operation. Note: In contrast to Absolute Maximum ratings, in which exceeding any *one* parameter may result in damage to the device, *all* of the Maximum Operating conditions may reliably be applied to the MGA-72543 *simultaneously*.

Controlling the Switch

The state of the MGA-72543 (amplifier or bypass mode) is controlled by the device current. For device currents greater than 5 mA, the MGA-72543 functions as an amplifier. If the device current is set to zero, the MGA-72543 is switched into a bypass mode in which the amplifier is turned off and the signal is routed around the amplifier with a loss of approximately 2.5 dB.

The bypass state is normally engaged in the presence of high input levels to prevent distortion of the signal that might occur in the amplifier. In the bypass state, the input TOI is very high, typically +39 dBm at 1900 MHz.

The simplest method of placing the MGA-72543 into the bypass mode is to open-circuit the ground terminals at Pins 1 and 4. With the ground connection open, the internal control circuit of the MGA-72543 auto-switches from the amplifier mode into a bypass state and the device current drops to near zero. Nominal current in the bypass state is 2 μ A with a maximum of 15 μ A.



Figure 9. MGA-72543 Amplifier/Bypass State Switching.

An electronic switch can be used to control states as shown in Figure 9. The control switch could be implemented with either a discrete transistor or simple IC.

The speed at which the MGA-72543 switches between states is extremely fast and will normally be limited by the time constants of external circuit components, such as the bias circuit and the bypass and blocking capacitors.

The input and output of the MGA-72543 while in the bypass state are internally matched to 50 Éd. The input return loss can be further improved at 1900 MHz by adding a 2.7 to 3.9 nH series inductor added to the input. This is the same approximate value of inductor that is used to improve input match when the MGA-72543 is in the amplifier state.

Thermal Considerations

Good thermal design is always an important consideration in the reliable use of any device, since the Mean Time To Failure (MTTF) of semiconductors is inversely proportional to the operating temperature.

The MGA-72543 is a comparatively low power dissipation device and, as such, operates at conservative temperatures. When biased at 3 volts and 20 mA for LNA applications, the power dissipation is 3.0 volts x 20 mA, or 60 mW. The temperature increment from the RFIC channel to its case is then 0.060 watt x 200°C/watt, or only 12°C. Subtracting the channel-to-case temperature rise from the suggested maximum junction temperature of 150°C, the resulting maximum allowable case temperature is 138°C.

The worst case thermal situation occurs when the MGA-72543 is operated at its Maximum Operating conditions in an effort to maximize output power or achieve minimum distortion. A similar calculation for the Maximum Operating bias of 4.2 volts and 60 mA yields a maximum allowable case temperature of 100°C. This calculation further assumes the worst case of no RF power being extracted from the device. When operated in a saturated mode, both power-added efficiency and the maximum allowable case temperature will increase.

Note: "Case" temperature for surface mount packages such as the SOT-343 refers to the interface between the package pins and the mounting surface, i.e., the temperature at the PCB mounting pads. The primary heat path from the RFIC chip to the system heatsink is by means of conduction through the package leads and ground vias to the groundplane of the PCB.

PCB Layout and Grounding

When laying out a printed circuit board for the MGA-72543, several points should be considered. Of primary concern is the RF bypassing of the ground terminals when the device is biased using the source resistor method.

Package Footprint

A suggested PCB pad print for the miniature,4-lead SOT-343 (SC-70) package used by the MGA-72543 is shown in Figure 10. This pad print provides allowance for package placement by auto- mated assembly equipment without adding excessive parasitics that could impair the high frequency performance of the MGA-72543. The layout is shown with a footprint of the MGA-72543 superimposed on the PCB pads for reference.



Figure 10. Recommended PCB Pad Layout for Avago's SC70 4L/SOT-343 Products.

RF bypass

For layouts using the source resistor method of biasing, both of the ground terminals of the MGA-72543 must be well bypassed to maintain device stability. Beginning with the package pad print in Figure 10, an RF layout similar to the one shown in Figure 11 is a good starting point for using the MGA-72543 with capacitor-bypassed ground terminals. It is a best practice to use multiple vias to minimize overall ground path inductance.

Two capacitors are used at each of the PCB pads for both Pins 1 and 4. The value of the bypass capacitors is a balance between providing a small reactance for good RF grounding, yet not being so large that the capacitor's parasitics introduce undesirable resonances or loss. If the source resistor biasing method is used, a ground pad located near either Pin 1 or 4 pin may be used to connect the current-setting resistor (Rbias) directly to DC ground. If the Rbias resistor is not located immediately adjacent to the MGA-72543 (as may be the case of dynamic control of the device 's linearity), then a small series resistor (e.g., 10Ω) located near the ground terminal will help de-Q the connection from the MGA-72543 to an external currentsetting circuit.

PCB Materials

FR-4 or G-10 type dielectric materials are typical choices for most low cost wireless applica- tions using single or multilayer printed circuit boards. The thickness of singlelayer boards usually range from 0.020 to 0.031 inches. Circuit boards thicker than 0.031 inches are not recommended due to excessive induc- tance in the ground vias.

Application Example

An example evaluation PCB layout for the MGA-72543 is shown in Figure 12. This evalua- tion circuit is designed for operation from a +3-volt supply and includes provision for a 2-bit DIP switch to set the state of the MGA-72543. For evaluation purposes, the 2-bit switch is used to set the device to either of four states: (1)bypass mode – switch bypasses the amplifier, (2)low noise amplifier mode – low bias current, (3)and (4) driver ampli- fier modes – high bias currents.

A completed evaluation amplifier optimized for use at 1900 MHz is shown with all related components and SMA connectors in Figure 13. A schematic diagram of the evaluation circuit is shown in Figure 14 with component values in Table 1. The on-board resistors R3 and R4 form the equivalent source bias resistor Rbias as indicated in the schematic diagram in Figure 14. In this example, resistor values of R3 = 10Ω and R4 = 24Ω were chosen to set the nominal device current for the four states to: (1) bypass mode, 0 mA, (2) LNA mode, 20 mA, (3) driver, 35 mA, and, (4) driver, 40 mA.



Figure 11. Layout for RF Bypass.



Figure 12. PCB Layout for Evaluation Circuit.

Other currents can be set by positioning the DIP switch to the bypass state and adding an external bias resistor to Vcon. Unless an external resistor is used to set the current, the Vcon terminal is left open. DC blocking capacitors are provided for the both the input and output.

The 2-pin, 0.100" centerline single row headers attached to the Vd and Vcon connections on the PCB provide a convenient means of making connections to the board using either a mating connector or clip leads.

A Note on Performance

Actual performance of the MGA-72543 as measured in an evaluation circuit may not exactly match the data sheet specifications. The circuit board material, passive components, RF bypasses, and connectors all introduce losses and parasitics that degrade device performance. For the evaluation circuit above, fabricated on 0.031-inch thick GETEK^[1] G200D ($\varepsilon r = 4.2$) dielectric material, circuit losses of about 0.3 dB would be expected at both the input an output sides of the RFIC at 1900 MHz. Measured noise figure (3 volts, 20 mA bias) would then be approximately 1.8 dB and gain 13.8 dB.

MGA-71, MGA-72 HM 8/98

Figure 13. Completed Amplifier with Component Reference Designators.

Table 1. Component Values for 1900 MHz Amplifier.

R1 =	5.1 KΩ	C (3 ea)	=100 pF	_
R2 =	5.1 KΩ	C (3 ea)	=1000 pF	_
R3 =	10Ω	C1	=100 pF	
R4 =	24Ω	C2	= 4 7 pF	_
L1 =	3.9 nH	C3	= 30 pF	_
RFC =	22 nH	C4	= 22 pF	
SW1, SW2	DIP switch	C5	=22 pF	_
SC	Short	(6	=30 pF	_

Hints and Troubleshooting • Preventing Oscillation

· Freventing vstillation

Stability of the MGA-72543 is dependent on having very good RF grounding. Inadequate device grounding or poor PCB layout techniques could cause the device to be potentially unstable.

[1] General Electric Co.



Figure 14. Schematic Diagram of 1900 MHz Evaluation Amplifier.