DOKUZ EYLÜL UNIVERSITY
GRADUATE SCHOOL OF NATURAL AND APPLIED SCIENCES

DESIGNING A MODULE FOR REALISATION AND TEST OF SMPS TRANSFORMER

by
Serkan ÜNAL

June, 2012
İZMİR

DESIGNING A MODULE FOR REALISATION AND TEST OF SMPS TRANSFORMER

A Thesis Submitted to the
Graduate School of Natural and Applied Sciences of Dokuz Eylül University
In Partial Fulfillment of the Requirements for the Degree of Master of Science in Electrical and Electronics Engineering

by
Serkan ÜNAL

June, 2012
İZMİR

M.Sc THESIS EXAMINATION RESULT FORM

We have read the thesis entitled **"DESIGNING A MODULE FOR REALISATION AND TEST OF SMPS TRANSFORMER"** completed by **SERKAN ÜNAL** under supervision of **PROF. DR. UĞUR ÇAM** and we certify that in our opinion it is fully adequate, in scope and in quality, as a thesis for the degree of Master of Science.

Prof. Dr. Uğur ÇAM

Supervisor

Prof.Dr. Haldun Karaca

(Jury Member)

Doç.Dr. Mustafa Taparlı

(Jury Member)

Prof.Dr. Mustafa SABUNCU

Director

Graduate School of Natural and Applied Sciences

ACKNOWLEDGEMENTS

I would like to thank to Dokuz Eylül University Graduate School Of Natural And Applied Sciences for my whole gaining across my graduate education.

I would also like to thank my family because of their continuous support.

Serkan ÜNAL

DESIGNING A MODULE FOR REALISATION AND TEST OF SMPS TRANSFORMER

ABSTRACT

Digital control of SMPS systems become popular due it provides new capabilities as parameter tuning according to passive elements, adaptive power conditioning and it is more flexible. In digital platforms that require digital representations of system working parameters as working frequency, duty cycle, etc, as digital power supplies used in laboratories, personal computers that can monitor and change the voltage levels according to the performance need of the CPU, digital control of SMPS can be beneficial. There can be many applications which need the operation parameters and voltage levels.

This thesis presents realization and test of a control scheme of a test device that tests SMPS (Switch Mode Power Supply) systems. In order to realize this task, study takes help of digital control techniques.

Device proposed by this study basically acts as a SMPS controller and finds the optimum working point of the system, namely, best frequency and the duty cycle. So the designer of the SMPS system and the magnetics can easily decide what is the condition of the design and if there needs any adjustments. A PCB board is made for the device. Control of the device is realized through a CPLD (Complex Programmable Logic Device). Gate drive PWM signals, device's LCD's conrol, buton and information LEDs control are implemented in a VHD code running over the CPLD. Tests are realized with a commercial power suplly board of a TV. Same tests are also realized with a sample test setup. Test results are also presented.

Keywords: SMPS, digital control of SMPS, VHDL, LCD driver implemented with VHDL.

SMPS TRAFOSU TASARIMI VE TESTİ NİN GERÇEKLENMESİ İÇİN BİR MODÜL TASARIMI

ÖZ

SMPS sistemlerinin sayısal kontrolü daha esnek olması, sistem içinde otomatik olarak ayar yapılabilmesi ve güç yönetimi yapılabilmesi gibi yetenekleri sayesinde populer olmaya başlamıştır. Laboratuvarlarda kullanılan sayısal güç kaynağı, kişisel bilgisayarlardaki dahili voltajların monitor edilmesi ve seviyesinin performans ihtiyacına göre ayarlanması gibi çalışma parametrelerinin sayısal bilgisine ihtiyaç duyulan sistemlerde sayısal control teknikleri kullanılabilir.

Bu tezde SMPS (Switch Mode Power Supply) sistemlerini test eden bir cihazın kontrol mekanizmasının uygulanması ve test edilmesi sunulmuştur. Çalışma bu görevi yerine getirirken sayısal control tekniklerinden yararlanmıştır.

Cihaz temel olarak bir SMPS denetçisi gibi davranır ve test edilen sistem için en iyi çalışma noktasını bulur. En iyi çalışma noktasındaki kasıt en iyi çalışma frekansı ve en iyi çalışma çevrimi oranıdır. Bu sayede tasarımcı SMPS sisteminin ve manyetik elemanların durumunu belirler ve bir düzeltmenin gerekip gerekmediğini anlayabilir. Bahsedilen cihaz için bir PCB kartı yapılmıştır. Cihazdaki kontrol fonksiyonları bir CPLD vasitası ile gerçeklenmiştir. Anahtarlama elemanları sürücü sinyalleri, cihazın LCDsinin kontrolü, tuş ve bilgilendirme LEDlerinin kontrolu bu CPLD de koşan bir VHDL kodunda gerçeklenmiştir. Bir televizyon güç kaynağı ile testler yapılmıştır. Cihazın ideal olmayan bir sistemin testindeki performansını gözlemek amacıyla örnek bir test düzeneği ile aynı testler tekrar yapılmıştır. Sonuçlar aktarılmıştır.

Anahtar Sözcükler: SMPS, SMPS sistemlerinin sayısal kontrolü, VHDL, VHDL diliyle LCD sürücü uygulaması.

CONTENTS

Page

CHAPTER ONE
INTRODUCTION

SMPS (Switch Mode Power Supply) is a very common part of electronic devices. Almost all electronic devices require a voltage conversion. Power supplies are used for these conversions. Some common power supplies are linear regulators and SMPS systems. For system reliability performance of power supply is very critical. For a SMPS system, design and verification of inductor is the core work. Beside inductor, passive elements as switching components (mosfets and diodes), filter components and active components as SMPS controller is also important. But for an SMPS system inductor performance determines the system performance. Choice of inductor starts with determining power density, desired topology, mechanical limitations, isolation requirements, and input and output voltage levels. Then calculation of number of turns, required core area, wire thickness and resistance of wounds, or leakage inductance (ex. for resonant topologies) of the inductor follows. There are common equations to find these parameters for each SMPS topology. Details of power transformer design relations can be reached from "Switching Power Supply Design Book" of Pressman A.I., 1991. Here it is a burden to state all equations. After these parameters calculated, inductor is realized and tested to be verified. Inductor design always requires iterations. Often some of these parameters are needed to be adjusted according to results of these tests. Design duration is mostly determined by this inductor sample preparation, testing and defining the required adjustments.

At this point this study claims to propose a device that can be used to determine which parameters are suitable, which are not, what should be done to fix inappropriate parameters. For this purpose device determines the best working frequency and PWM duty cycle for a transformer for a specific input voltage, output voltage, output current, selected topology and filter values. Device works as a SMPS controller, has closed loop control and PWM gate drivers. This device is called SMPS transformer test device through this thesis. Finding the best working frequency and PWM duty cycle, user can easily decide what to do, to reach his goal working point. Device will produce gate driver signals to switching components.

Device will have connections to open loop system which is subject to test. These connections are PWM gate drivers for switching components, output voltage sense ADC signal, switching component current sense ADC signal and reference ground. User should connect these signals and arrange open loop system which is subject to test. Open loop system is input supply, transformer connected to input supply, switching components, the output filter and the load. User should arrange the input voltage, switching component, output filter and load. For this study a sample handmade SMPS system and a television power supply board is used for verification of SMPS transformer test device.

After device connections are mounted and device is run, device starts switching the gates of switching components, monitors the output voltage and switching component current and settles to a frequency and PWM duty cycle point according to the value given for output voltage level by user, and according to system parameters as inductance, capacitance and load. Device shows these frequency and PWM duty cycle value on its LCD screen.

Device uses a digital control technique at control loop in order to regulate PWM duty cycle. Study claims that, although analog controller ICs are still dominant and cheaper, digital control is more suitable for such a system as in the study that you can easily derive the digital numerical value of switching frequency and duty cycle, that the final goal of the study is to present the best operating values. All parameters are stored in digital form, so you can easily use these values to realize digital functions, as printing the values on the LCD. Also decreasing costs of programmable devices as PLDs, CPLDs and FPGAs is another point that why study chose digital control.

There are some limitations at analog control of SMPS systems. Analog components are vulnerable to the environmental influence, such as temperature, aging, noise, tolerance of fabrication, which results in lack of flexibility, low reliability, not to mention the parameter auto-tuning and system diagnosis. Besides it is difficult to apply sophisticated control algorithms with an analog approach implementation. In addition, to meet the size miniaturization demand, high switching

frequencies is inappropriate. However in higher switching frequency operation, the analog controller signal transmission through the process will suffer from the limitation of band-width and large gain variation. The variability of the integration technology is more critical with higher switching frequency. Although analog control is still dominating in SMPS applications, it is less adequate to meet the complex requirements of higher switching frequency for the reduction of passive components and dynamic response in today's portable devices (Guo, 2009). This study finds it logical to focus on digital control techniques of SMPS systems, because analog control of SMPS advanced enough and there will not any progress in analog control techniques. But digital control is a new topic and includes a big progress possibility

Considering digital control of SMPS systems, there are applications with PICs, DSPs and PLDs. Although there are cheap remarkable SMPS solutions through DSPs or PICs, study focuses on a PLD solution because it becomes cheaper, and more proper to implement a control loop of a SMPS system which requires concurrent calculations. By just adding two ADCs to a CPLD you can easily realize a SMPS controller in a single chip. So it will replace all the circuitry used with analog SMPS control. It does not require any memory device to hold program code as in standard FPGAs. A CPLD can also run as high as 500 MHz. In this study XC2C512 CPLD is used. It has 512-macrocell which is found optimal for this study. VHD code of this study occupied 86 percent of macrocells of XC2C512 CPLD.

This thesis's main task is to realize a device that finds the optimum working point of a tested SMPS system. In order to realize this, device proposed by this thesis should mimic SMPS controllers. Device also has to realize the LCD driving and other user interface functions. So device should have a digital control unit, because all LCD and user interface units are digital. At this point, study finds it logical to use a single smart chip to realize all this works. SMPS control issues also should be implemented in this chip. So it is better to use a digital control technique which is implemented in chip, for mimicking SMPS controller.

Even though the advantages of digital control are very attractive, there are some issues that should be carefully considered in practical implementation. Analog to digital conversion time, resolution of this conversion, resolution of PWM generation unit or DPWM (Digital PWM) unit, speed of control algorithm should be decided carefully for system bandwidth and meeting specs.

Considering digital control algorithms for SMPS systems, there are PID algorithm control, fuzzy logic control and look-up table (or feed-forward) control approaches. Fuzzy logic control is realized by modifying some coefficients that are used to determine PWM duty cycle. System works as neural network, there are calculation joints, whose parameters are modified according to inputs and the previous output. System measures voltage or current of SMPS system and determines the PWM duty cycle. A fuzzy logic system can be viewed as a 3-layer feed forward neural network. The first layer represents input variables, the middle (hidden) layer represents fuzzy rules and the third layer represents output variables. Fuzzy sets are encoded as (fuzzy) connection weights (Bay&Atacak, 2005). System educates itself and learns the goal system as it works.

Look-up table approach is based on some defined tables which are the coefficients of closed loop PID control equation. For each input condition, system has a dedicated table and retrieves this table to determine the PWM duty cycle. Look-up table approach computes the expected pwm duty cycle based on input-output voltages, currents, and circuit topology.

With the advent of modern DSPs and microprocessors, the PID algorithm is being improved. With a computer, knowledge of the application system can be used to add more terms to the PID equation so the control loop does not have to be purely reactive to an output state. Given the input voltage, system component values, and the desired output voltage, an ideal control loop command output can be calculated. This calculated ideal command is called the “Feed-Forward” term. The feed-forward term is added to the standard PID error terms. Other system aspects, such as anticipated load current changes, may also be added to the feed-forward calculations.

For example: If a processor is in sleep mode, and it is about to enter active operation, it can provide a signal to the power supply to begin increasing the current supply. Feed-forward terms can anticipate system changes before they are reflected in the output state of the power supply. As more information can be integrated into the feed-forward terms, the output errors become smaller, and fewer unexpected transients will be encountered.

With modern DSPs, the circuit equations for an SMPS system can be directly solved yielding voltage and current values without directly measuring them. This capability can circumvent stability issues created by system component induced measurement delays that plague traditional control techniques. Look-up table approach makes use of these benefits.

These two approaches require a memory to store information, namely calculated coefficients at fuzzy logic control and look-up tables at look-up table approach. In these two approaches revising the control behavior no longer requires circuit board or component change, instead a new system can be adopted just by updating the control program in flash.

In the PID algorithm control approach the proportional error, the integral error, and the derivative error of the actual output versus the desired output voltage are summed to control the PWM duty cycle. The proportional term is the error between the desired output state and the actual output state. The derivative term is the change in the proportional error over time. If the derivative error is non zero then it indicates that the system's conditions are changing rapidly. The integral error is the slow accumulation of the proportional errors. The integral error will drive the control system to the final end point. Analog ICs generally use PID algorithm. PID algorithms are also commonly used with digital control techniques. Digital control techniques can utilize both output voltage and inductor current, so current mode and voltage mode techniques can be combined. The classic proportional, integral, derivative (PID) controller is a parallel filter structure. It is useful to express the filter in this form mathematically as in Equation 1.1.

$$G_c(z) = \frac{d(z)}{e(z)} = K_P + K_I \frac{z}{z-1} + K_D \frac{z-1}{z-\alpha}$$

Equation 1.1

In Equation 4.1, we see that a PID compensator is the sum of the voltage error multiplied by a proportional gain, KP, the voltage error multiplied by a integral gain, KI, and accumulated, and the voltage error subtracted from the previous voltage error and multiplied by KD. We can multiply this expression out so that it is expressed as a ratio of polynomials with a common denominator as in Equation 1.2.

$$G_c(z) = \frac{(K_P + K_I + K_D)z^2 - (K_P(1+\alpha) + K_I\alpha + 2K_D)z + (K_P\alpha + K_D)}{z^2 - (1+\alpha)z + \alpha}$$

Equation 1.2

In digital world, this expression can be represented as in Figure 1.1. d[n] is the duty cycle at the time. e[n] is the difference between goal output voltage and the voltage at the time. dI[n] is the integrator state and represents the average duty cycle for the controlled loop. dD[n] is the derivative state and is zero at steady state. Of the three K gains, KD is the largest and is a function of the location of the zeros in the compensator-transfer function (Hagen&Yousefzadeh,2008).

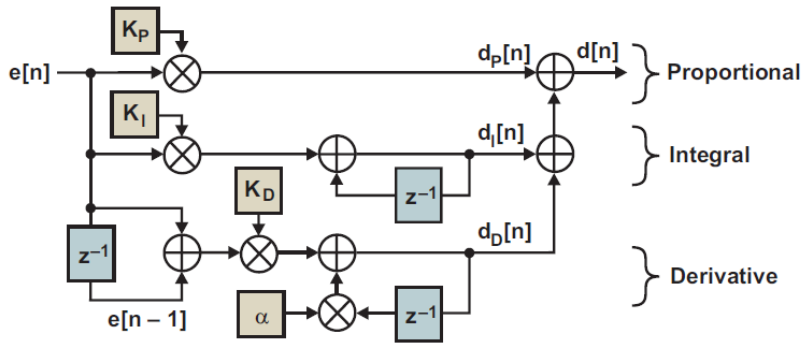


Figure 1.1 PID digital compensator filter implementation (Zhao&Prodic,2007).

This structure is used by many researches. Some modifications can be implemented in different algorithms, but generally, algorithms use the present value of the output voltage error, and the errors of one and two switching cycles before or

the present value of the inductor current, and the errors of one and two switching cycles before, or both.

The control algorithm of PID technique is almost as in Figure 1.2. If an adaptive algorithm is the aim, DAC is used to produce Vref. But if an adaptive control is not the case, Vref can be derived from a fixed value and structure, so DAC is not needed in this case. Error ADC, compensator control law and digital PWM generator unit are the main parts of a PID digital control algorithm.

Although these digitally controlled switching converters showed new features such as estimation and prediction techniques, implementation of nonlinear and fuzzy control law, they operated at switching frequency in range of tens of kHz which made them inferior in comparison to commercially available analog controlled systems that usually operate at much higher switching frequencies (>1MHz).

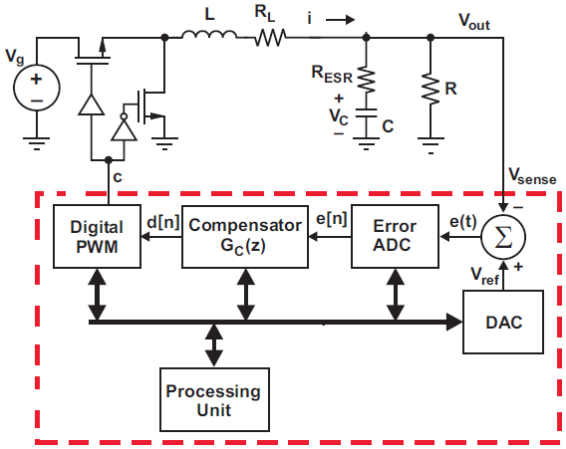


Figure 1.2 PID digital control algorithm in a SMPS.

Therefore broader acceptance of digital techniques in low-power high-frequency SMPS applications is still hampered by a combination of issues of cost, performance and power consumption. Recently, due to the rapid development of VLSI technologies and digital CMOS technique, more and more research focus on the practical implementation of high performance digital control in low power portable electronics system. The main issues are processing/sampling (ADC) delay, limited resolution of ADC and DPWM, quantization error and limit cycle and requirements of real-time regulation, etc. Low-power digital controller architectures are seldom

available that can support operation at constant switching frequencies significantly higher than MHz, which results in high power consumption in control-law algorithm computation and DPWM generator. The power consumption of controller is always compared with system output power, which causes a poor efficiency in low-power portable system at high-frequency, where the analog counterparts take less power. So there needs a big research at more efficient digital control techniques at higher frequencies. Progress generally passes through the optimization of current technologies, so this study find it logical to proceed with already developed PID control and DPWM techniques. Next chapter will explain the details of the methodology to realize this.

1.1 Outline

This thesis is presented in five chapters.

In chapter two, a brief review was given about programmable logic devices, especially CPLDs and about programmable logic language, VHDL.

Chapter three introduces fundamentals of power supplies, especially about SMPS and flyback type SMPS.

Chapter four presents what is done with this thesis and explains the methods utilized through the study.

Chapter five includes conclusion and the gainings from this study. It also gives some suggestions for future works.

CHAPTER TWO
PROGRAMMABLE LOGIC OVERVIEW

2.1 What is Programmable Logic Device

The goal of this thesis is to develop FPGA realizations of three popular image processing algorithms on two FPGA architectures: the Altera FLEX 10K100 and the Xilinx Virtex

A programmable logic device is an electronic component used to build reconfigurable digital circuits. Field-Programmable Device (FPD), a general term that refers to any type of integrated circuit used for implementing digital hardware, where the chip can be configured by the end user to realize different designs. Another name for FPDs is programmable logic devices (PLDs); although PLDs encompass the same types of chips as FPDs, the term FPD is preferred because historically the word PLD has referred to relatively simple types of devices. Unlike a logic gate, which has a fixed function, a PLD has an undefined function at the time of manufacture. Many types of programmable logic are available. The current range of offerings includes everything from small devices capable of implementing only a handful of logic equations to huge FPGAs that can hold an entire processor core (plus peripherals). In addition to this difference in size there is also much variation in architecture.

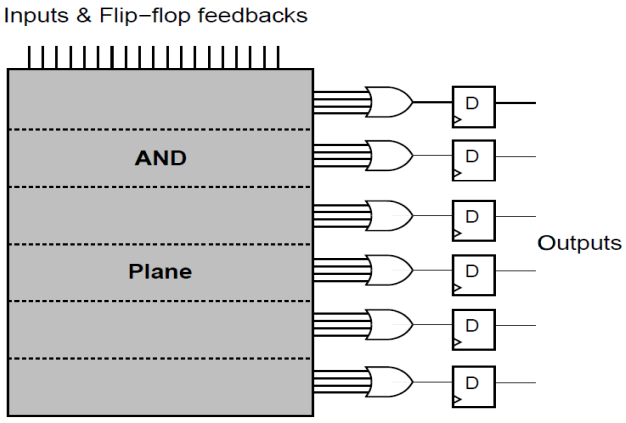


Figure 2.1 Structure of a PAL(Brown&Rose,2004).

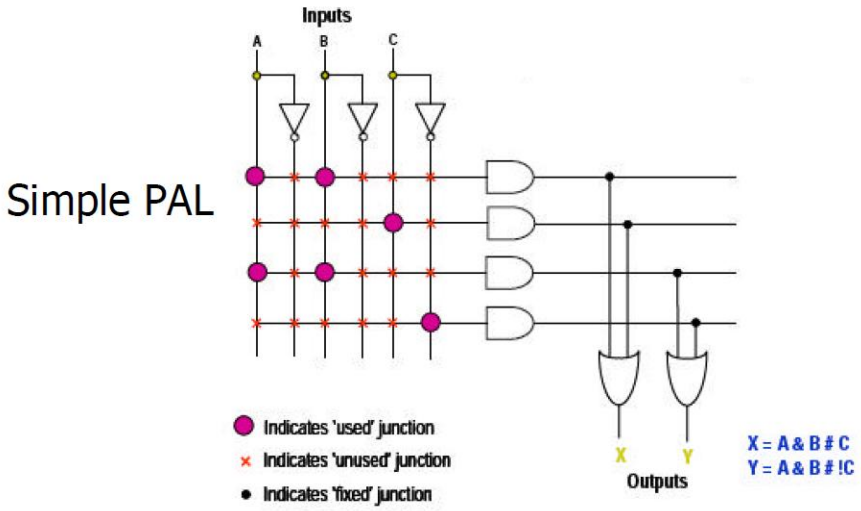


Figure 2.2 More close look to a PAL.

2.2 The Evolution of Programmable Devices

The first type of user-programmable chip that could implement logic circuits was the Programmable Read-Only Memory (PROM), in which address lines can be used as logic circuit inputs and data lines as outputs. Logic functions, however, rarely require more than a few product terms, and a PROM contains a full decoder for its address inputs. PROMS are thus an inefficient architecture for realizing logic circuits, and so are rarely used in practice for that purpose. The first device developed later specifically for implementing logic circuits was the Field-Programmable Logic Array (FPLA), or simply PLA for short. A PLA consists of two levels of logic gates: a program mable “wired” AND-plane followed by a programmable “wired” OR-plane. A PLA is structured so that any of its inputs (or their complements) can be AND’ed together in the AND-plane; each AND-plane output can thus correspond to any product term of the inputs. Similarly, each ORplane output can be configured to produce the logical sum of any of the AND-plane outputs. With this structure, PLAs are well-suited for implementing logic functions in sum-of-products form. They are also quite versatile, since both the AND terms and OR terms can have many inputs (this feature is often referred to as wide AND and OR gates)((Brown&Rose,2004).

When PLAs were introduced in the early 1970s, by Philips, their main drawbacks were that they were expensive to manufacture and offered somewhat poor speed-

performance. Both disadvantages were due to the two levels of configurable logic, because programmable logic planes were difficult to manufacture and introduced significant propagation delays. To overcome these weaknesses, Programmable Array Logic (PAL) devices were developed. As Figure 2.2 illustrates, PALs feature only a single level of programmability, consisting of a programmable “wired” AND plane that feeds fixed OR-gates. To compensate for lack of generality incurred because the OR plane is fixed, several variants of PALs are produced, with different numbers of inputs and outputs, and various sizes of OR-gates. PALs usually contain flip-flops connected to the OR-gate outputs so that sequential circuits can be realized. PAL devices are important because when introduced they had a profound effect on digital hardware design, and also they are the basis for some of the newer, more sophisticated architectures that will be described shortly. Variants of the basic PAL architecture are featured in several other products known by different acronyms. All small PLDs, including PLAs, PALs, and PAL-like devices are grouped into a single category called Simple PLDs (SPLDs), whose most important characteristics are low cost and very high pin-to-pin speed-performance. As technology has advanced, it has become possible to produce devices with higher capacity than SPLDs. The difficulty with increasing capacity of a strict SPLD architecture is that the structure of the programmable logic-planes grow too quickly in size as the number of inputs is increased. The only feasible way to provide large capacity devices based on SPLD architectures is then to integrate multiple SPLDs onto a single chip and provide interconnect to program connect the SPLD blocks together. Many commercial FPD products exist on the market today with this basic structure, and are collectively referred to as Complex PLDs (CPLDs) (Brown&Rose,2004).

CPLDs were pioneered by Altera, first in their family of chips called Classic EPLDs, and then in three additional series, called MAX 5000, MAX 7000 and MAX 9000. Because of a rapidly growing market for large FPDs, other manufacturers developed devices in the CPLD category and there are now many choices available. CPLDs provide logic capacity up to the equivalent of about 50 typical SPLD devices, but it is somewhat difficult to extend these architectures to higher densities. To build

FPDs with very high logic capacity, a different approach is needed (Brown&Rose,2004).

The highest capacity general purpose logic chips available today are the traditional gate arrays sometimes referred to as Mask-Programmable Gate Arrays (MPGAs). MPGAs consist of an array of pre-fabricated transistors that can be customized into the user's logic circuit by connecting the transistors with custom wires. Customization is performed during chip fabrication by specifying the metal interconnect, and this means that in order for a user to employ an MPGA a large setup cost is involved and manufacturing time is long. Although MPGAs are clearly not FPDs, they are mentioned here because they motivated the design of the user-programmable equivalent: Field-Programmable Gate Arrays (FPGAs). Like MPGAs, FPGAs comprise an array of uncommitted circuit elements, called logic blocks, and interconnect resources, but FPGA configuration is performed through programming by the end user. As the only type of FPD that supports very high logic capacity, FPGAs have been responsible for a major shift in the way digital circuits are designed (Nelson, 2000).

2.3 How PLDs Retain Their Configuration

A PLD is a combination of a logic device and a memory device. The memory is used to store the pattern that was given to the chip during programming. Most of the methods for storing data in an integrated circuit have been adapted for use in PLDs.

These include:

- Silicon antifuses
- SRAM
- EPROM or EEPROM cells
- Flash memory

Silicon antifuses are the storage elements used in the PAL, the first type of PLD. These are connections that are made by applying a voltage across a modified area of silicon inside the chip. They are called antifuses because they work in the opposite

way to normal fuses, which begin life as connections until they are broken by an electric current.

SRAM, or static RAM, is a volatile type of memory, meaning that its contents are lost each time the power is switched off. SRAM-based PLDs therefore have to be programmed every time the circuit is switched on. This is usually done automatically by another part of the circuit.

An EPROM cell is a MOS (metal-oxide-semiconductor) transistor that can be switched on by trapping an electric charge permanently on its gate electrode. This is done by a PAL programmer. The charge remains for many years and can only be removed by exposing the chip to strong ultraviolet light in a device called an EPROM eraser (wiki,2012).

Flash memory is non-volatile, retaining its contents even when the power is switched off. It can be erased and reprogrammed as required. This makes it useful for PLD memory. image (Chikkali & Prabhushetty, 2011).

2.4 FPGA Overview

While PALs were busy developing into GALs and CPLDs, a separate stream of development was happening. This type of device is based on gate array technology and is called the field-programmable gate array (FPGA). The term "field-programmable" means the device is programmed by the customer, not the manufacturer.

FPGAs are digital integrated circuits (ICs) that contain configurable (programmable) blocks of logic along with configurable interconnects between these blocks. Design engineers can configure (program) such devices to perform a tremendous variety of tasks. The “field programmable” portion of the FPGA’s name refers to the fact that its programming takes place “in the field”. This may mean that FPGAs are configured in the laboratory, or it may refer to modifying the function of

a device resident in an electronic system that has already been deployed in the outside world (Maxfield, 2004).

In most larger FPGAs the configuration is volatile, and must be re-loaded into the device whenever power is applied or different functionality is required. Configuration is typically stored in a configuration PROM or EEPROM. EEPROM versions may be in-system programmable (typically via JTAG). (Gunay, 2010).

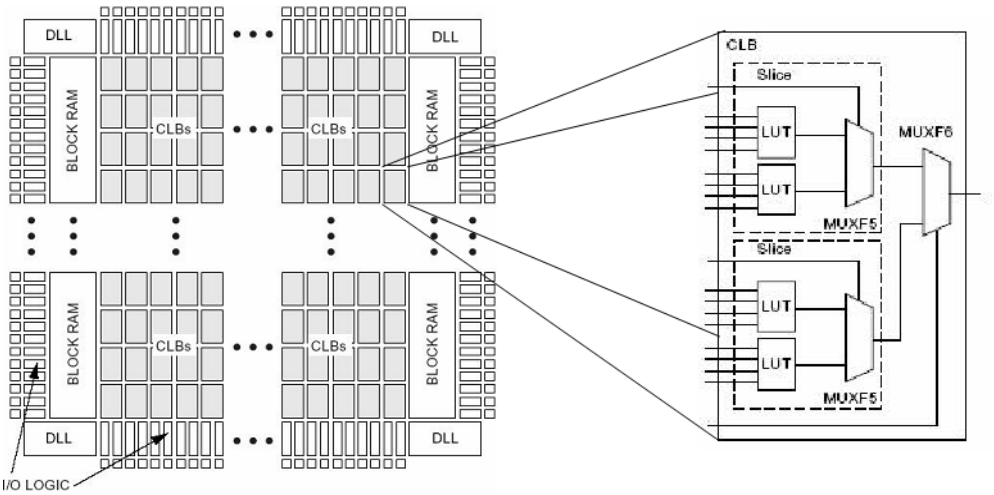


Figure 2.3 FPGA structure (Altium Designer, 2008).

In Figure 2.3 logic blocks and programmable interconnections can be seen. The function of each logic cell and interconnections are specified by hardware description languages to implement desired circuit design.

2.5 CPLD Overview

PLDs are available only in small sizes, equivalent to a few hundred logic gates. For bigger logic circuits, complex PLDs or CPLDs (Complex programmable logic device) can be used. These contain the equivalent of several PALs linked by programmable interconnections, all in one integrated circuit. CPLDs can replace thousands, or even hundreds of thousands, of logic gates. For most practical purposes, CPLDs can be thought of as multiple PLDs (plus some programmable interconnect) in a single chip. The larger size of a CPLD allows you to implement either more

logic equations or a more complicated design. In fact, these chips are large enough to replace dozens of those 7400 series parts.

CPLD manufacturers are XILINX, AMD, Altera, ICT, Lattice, Cypress, and Philips-Signetics. Each manufacturer has its architecture and property but generally, they are common at being non-volatile, reprogrammable, robust devices. (Cho, Mirzaei, Oberg, & Kastner, 2009).

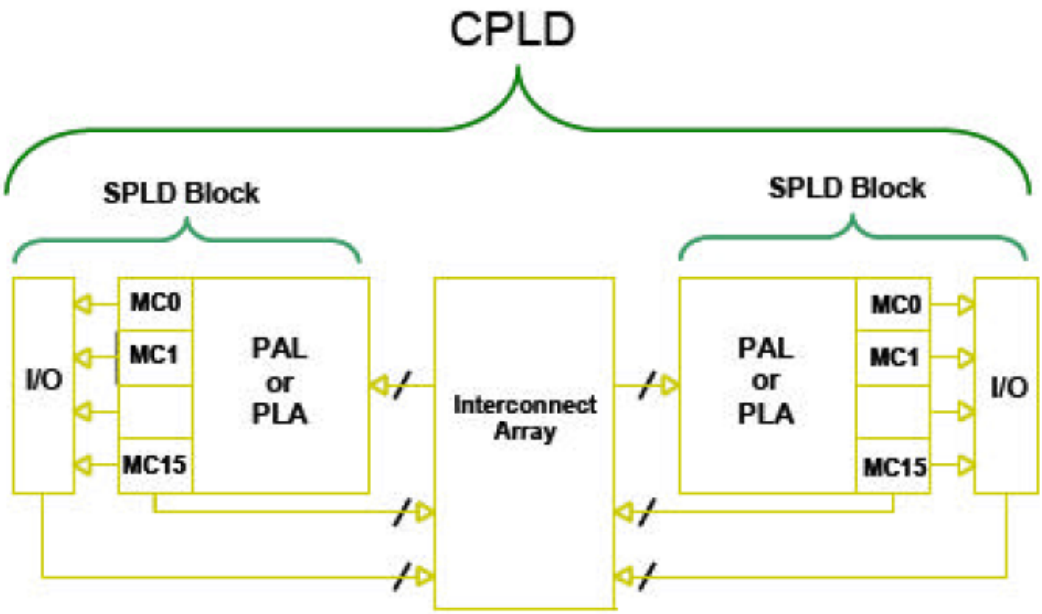


Figure 2.4 Internal structure of a CPLD (Xilinx XC4000 CLB) (Brown&Rose,2004).

2.5.1 Function Block

In Figure 2.2 contains a block diagram of a hypothetical CPLD. Each of the PAL shown there is the equivalent of one function blocks. Usually, the function blocks are designed to be similar to existing PAL architectures, so that the designer can use familiar tools or even older designs without changing them. A typical function block is shown in Figure 2.5. The AND plane still exists as shown by the crossing wires. The AND plane can accept inputs from the I/O blocks, other function blocks, or feedback from the same function block. The terms and then ORed together using a fixed number of OR gates, and terms are selected via a large multiplexer. The

outputs of the mux can then be sent straight out of the block, or through a clocked flip-flop. This particular block includes additional logic such as a selectable exclusive OR and a master reset signal, in addition to being able to program the polarity at different stages.

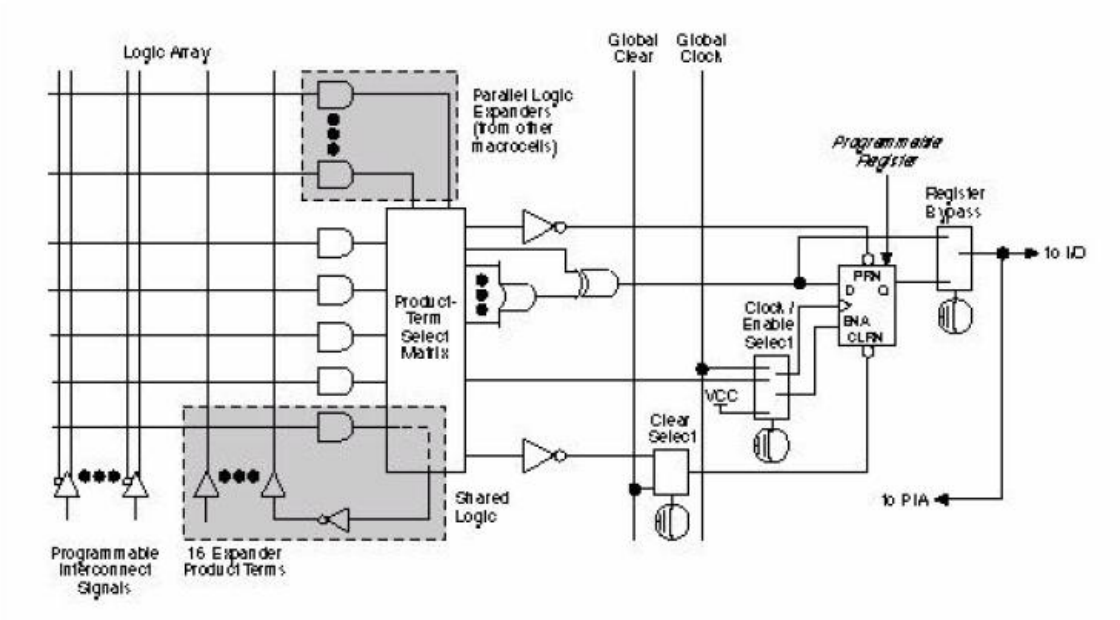


Figure 2.5 General structure of CPLD Function Block (Senouci,2008).

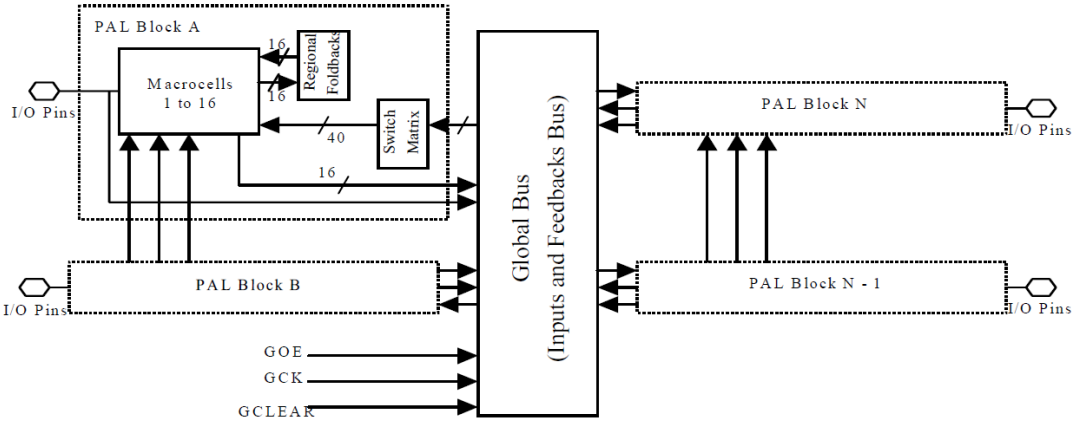


Figure 2.6 Atmel's ATF15xx family of CPLDs (Senouci,2008).

2.5.2 I/O Blocks

Figure 2.5 shows a typical I/O block of a CPLD. The I/O block is used to drive signals to the pins of the CPLD device at the appropriate voltage levels with the appropriate current. Usually, a flip-flop is included, as shown in the figure. This is done on outputs so that clocked signals can be output directly to the pins without encountering significant delay. It is done for inputs so that there is not much delay on a signal before reaching a flip-flop which would increase the device hold time requirement. Also, some small amount of logic is included in the I/O block simply to add some more resources to the device.

2.5.3 Interconnects

The CPLD interconnect is a very large programmable switch matrix that allows signals from all parts of the device go to all other parts of the device. While no switch can connect all internal function blocks to all other function blocks, there is enough flexibility to allow many combinations of connections.

2.5.4 Programmable Elements

Different manufacturers use different technologies to implement the programmable elements of a CPLD. The common technologies are Electrically Programmable Read Only Memory (EPROM), Electrically Erasable PROM (EEPROM) and Flash EPROM. These technologies are similar to, or next generation versions of, the technologies that were used for the simplest programmable devices, PROMs. As of 2005, most CPLDs are electrically programmable and erasable, and non-volatile.

2.5.5 CPLD Choosing Considerations

When considering a CPLD for use in a design, the following issues should be taken into account:

1. The programming technology-EPROM, EEPROM, or Flash EPROM? This will determine the equipment needed to program the devices and whether they came be programmed only once or many times.

2. The function block capability

-How many function blocks are there in the device?

- How many product and sum terms can be used?

-What are the minimum and maximum delays through the logic?

-What additional logic resources are there such as XNORs, ALUs,etc.?

-What kind of register controls are available (e.g., clock enable, reset, preset, polarity control)?

-How many are local inputs to the function block and how many are global, chip wide inputs?

-What kind of clock drivers are in the device and what is the worst case skew of the clock signal on the chip. This will help determine the maximum frequency at which the device can run.

3. The I/O capability

-How many I/O are independent, used for any function?

-How many are dedicated for clock input, master reset, etc.?

-What is the output drive capability in terms of voltage levels and current?

-What kind of logic is included in an I/O block that can be used to increase the functionality of the design? (Zeidman,2012).

2.5.6 Example CPLD Families

Some CPLD families from different vendors are listed; Altera MAX 7000 and MAX 9000 families, Atmel ATF and ATV families, Lattice ispLSI family, Lattice (Vantis) MACH family, Xilinx XC9** and CoolRunner family.

2.6 CPLDs versus FPGAs

The two major types of programmable logic devices are field programmable gate arrays (FPGAs) and complex programmable logic devices (CPLDs). Of the two, FPGAs offer the highest amount of logic density, the most features, and the highest performance. The largest FPGA now shipping, part of the Xilinx Virtex™ line of devices, provides eight million "system gates" (the relative density of logic). These advanced devices also offer features such as built-in hardwired processors (such as the IBM Power PC), substantial amounts of memory, clock management systems, and support for many of the latest, very fast device-to-device signaling technologies. FPGAs are used in a wide variety of applications ranging from data processing and storage, to instrumentation, telecommunications, and digital signal processing (Xilinx,2012).

CPLDs, by contrast, offer much smaller amounts of logic - up to about 10,000 gates. But CPLDs offer very predictable timing characteristics and are therefore ideal for critical control applications. CPLDs also require extremely low amounts of power and are very inexpensive, making them ideal for cost-sensitive, battery-operated, portable applications such as mobile phones and digital handheld assistants.

The difference between FPGAs and CPLDs is that FPGAs are internally based on Look-up tables (LUTs) whereas CPLDs form the logic functions with sea-of-gates (e.g. sum of products). CPLDs are meant for simpler designs while FPGAs are meant for more complex designs. In general, CPLDs are a good choice for wide combinational logic applications, whereas FPGAs are more suitable for large state machines (i.e. microprocessors).

2.7 The Advantages of Programmable Logic Devices

Fixed logic devices and PLDs both have their advantages. Fixed logic devices, for example, are often more appropriate for large volume applications because they can

be mass-produced more economically. For certain applications where the very highest performance is required, fixed logic devices may also be the best choice.

However, programmable logic devices offer a number of important advantages over fixed logic devices, including:

- PLDs offer customers much more flexibility during the design cycle because design iterations are simply a matter of changing the programming file, and the results of design changes can be seen immediately in working parts.

- PLDs do not require long lead times for prototypes or production parts - the PLDs are already on a distributor's shelf and ready for shipment.

- PLDs do not require customers to pay for large NRE costs and purchase expensive mask sets - PLD suppliers incur those costs when they design their programmable.

2.8 Software Design With Programmable Logic Devices

According to the Supplier of the PLD, user uses different programming platforms. If PLD is of Xilinx, user should use Xilinx ISE Design Suit. If PLD is of Altera, user should use Quartus or Modelsim. If PLD is of Atmel, user should use CULP. As a language user can select any of VHDL or Verilog with these platforms. Design flow is given in Figure 2.7. After code is deigned by designer on any of the language, platform compiles the code, simulates according to the selected device, and if wanted, programs the device. Hardware verification is made by the designer. If any problems are observed , design is modified and flow is redone.

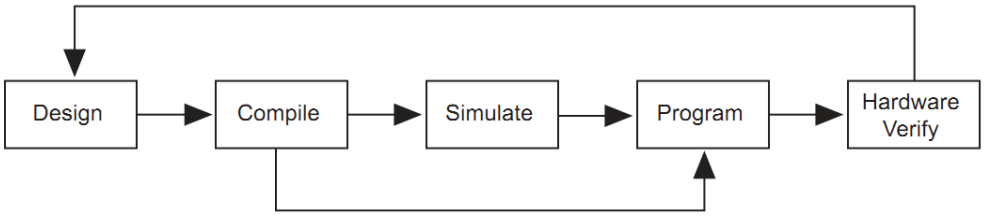


Figure 2.7 Design Flow (Altera, 2008).

Because VHDL is used through this study, there is given the structure of VHDL and it's basic properties.

2.8.1 VHDL Main Structure

A circuit or subcircuit described with VHDL code is called a design entity, or just entity. Figure 2.8 shows the general structure of an entity. It has two main parts: the entity declaration, which specifies the input and output signals for the entity, and the architecture, which gives the circuit details.

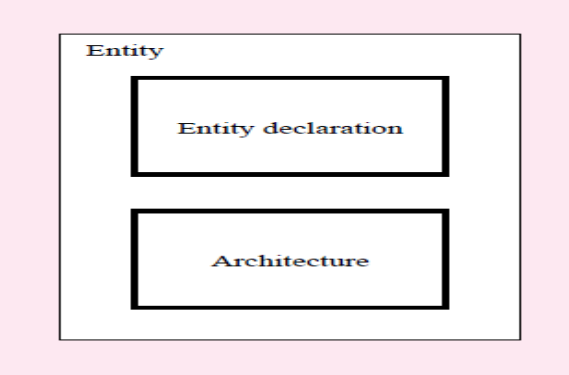


Figure 2.8 Structure of a VHDL Entity(Brown&Vranesic,1999).

ENTITY Declaration

The input and output signals in an entity are specified using the ENTITY declaration, as indicated in Figure 2.9. The name of the entity can be any legal VHDL name. The square brackets indicate an optional item. The input and output signals are specified using the keyword PORT. Whether each port is an input, output, or bidirectional signal is specified by the mode of the port. The available modes are

summarized in Table 2.1. If the mode of a port is not specified, it is assumed to have the mode IN.

Table 2.1 Possible signal modes used in ENTITY(Brown&Vranesic,1999).

The possible modes for signals that are entity ports.

Mode	Purpose
IN	Used for a signal that is an input to an entity.
OUT	Used for a signal that is an output from an entity. The value of the signal can not be used inside the entity. This means that in an assignment statement, the signal can appear only to the left of the <= operator.
INOUT	Used for a signal that is both an input to an entity and an output from the entity.
BUFFER	Used for a signal that is an output from an entity. The value of the signal can be used inside the entity, which means that in an assignment statement, the signal can appear both on the left and right sides of the <= operator.

```
ENTITY entity_name IS
    PORT ( [SIGNAL] signal_name {, signal_name} : [mode] type_name {;
           SIGNAL] signal_name {, signal_name}  : [mode] type_name } ) ;
END entity_name ;
```

Figure 2.9 ENTITY Declarations in VHDL(Brown&Vranesic,1999).

ARCHITECTURE

An architecture provides the circuit details for an entity. The general structure of an architecture is shown in Figure 2.10. It has two main parts: the declarative region and the architecture body. The declarative region appears preceding the BEGIN keyword. It can be used to declare signals, user-defined types, and constants. It can also be used to declare components and to specify attributes. The functionality of the entity is specified in the architecture body, which follows the BEGIN keyword. This specification involves statements that define the logic functions in the circuit, which can be given in a variety of ways.

```
ARCHITECTURE architecture_name OF entity_name IS
    [SIGNAL declarations]
    [CONSTANT declarations]
    [TYPE declarations]
    [COMPONENT declarations]
    [ATTRIBUTE specifications]
BEGIN
    {COMPONENT instantiation statement ;}
    {CONCURRENT ASSIGNMENT statement ;}
    {PROCESS statement ;}
    {GENERATE statement ;}
END [architecture_name] ;
```

Figure 2.10 ARCHITECTURE Declaration in VHDL(Brown&Vranesic,1999).

PACKAGE

A VHDL package serves as a repository. It is used to hold VHDL code that is of general use, like the code that defines a type, a group of ENTITY. The package can be included for use in any number of other source code files, which can then use the definitions provided in the package. Like an architecture, a package can have two main parts: the package declaration and the package body. The package_body is an optional part, which we do not use in this book; one use of a package body is to define VHDL functions, such as the conversion functions. The general form of a package declaration is depicted in Figure 2.11. Definitions provided in the package, such as the definition of a type, can be used in any source code file that includes the statements:

```
LIBRARY library_name ;
USE library_name.package_name.all.
```

The library_name represents the location in the computer file system where the package is stored. A library can either be provided as part of a CAD system, in which case it is termed a system library, or be created by the user, in which case it is called a user library.

```
PACKAGE package_name IS
    [TYPE declarations]
    [SIGNAL declarations]
    [COMPONENT declarations]
END package_name ;
```

Figure 2.11 Package declaration(Brown&Vranesic,1999).

2.8.2 Concurrent Assignment Statements

A concurrent assignment statement is used to assign a value to a signal in an architecture body. A simple signal assignment statement is used for a logic or an arithmetic expression. The general form is

```
signal_name <= expression ;
```

where " <= " is the VHDL assignment operator. The following examples illustrate its use.

```
f <= (x1 AND x2) OR x3 ;
C <= A AND B ;
```

2.8.3 Sequential Assignment Statements

The order in which the concurrent assignment statements in an architecture body appear does not affect the meaning of the code. Many types of logic circuits can be described using these statements. However, VHDL also provides another type of statements, called sequential assignment statements, for which the order of the statements in the code can affect the semantics of the code. There are three variants of the sequential assignment statements: IF statement, CASE statement, and loop statements(Brown&Vranesic,1999).

PROCESS Statement

Since the order in which the sequential statements appear in VHDL code is significant, whereas the ordering of concurrent statements is not, the sequential

statements must be separated from the concurrent statements. This is accomplished using a PROCESS statement. The PROCESS statement appears inside an architecture body, and it encloses other statements within it. The IF, CASE, and LOOP statements can appear only inside a process. The general form of a PROCESS statement is shown in Figure 2.12. Its structure is somewhat similar to an architecture. VARIABLE data objects can be declared (only) inside the process. Any variable declared can be used only by the code within the process; we say that the scope of the variable is limited to the process. To use the value of such a variable outside the process, the variable's value can be assigned to a signal.

```
[process_label:]
PROCESS [( signal name {, signal name} )]
      [VARIABLE declarations]
BEGIN
      [WAIT statement]
      [Simple Signal Assignment Statements]
      [Variable Assignment Statements]
      [IF Statements]
      [CASE Statements]
      [LOOP Statements]
END PROCESS [process_label] ;
```

Figure 2.12 General form of PROCESS statement(Brown&Vranesic,1999).

SEQUENTIAL ASSIGNMENT STATEMENTS

```
IF expression THEN
      statement ;
      {statement ;}
ELSIF expression THEN
      statement ;
      {statement ;}
ELSE
      statement ;
      {statement ;}
END IF ;
```

Figure 2.13 General form of sequential IF statement(Brown&Vranesic,1999).

```
CASE expression IS
        WHEN constant_value =>
                statement ;
                {statement ;}
        WHEN constant_value =>
                statement ;
                {statement ;}
        WHEN OTHERS =>
                statement ;
                {statement ;}
END CASE ;
```

Figure 2.14 General form of sequential CASE statement(Brown&Vranesic,1999).

2.8.4 Registers

Every signal or variable in ARCHITECTURE is infact a register. While setting a signal or variable, ENTITY instantiates multiple flip-flops which represent registers. Using the register, state machines can be realized. Through these state machines complex structures can be realized.

2.8.5 A Full-adder Example

The entity declaration specifies the input and output signals. The input port Cin is the carry-in, and the bits to be added are the input ports x and y. The output ports are the sum, s, and the carry-out, Cout. The input and output signals are called the ports of the entity. This term is adopted from the electrical jargon in which it refers to an input or output connection in an electrical circuit. The architecture defines the functionality of the full-adder using logic equations. The name of the architecture can be any legal VHDL name. There is chosen the name LogicFunc for this simple example. In terms of the general form of the architecture in Figure 2.15, a logic equation can be a type of concurrent assignment statement.

```
LIBRARY ieee ;
USE ieee.std_logic_1164.all ;

ENTITY fulladd IS
    PORT ( Cin, x, y  : IN   STD_LOGIC ;
           s, Cout    : OUT  STD_LOGIC ) ;
END fulladd ;

ARCHITECTURE LogicFunc OF fulladd IS
BEGIN
    s <= x XOR y XOR Cin ;
    Cout <= (x AND y) OR (x AND Cin) OR (y AND Cin) ;
END LogicFunc ;
```

Figure 2.15 An example VHD Code of A full-adder(Brown&Vranesic,1999).

CHAPTER THREE
POWER SUPPLY OVERVIEW

3.1 What is Power Supply

All electrical components need a supply voltage to realize it's task. A physical impact on a conductor or semiconductor occurs, electrons move, accumulate or radiate. These phonemons occur only if there is an electrical potential. In order to realize this potential, a voltage should be applied across the component. Level of this voltage varies according to the component and the structure. In an electronic device, there can be many different voltage levels. But commonly in a device there is just one main supply, a battery, or a socket from another device or supply mains. So other voltage levels inside a device should be produced from this main supply level. These supply level transitions are made by power supplies. Power supplies mainly realize this voltage conversion and filtering of the output. Filtering is important for electrical systems, in order to eliminate the ripple and transients.

There are two broad categories of power supplies: Linear regulated power supply and switched mode power supply (SMPS). In some cases one may use a combination of switched mode and linear power supplies to gain some desired advantages of both the types.

3.2 Linear Regulated Power Supply

Fig. 3.1 shows the basic block for a linear power supply operating from an unregulated dc input. The unregulated capacitor voltage becomes the input to the linear type power supply circuit. The filter capacitor size is chosen to optimize the overall cost and volume. However, unless the capacitor is sufficiently large the capacitor voltage may have unacceptably large ripple (Kharagpur, 2010).

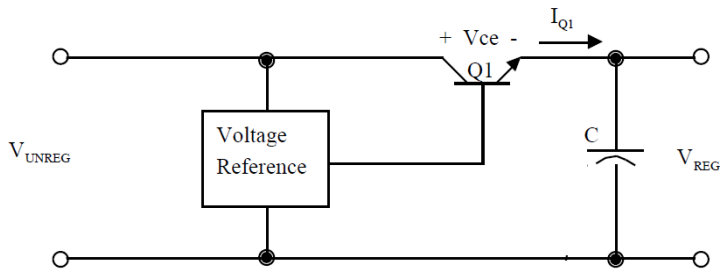


Figure 3.1 Schematic linear voltage regulators (Counsil,2000).

Power Dissipation Calculation Model:

PQ1=Vce x IQ1, for example, if Vunreg is 18V and Vreg is 14V and load is 1A, consumption over the Q1 is 4 WATTs, which is quite big.

Advantage of the linear regulated power supply is that it is simple in design, and easy to repair. This is a reliable design due to its simplicity and small number of parts. Disadvantage is that the unregulated voltage must not be very much higher than the regulated output voltage, or the power dissipation in the pass transistor becomes unacceptably large.

3.3 Switched Mode Power Supply (SMPS)

Like a linear power supply, the switched mode power supply too converts the available unregulated ac or dc input voltage to a regulated dc output voltage. The ‘Switched Mode Power Supply’ owes its name to the dc-to-dc switching converter for conversion from unregulated dc input voltage to regulated dc output voltage. The switch employed is turned ‘ON’ and ‘OFF’ (referred as switching) at a high frequency. During ‘ON’ mode the switch is in saturation mode with negligible voltage drop across the collector and emitter terminals of the switch where as in ‘OFF’ mode the switch is in cut-off mode with negligible current through the collector and emitter terminals. On the contrary the voltage-regulating switch, in a linear regulator circuit, always remains in the active region.

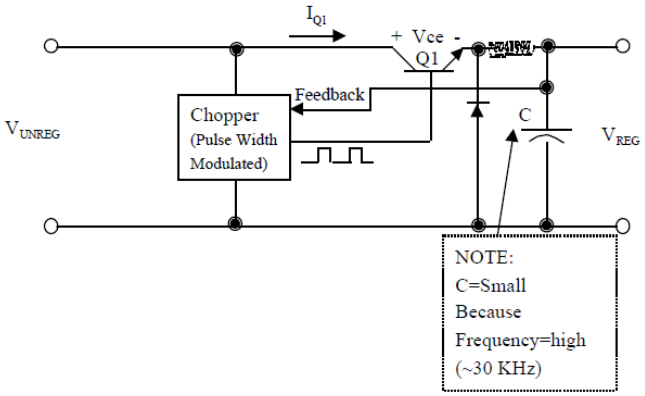


Figure 3.2 Schematic linear voltage regulators (Counsil,2000).

Power Dissipation Calculation Model:

PQ1=Vce x IQ1avarage, for example, if Vunreg is 18V and Vreg is 14V , Vce is 0.5V and load is 1A, consumption over the Q1 is 0.5V WATTs, which is quite big. Advantages are, runs cooler, it is lighter due to no need for large transformers or inductors, the unregulated voltage can be much higher than the regulated output voltage and the power dissipation remains low. This design will operate over a very wide input voltage range.

A disadvantage of the switch-mode power supply is that due to the chopper circuit, it might generate some RFI. This can be overcome by fully enclosing it in a grounded case, and with good input and output RF filtering. Another disadvantage is that this design has a larger number of parts, thus making it more complex to diagnose and repair problems, as well as having a lower reliability (Counsil,2000).

3.4 Power Supply Specifications

Power supplies may have several specifications to be met, including their voltage and current ratings. One needs to specify the tolerable limits on the ripple voltages, short-circuit protection level of current (if any) and the nature of output volt-current curve during over-current or short circuit (the output voltage magnitude should

reduce or fold back towards zero, gradually, depending on the severity of over-current). The fuse requirement (if any) on the input and the output side may need to be specified. One needs to specify the type of input supply (whether ac or dc) or whether the power supply can work both from ac or dc input voltages. Acceptable range of variation in input voltage magnitude, supply frequency (in case of ac input) are also to be specified. Efficiency, weight and volume are some other important specifications. Some applications require the electro-magnetic compatibility standards to be met. By electromagnetic compatibility it is meant that the level of EMI generation by power supply should be within tolerable limits and at the same time the power supply should have the ability to work satisfactorily in a limited noisy environment. It is quite common to have output voltage isolation and it is specified in terms of isolation breakdown voltage. In case of multiple power supplies it needs to be specified what should be the acceptable ripple voltage range for each and isolation requirements.

3.5 Some Common Types of SMPS Circuits

There are several different topologies for the switched mode power supply circuits. Some popular ones are: flyback, forward, push-pull, C'uk, Sepic, half bridge and full bridge circuits. A particular topology may be more suitable than others on the basis of one or more performance criterions like cost, efficiency, overall weight and size, output power, output regulation, voltage ripple, etc. Figure 3.3 summarizes the common SMPS topologies.

3.6 Topology Selection Considerations

There is no single topology, which is best for all applications. The right switching power supply topology for a given application should be selected based on specific requirements for the power supply design including cost, size, time factors, intention and mechanical considerations. For example, for low-volume designs, the engineering expenses may be more important than BOM cost. In this case, you may want to choose a straightforward "textbook-based" approach in which you are most

experienced. For a high-volume production, you'll want to put extra engineering efforts in developing new solutions, minimizing component cost and assembly labor.

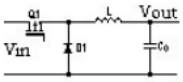
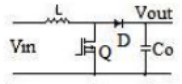
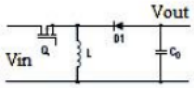
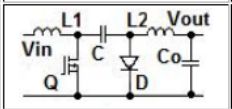
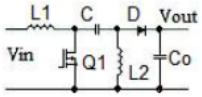
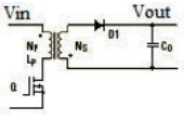
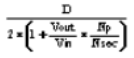
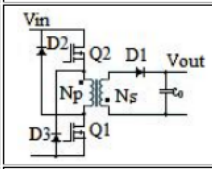
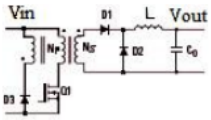
Converter topology	Diagram	DC transfer function (Vout/Vin)	Max switch voltage	Peak switch current	Max rectifier voltage	Average rectifier current	Switch utilization ratio (SUR)
NON-ISOLATING DC-DC CONVERTERS							
Buck		D (0<D<1)	Vin	Iout	Vin	Iout×D	Vout/Vin
Boost		1/(1-D) (0<D<1)	Vout	Iout×Vout /Vin	Vout	Iout	Vin/Vout
Flyback (inverting) or buck-boost		-D/(1-D) (0<D<1)	Vin+|Vout|	Iout× (1+|Vout|/Vin)	Vin+|Vout|	Iout	|Vout|/Vin
Ćuk		-D/(1-D) (0<D<1)	Vin+|Vout|	Iout× (1+|Vout|/Vin)	Vin+|Vout|	Iout	|Vout|/Vin
Sepic		D/(1-D) (0<D<1)	Vin+Vout	Iout	Vin+Vout	Iout	Vout/ (Vin+Vout)
ISOLATING DC-DC CONVERTERS							
Flyback		√(2Pout× LpF/Vin) (0<D<1)	Vin+Vout ×(Np/Ns)	D×Vin/Lp×F	Vout+ (Vin×Ns/Np)	Iout	
2-switch flyback		√(2Pout× LpF/Vin) (0<D<0.5)	Vin	D×Vin/Lp×F	Vout+ (Vin×Ns/Np)	Iout	D/4
Forward		Ns/Np×D (0<D<0.5)	2×Vin	Iout×Ns/Np	Vin×Ns/Np	D1: Iout×D D2: Iout(1-D)	Vout/2Vin ×Ns/Np

Figure 3.3 Main single-stage switching regulator circuits (Rozenblat,2012).

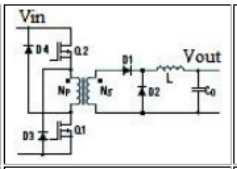
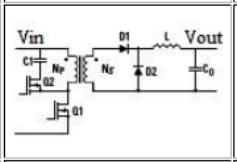
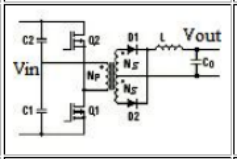
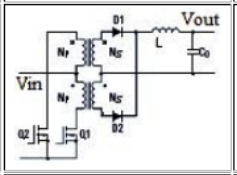
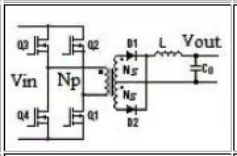
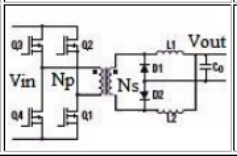
2-switch forward		Ns/Np×D (0<D<0.5)	Vin	Iout×Ns/Np	Vin×Ns/Np	D1: Iout×D D2: Iout(1-D)	Vout/2Vin ×Ns/Np
Active clamp forward		Ns/Np×D (0<D<1)	Vin/(1-D)	Iout×Ns/Np	Vin×Ns/Np	D1: Iout×D D2: Iout(1-D)	Vout/Vin× (1-Vout×Np/ Vin×Ns)
Half-bridge		Ns/Np×D (0<D<0.5)	Vin	Iout×Ns/Np	Vin×Ns/Np	0.5×Iout	Vout/2Vin ×Ns/Np
Push-pull		2Ns/Np×D (D<0.5)	2×Vin	Iout×Ns/Np	2Vin×Ns/Np	0.5×Iout	Vout/4Vin ×Ns/Np
Full bridge		2Ns/Np×D (0<D<0.5)	Vin	Iout×Ns/Np	2Vin×Ns/Np	0.5×Iout	Vout/2Vin ×Ns/Np
Phase shifted full bridge		2Ns/Np×D (0<D<0.5)	Vin	Iout×Ns/Np	Vin×Ns/Np	0.5×Iout	Vout/2Vin ×Ns/Np

Figure 3.3 (continued) Main single-stage switching regulator circuits (Rozenblat,2012).

Notes:

1. All formulas are given for ideal circuits. Ripple currents, voltage spikes, diodes voltage drop and power losses are excluded.
2. Flyback equations are given for discontinuous mode of operation.
3. SUR is total switch utilization ratio defined as SUR=Pout/n×Vmax×Imax, where n- the number of power switches in the circuit, Vmax and Imax- their peak voltage and current.

When the functional requirements are pretty much conventional, the power level is usually the main factor that determines the topology. As an illustration, the Table 3.1 shows the topologies in an offline switching power circuit depending on its output power level. This selector guide is given for the power sources with output voltages below 60V running off 120 to 400V DC-link (which is typical for rectified AC input line voltage or the output of a PFC boost) This selector guide is given mostly considering efficiency and switching elements' stresses (Rozenblat,2012).

Table 3.1 Main single-stage switching regulator circuits (Rozenblat,2012).

	0-100 W, Iout<5 A	0-100 W, Iout>5 A	200-400 W	400-1200 W	1200-3000 W
Single switch flyback	✓	-	-	-	-
2-switch flyback	✓	-	-	-	-
Single switch forward	✓	✓	-	-	-
2-switch forward	✓	✓	✓	-	-
Half bridge	-	-	✓	✓	-
Full bridge	-	-	-	✓	-
ZVT full bridge	-	-	-	✓	✓

3.7 Flyback Topology Overview

Flyback topology is the most common SMPS structure. It can be generally used from 0 Watts to 100 Watts. In fact there is not any power limit due to topology, if you find the right components, namely, mosfets, diodes and the transformer, you can get any output power. It can be used directly from passively rectified systems from mains. Considering BOM cost, it is the cheapest among other isolated topologies. Transformer structure of Flyback systems is easier. Flyback systems are relatively more tolerable to transformer tolerances. Closed loop control is easier, there is a big magnetic compensation on control loop, there does not happen fast transients.

The flyback converter is based on the buck-boost converter. It's derivation is illustrated in Figure 3.4. Figure 3.4 (a) depicts the basic buck-boost converter, with the switch realized using a mosfet and diode. In Figure 3.4(b), the inductor winding is constructed using two wires, with a 1:1 turns ratio. The basic function of the inductor is unchanged, and the parallel windings are equivalent to a single winding constructed of larger wire. In Figure 3.4(c), the connections between the two windings are broken. One winding is used while the transistor Q1 conducts, while the other winding is used when diode D1 conducts. The total current in the two windings is unchanged from the circuit of Figure 3.4(b); however, the current is now distributed between the windings differently. The magnetic fields inside the inductor in both cases are identical. Unlike the ideal transformer, current does not flow

simultaneously in both windings of the flyback transformer. Figure 3.4(d) illustrates the usual configuration of the flyback converter. The switching element, mosfet source is connected to the primary-side ground, simplifying the gate drive circuit. The transformer polarity marks are reversed, to obtain a positive output voltage. A 1:n turns ratio is introduced to attain desired output voltage (Erickson&Maksimovic,2001).

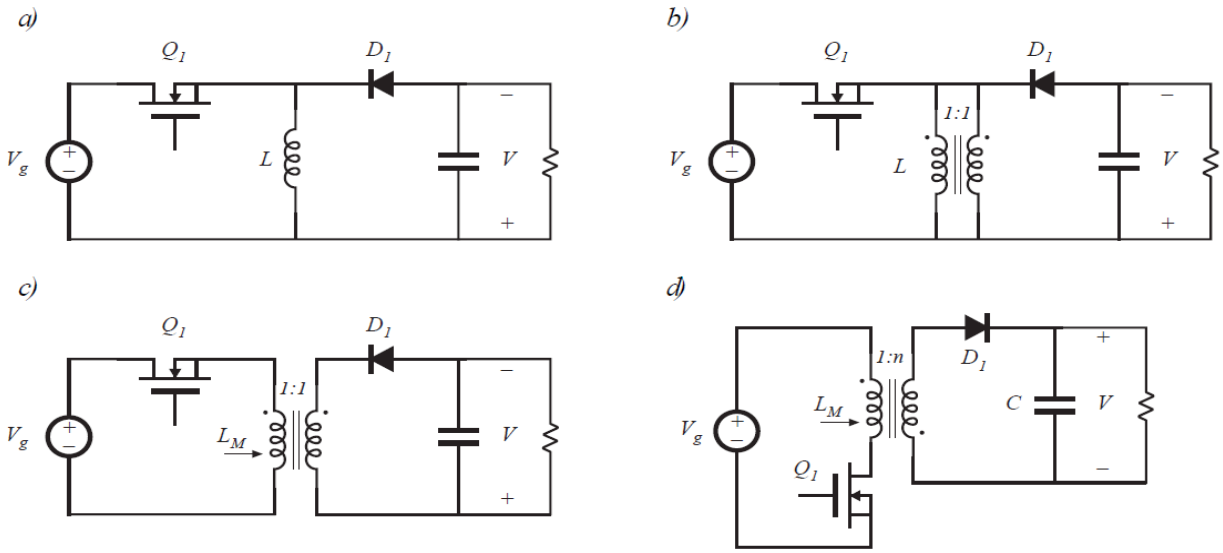


Figure 3.4 Derivation of the flyback converter: (a) buck-boost converter, (b) inductor L is wound with two parallel wires, (c) inductor windings are isolated, leading to the flyback converter, (d) with a 1:n turns ratio and positive output (Colorado,2012).

3.7.1 Analysis of the Flyback Topology

The behavior of most transformer-isolated converters can be adequately understood by modeling the physical transformer with a simple equivalent circuit consisting of an ideal transformer in parallel with the magnetizing inductance. The magnetizing inductance must then follow all of the usual rules for inductors. In particular, volt-second balance must hold when the circuit operates in steady-state. This implies that the average voltage applied across every winding of the transformer must be zero. If we replace the transformer of Figure 3.4(d) with the equivalent circuit, the circuit of Figure 3.5(a) is then obtained. The magnetizing inductance LM functions in the same manner as inductor L of the original buck-boost converter of

Figure 3.4(a). When transistor Q1 conducts, energy from the dc source Vg is stored in LM. When diode D1 conducts, this stored energy is transferred to the load, with the inductor voltage and current scaled according to the 1:n turns ratio.

During subinterval 1, while transistor Q1 conducts, the converter circuit model reduces to Figure 3.5(b). With small ripple approximation, the inductor voltage vL, capacitor current iC, and dc source current ig, are given by

VL = Vg

iC = – v/R

ig = I

Equation 3.1

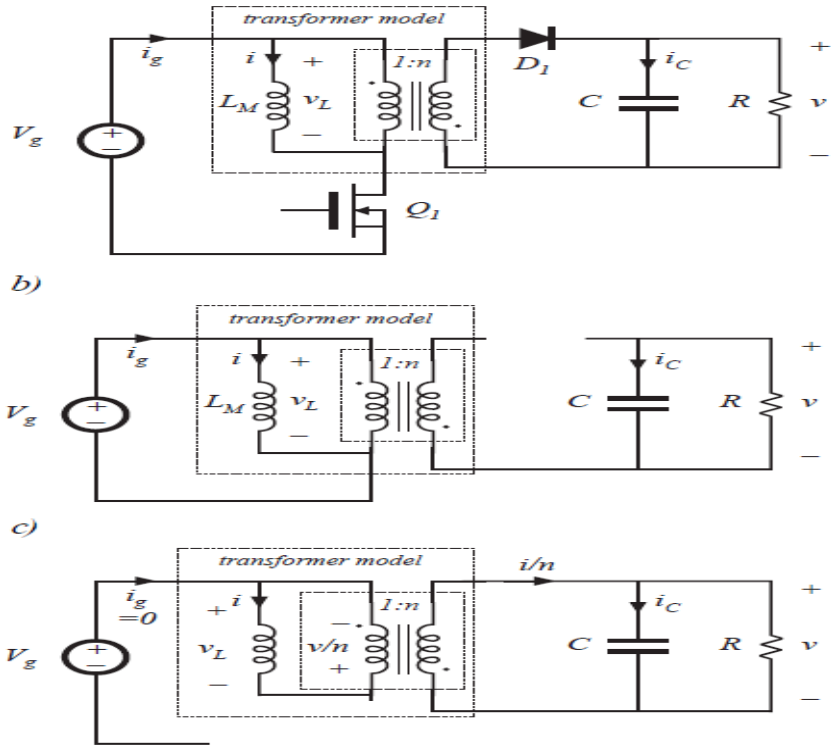


Figure 3.5 Flyback converter circuit, (a) with transformer equivalent circuit model, (b) during subinterval 1, (c) during subinterval 2 (Colorado,2012).

During the second subinterval, the transistor is in the off-state, and the diode conducts. The equivalent circuit of Figure 3.5(c) is obtained. The primary-side magnetizing inductance voltage vL, the capacitor current iC, and the dc source current ig, for this subinterval, with small ripple approximation, are:

vL= – V/n

iC = I/n–V/R

ig = 0

Equation 3.2

The vL(t), iC(t), and ig(t) waveforms are sketched in Figure 3.6.

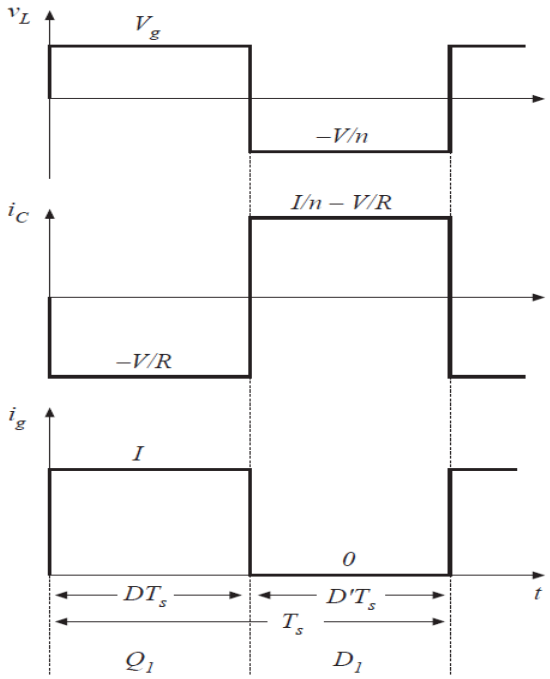


Figure 3.6 Flyback converter waveforms, continuous conduction mode (Colorado,2012).

Application of the principle of volt-second balance to the primary-side magnetizing inductance yields;

<vL> = D x (Vg) + D' x (– V/n) = 0

Equation 3.3

Solution then leads to;

V/Vg= n x (D/D')=> V=n x Vg x (D / (1 – D))

Equation 3.4

Application of the principle of charge balance to the output capacitor C leads to;

<iC>= D x (– V/R) + D' x (I/n – V/R) = 0

Equation 3.5

Solution for I yields;

$$I = (n \times V) / (D' \times R)$$

Equation 3.6

D is Duty Cycle. D’ is 1 – D. These calculations are made for small signal analysis of the circuit, but equations differ according to magnetic alignment of the transformer material. Alignment is the physical direction of the molecules of core material. Alignment of the material determines the B-H curve and mode of operation determines the path of alignment over B-H curve. For Continuous Conduction Mode, alignment occurs just upper right side of B-H curve and material never aligns to zero point. But in Critical Conduction Mode and Discontinuous Conduction Mode alignment passes and stays at the zero point of B-H curve. B-H curve is given in Figure 3.7 for a representation. Here it is beneficial to mention about modes of operation.

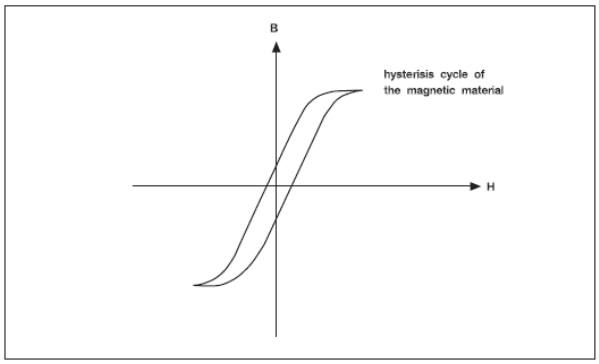


Figure 3.7 B-H curve (Wuidart, 1999).

3.7.2 Modes of Operation of Flyback Topology

Continuous Conduction Mode (CCM)

In CCM, the magnetizing inductance of the transformer stsrts from a nonzero current condition when the switch turns on and requires cycle-to-cycle energy storage in the transformer. CCM flyback circuits are typically implemented in fixed frequency applications. The secondary current also does not return to zero, hence requires transformer store the energy across the cycles. Amount of this stored energy

differs with the power level. CCM switching elements waveforms are given in Figure 3.8.

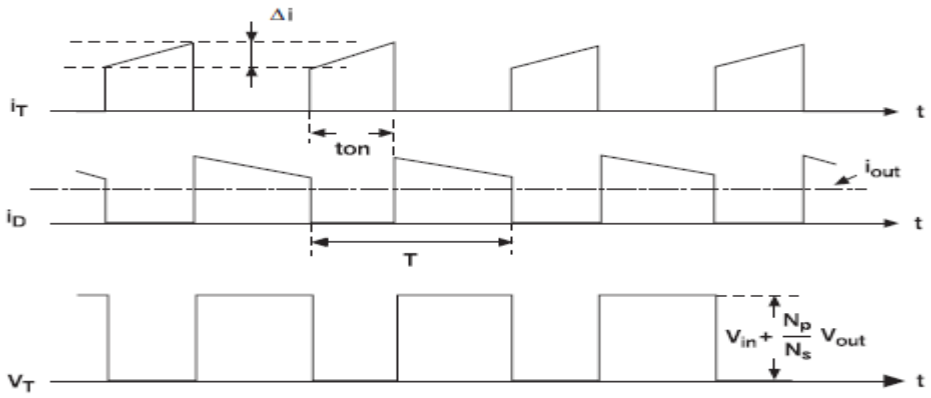


Figure 3.8 CCM operation (Wuidart, 1999).

Steady state equations of CCM are given below.

$$\text{Duty Cycle} = \frac{Vout + Vd}{Vin \bullet N + Vout + Vd} \approx \frac{Vout}{Vin \bullet N + Vout}$$

$$\text{Switch peak current and turn on current} = \frac{Iout \cdot N}{1 - D} + \frac{Vin \cdot D}{2 \cdot Lpri \cdot f}$$

$$\text{Diode turn on and off currents} = \frac{IswPk}{N}$$

Equation 3.7

Where D is duty cycle, Vin is input voltage, N is transformer turns ratio, Vout is output voltage, f is frequency of operation, Vd is diode forward voltage, Lpri is transformer primary inductance, Iout is output current load and IswPk is switch peak current. Considering switching element stresses for system design below equations are beneficial to choose the right components. ICpeak is mosfet's peak current, IDrms is mosfet's RMS current, IFpeak is diode's peak current, IF(AV) is the diodes RMS current, Poutmax is the maximum available output power desired, Vinmin is the minimum input rail voltage of the transformer, A is output diode on time duty cycle, VDDS is switching element, mosfet's, Drain to Source voltage and VRRM is secondary diodes reverse breakdown voltage.

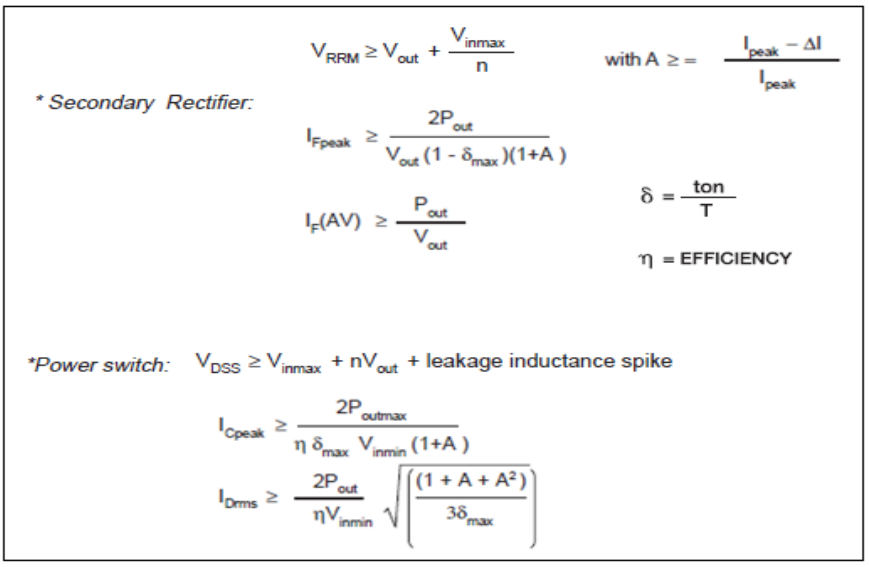


Figure 3.9 CCM operation equations (Wuidart, 1999).

Advantages and disadvantages of CCM

ADVANTAGES	DISADVANTAGES
- Peak current of rectifier and switch is half the value of discontinuous mode	- Recovery time rectifier losses
- Low output ripple: C_{out} (cont.) = 0.5 C_{out} (disc.)	-Feedback loop difficult to stabilize (2 poles and right half plane zero)

Figure 3.10 Advantages and disadvantages of CCM (Wuidart, 1999).

Right Half Plan (RHP) Zero

Gain function of CCM involves two zeros that causes cut offs on the bandwith, decreases the available working frequency gap. With upward step load, secondary current is supposed to increase, but Vo will drop temporarily, duty cycle will increase in response, secondary current pulse will be cut short and secondary current is reduced, instead. System controller will eventually catch up the referance, but momentarily the response walks in the opposite direction. This is in conflict with what is desired, and is represented as a RHP zero. The Right Half Plan (RHP) zero

complicates the loop compensation. When the load decreases, the RHP Zero moves toward the higher frequency range. When the duty cycle decreases, i.e. the input voltage increases, the RHP Zero moves to a higher frequency. Therefore, the worst case to consider is the maximum power at the minimum input voltage. An extremely large inductance results in a lower RHP Zero (National Semiconductor, 2010).

Boundary Conduction Mode (BCM)

The name boundary conduction mode comes from the fact that the controller operates right on the boundary between CCM and DCM. It is in fact a subset of DCM. The switch turns on and stores just enough charge to replenish the load during the time the switch opens. Thus the switch turns on again as soon as all the energy is transferred to the output. The controller ensures that there is very little time when the transformer has no energy stored as flux, known as dead time. Typical waveforms on osciloscope are given in Figure 3.11.

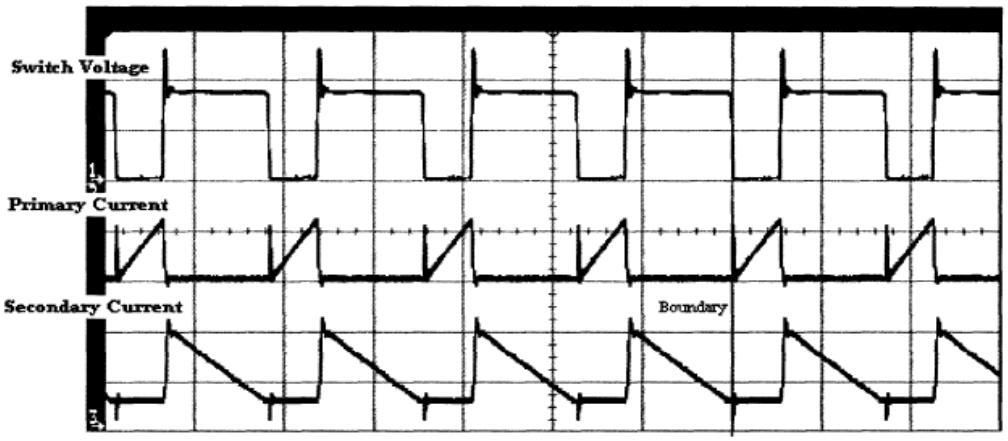


Figure 3.11 An oscilloscope print out of Switchind elements waveforms in BCM (Kenia, 2004).

The point where the switch is turned on and current begins to ramp in primary occurs as soon as the current returns to zero in secondary. Depending on the load and the input voltage, the primary current must reach a different level to ensure output regulation. Since switching occurs after all the energy is transferred, the operating frequency is dependent on line and load conditions. For wide load requirements this

mode is not appropriate because it should work at very higher frequencies in light load and it should work at very low frequencies at heavy load.

Steady state Equations are:

$$\text{Duty Cycle} = \frac{Vout + Vd}{Vin \cdot N + Vout + Vd} \approx \frac{Vout}{Vin \cdot N + Vout}$$

$$\text{Frequency} = \frac{D \cdot Vin \cdot (1 - D)}{2 \cdot Iout \cdot N \cdot Lpri}$$

$$\text{Switch peak current} = \frac{2 \cdot Iout \cdot N}{1 - D}$$

Equation 3.8

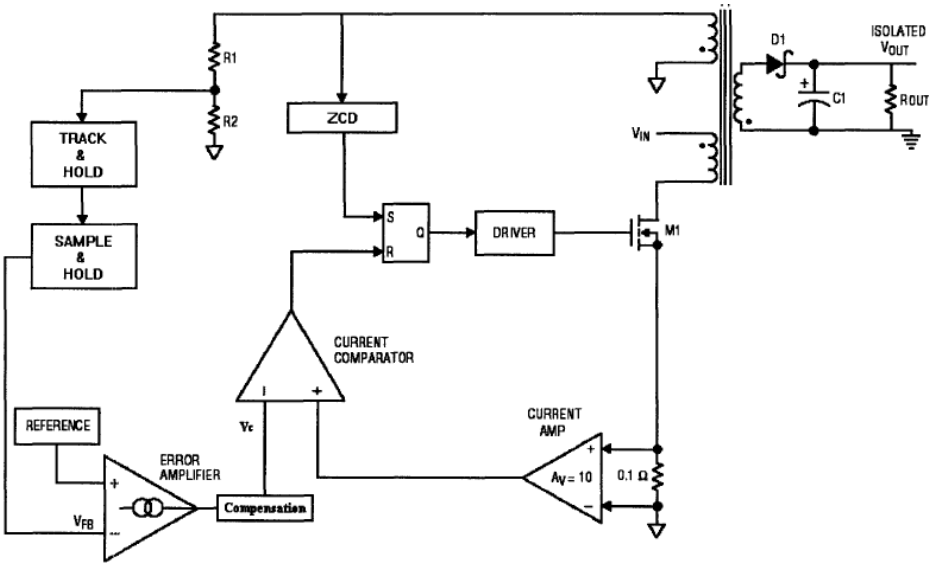


Figure 3.12 A typical magnetic-flux sensing (output voltage is sensed from primary auxiliary winding) flyback solution using BCM operation. (Kenia, 2004).

Discontinuous Conduction Mode (DCM)

In DCM stored transformer energy and current start and return to zero in each cycle. The transformer never has to store energy across the cycles. The energy stored in the primary when switch turns on is completely transferred to the output through the secondary after the switch opens. The time when the switch open and energy is not transferred to the load is known as dead time. In dead time there occurs an oscillation between the leakage inductance of the transformer and input and stray capacitances.

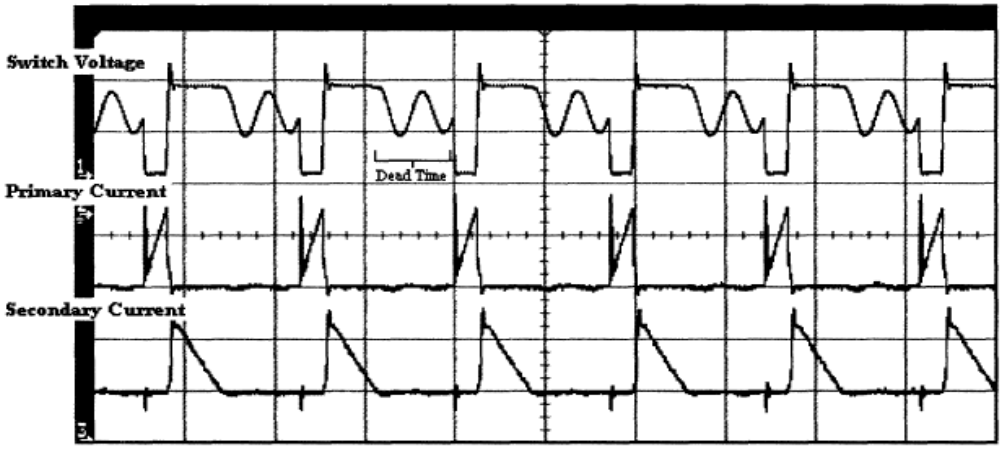


Figure 3.13 An oscilloscope print out of switching elements' waveforms in DCM (Kenia, 2004).

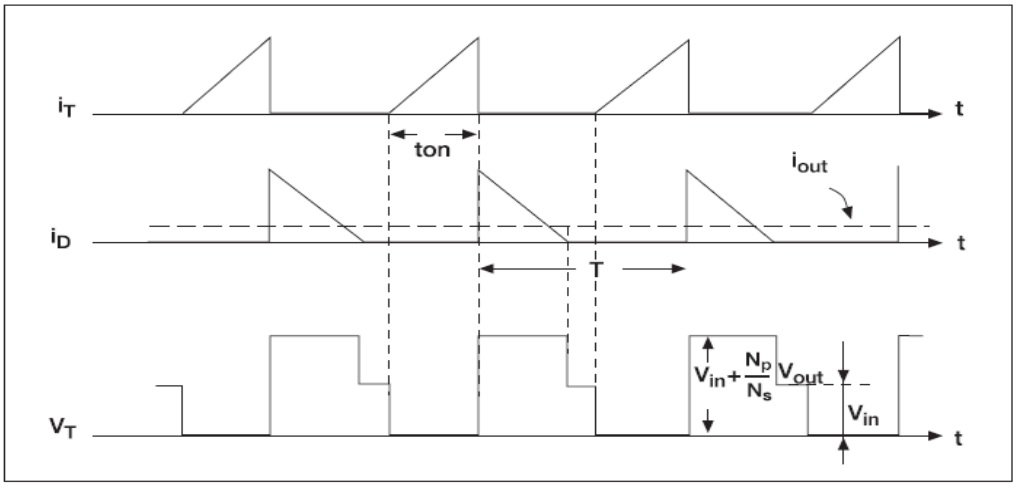


Figure 3.14 Typical Waveforms for DCM operation.(ST electronics, 1999).

DCM mode can be implemented in a variety of ways. Controller can operate with a fixed frequency of operation, or fixed on times of operation, or quassi-mode of operation. DCM mode shares the same steady state equations with BCM. Considering switching component stresses for system design, below equations can be beneficial for DCM.

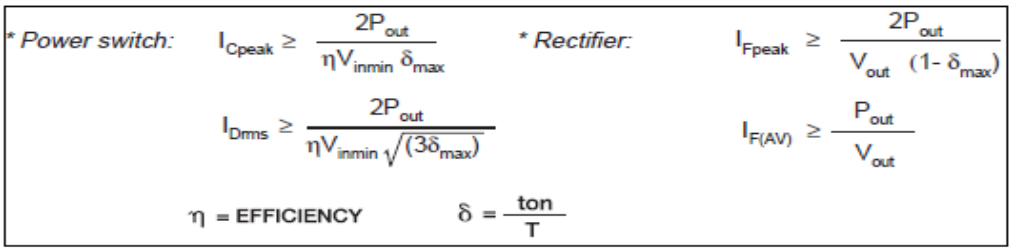


Figure 3.15 DCM and BCM equations (ST electronics, 1999).

Advantages and disadvantages of DCM and BCM

ADVANTAGES	DISADVANTAGES
- Zero turn-on losses for the power switch	- High peak currents in rectifiers and power switches
- Good transient line/load response	- Large output ripple: C_{out} (disc.) $\approx 2 \cdot C_{out}$ (cont.)
- Feedback loop (single pole) easy to stabilize	
- Recovery time rectifier not critical: current is zero well before reverse voltage is applied	

Figure 3.16 Advantages and disadvantages of DCM and BCM (ST electronics, 1999).

All these methods have their drawbacks and gainings. Though BCM and DCM exhibit higher conduction losses at transformer windings and switching elements forward resistances because of higher peak and RMS current levels, CCM exhibits higher switching loss because the switchings are made while there is still current over the switching elements, and also because CCM systems preferably operates at higher frequencies. Considering copper loss at the transformer, CCM has an advantage because of smaller flux swing in B-H curve. On the other hand, considering EMI performance, DCM, especially quassi-resonant mode, has an advantage because of smooth turns on and offs of switching elements. Considering short circuit protection and loop response, BCM and DCM are also better because there is smaller energy on secondary diode and voltage over the diode diminishes

easily if a short occurs. CCM designs continues to operate unless the switching elements break if there is not a fast protection, in a short situation. A higher inductance is needed to keep operation in continuous conduction mode over a wider load range. With higher inductance, the ripple currents in both the primary and secondary circuit will be lower. In order to realize a higher inductance, number of turns increase which increases the size and resistance of the windings. So by choosing CCM while one decreases the RMS currents of the transformer, it increases the resistance of the windings. Choosing the right mode depends on the designer and the situation. Design of transformer is important to choose mode, but mode is definitely depends on the controller. Some controllers can run in all modes, but generally their control loop is constructed according to one of the mode and one should design the transformer according to the mode of intention, if you want to work with that controller at a specific input, load and filter condition. The device proposed by this thesis can cover all modes, it clearly finds the proper working point for a transformer at a specific input, load and filter condition.

3.7.3 Advantages and Disadvantages of the Flyback Topology

Advantages are voltage step-down or step-up can be applied just by duty cycle and turns ratio, multiple outputs are easy to implement, it does not need a separate output inductor as in forward topology. Flyback converters use the simplest isolated topology, and thus have the lowest cost. Flyback converters provide better cross regulation for slave rails, including bias Vcc rail than other topologies. Disadvantages are high output ripple current, high input ripple current, loop bandwidth may be limited by the Right Half Plan (RHP) Zero. Another disadvantage of the flyback converters is the need for snubber to prevent voltage spikes over the switching element.

No transformer is perfectly ideal. There are always magnetic field lines generated by the primary windings that are not enclosed by the secondary windings. This cause leakage inductance usually modeled as a small inductor in series with the primary winding of the transformer. The energy that is stored in the transformer is dumped in

the buffer capacitor, but this does not include the small amount of energy stored as stray inductance. The opening and closing of the switch causes sharp voltage peak just as any inductor that is disconnected from a DC current. The small stray inductor connected in series with the source drain capacitance will cause a dampened high frequency oscillation. To prevent this from occurring, the switching transistor can be protected by passive clamps as RC snubber network, a zener diode, resonant structures or by an active clamp. They, all, are used to limit the maximum source-drain voltage.

Typically, the voltage spike due to transformer's leakage inductance is limited by clamp circuits. Its action is to limit the voltage spike so it never exceeds the voltage rating of the switching element. This will optimize energy transfer from primary to secondary. A low leakage inductance of the transformer is, of course, extremely helpful. RCD clamps in Figure 3.18(a) dissipate power even under no-load conditions. There is always the reflected voltage across the clamp resistor (R). To reduce clamp losses to a negligible level at light load, the use of a zener clamp as in Figure 3.17(b) is recommended whenever possible. Such a circuit gives also a well defined clamping level but, on the other hand, dissipates more power at full load. Its use is therefore limited to low power applications. An alternative to these solutions can be the use of a non-dissipative clamp like the LCD one shown in Figure 3.18 (c), which helps also reduce turn-off losses in the mosfet. This circuit recovers the majority of the leakage inductance energy by transferring it back onto the input voltage rail through C and D2. There is just a little power dissipation on the two diodes and the inductor. However, there is a slight increase of the conduction losses in the mosfet at heavy load and, besides, the circuit is quite expensive and not easy to optimize (Adragna, 1998).

Beside these passive clamp solutions, there is active clamp method. In active clamp there is another switch as a clamp, which is opened when the main switch closes. So the leakage energy is transmitted to input suplly over this clamp switch. This method is also called as two-switch flyback. Two-switch flyback has superior performance with CCM operation combined with zero voltage switching. Zero

voltage switching is the method that mosfets are switched while the reverse diodes of the mosfets are transmitting some current. Zero voltage switching occurs if primary side leakage inductance resonates with the primary side total capacitance. By this method, primary side switching component losses are very low, EMI performance is better and transformer design becomes easier.

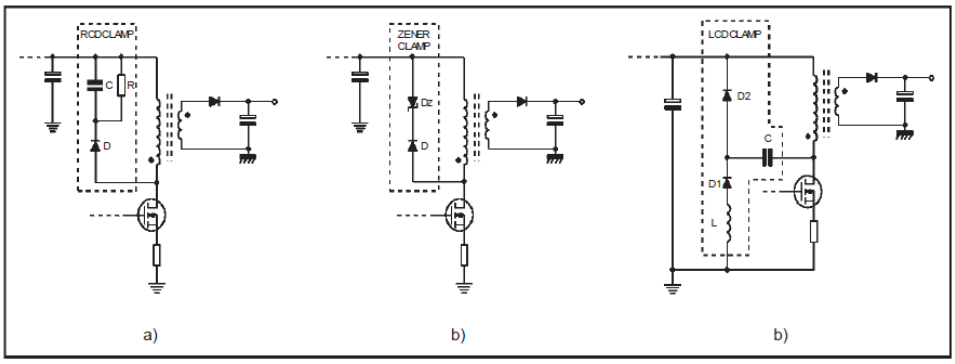


Figure 3.17 Some passive clamp circuit topologies. a)RCD Clamp b) Zener Clamp c)LCD Clamp (Adragna, 1998).

3.7.4 System Design Considerations of the Flyback Topology

Before starting a SMPS system with, one should first state the input voltage level, output voltage level, output power level desired and desired operation method. Design starts with the calculation of transformer according to desired operation mode, working frequency and duty cycle, desired efficiency and available switching components. Switching components determine the maximum allowable drain source voltage at primary side mosfet. From this maximum allowable duty cycle (δmax) is found. Vflbk is of time rectified voltage over primary winding.

$$\delta_{max} = \frac{V_{flbk}}{V_{flbk} + V_{in(min)}}$$

Equation 3.9

Secondary side rectifier diodes reverse breakdown voltage generally is not a concern because output voltage swing is generally small. Knowing maximum output power (Pout) and minimum input voltage (Vin(min)) and efficiency (η), average primary side current Iin-av is found as below.

$$I_{in-av(max)} = \frac{P_{out}}{\eta \cdot V_{in(min)}}$$

Equation 3.10

The maximum input primary peak current is then found by

$$I_{ppk} = \frac{2 \cdot I_{in-av(max)}}{\delta_{max}}$$

Equation 3.11

After determining maximum primary side current, one should determine, primary side inductance according to below equitation. Fmin is the minimum allowed working frequency.

$$L_p = \frac{\delta_{max} \cdot V_{in(min)}}{I_{ppk} \cdot f_{min}}$$

Equation 3.12

As it is observed, one should determine a maximum duty cycle and a minimum working frequency. Transformer is designed according to these decisions. Considering gain curve of the system and desired mode of operation one determines these values. After these decisions, construction of the transformer is straight forward, but design always requires iterations. After a frequency and duty cycle is determine, one calculates the corresponding transformer parameters, but can reach absurd solutions. So there can be modifications at the decisions, as frequency, duty cycle, mode of operation, or switching voltage stresses. For example if you can not reach a desired number of turns, and want to decrease it, you should increase the peak primary side current, so you should change duty cycle or rectified voltage or turns ratio or both.

The operating flux density of the transformer is given by

$$B_{max} = \frac{L_p \cdot I_{ppk}}{n_p \cdot A_c}$$

Equation 3.13

The cross-sectional area AC depends on the core, and given by the core datasheet by producer. Bmax is generally 220 mT. From this equation one can obtain the equation for the number of turns of the primary winding, np.

The number of turns needed by secondary is :

$$n_s = \frac{(V_s + V_{fwd}) \cdot (1 - \delta_{max}) \cdot n_p}{\delta_{max} \cdot V_{in(min)}}$$

Equation 3.14

Ns is secondary number of turns, Vfwd is secondary diode forward voltage. The approximate equation for the output capacitance value is given by

$$C_{out} = \frac{I_{out(max)}}{f_{min} \cdot V_{rip(max)}}$$

Equation 3.15

Vrip(max) is maximum allowable voltage ripple at the (Lidak,1998).

CHAPTER FOUR
METHODOLOGY

4.1 System Overview

SMPS transformer test device shown in Figure 4.1 composes of a PLD, two ADCs, one LCD, one FRAM, buttons and information LEDs, two PWM gate drivers and the connections. All these parts are combined in a printed circuit board which forms the SMPS transformer test device. User should arrange the required connection to the system subject to test.

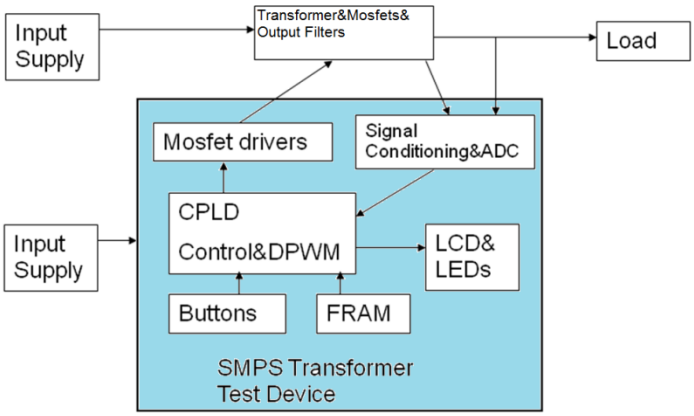


Figure 4.1 Hardware block diagram of proposed SMPS transformer test device.

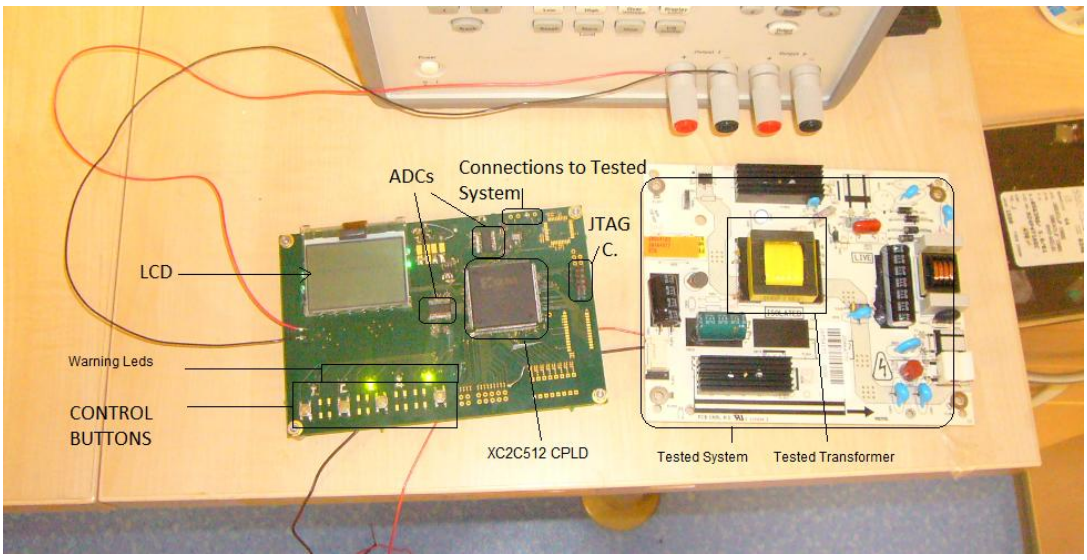


Figure 4.2 A Picture of SMPS transformer test device and a tested setup.

4.2 PWM Control Technique used in this Study

Basically, a system is controlled through it's inputs. A controller seeks the outputs of a system and according to these outputs, it adjusts the inputs. In order to realize this, controller makes use of a reference signal for the system output, in order to reach a steady state. But it is not a must to reach a steady state for all system and control structure, but for SMPS systems, reaching a steady state is always the case. So controller in SMPS systems always tries to decrease the error between the reference signal and the real output at the moment.

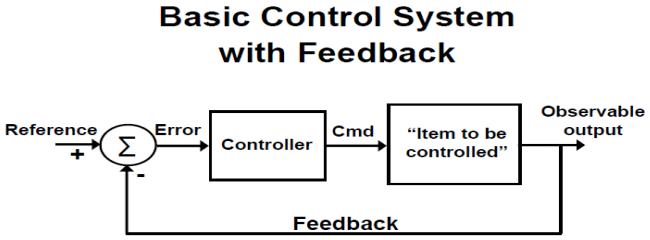


Figure 4.3 A general closed loop structure.

In order to control an analog system with digital units we have to model the system and make some analog to digital conversions, converted data then processed by a transfer function and an array for DPWM (Digital Pulse Width Modulator) is produced. Then DPWM produces the drive signals for switching components using a clock signal.

In order to design and test a SMPS transformer, you should first determine the aim of SMPS system. The first step in power-supply design is to choose a topology that fits the application's needs. Choices are non isolated topologies as step-up (boost), step-down (buck) or isolated topologies as flyback, forward, half-bridge or full-bridge. Next, switching technique must be selected, continuous mode or discontinuous mode, or whether hard-switch, soft-switch or resonant. Whilst soft-switching offers lower losses, it can require more complex circuitry and control algorithm. Considering control architectures, there are also Current Mode Control and Voltage Mode Control Techniques.

Although study aims to cover all topologies, it mainly focuses on Flyback Topology and a Modified Voltage Mode Control Technique. Flyback Topology is more common and Voltage Mode Control Technique is easier for Digital Control Techniques. The Voltage Mode Control Technique only needs to monitor the output voltage so only one ADC and one feedback path is required, thus simplifies the design of the Control Loop. But in Voltage Mode Control Loop , inductor pole or delay is not taken in to account, so the circuit lacks current limiting to protect the circuit components, especially switching unit, and offers a slower response to input or output transients. Voltage mode has two poles at feedback loop.

In Current Mode Control Technique peak inductor current is controlled directly by the error signal, so technique eliminates potential circuit failures due to excessive current conditions. Current Mode Control Technique has faster response due to single pole system. Output capacitor is removed from feedback path. But control stability is more difficult with duty cycles bigger than 50%. In Current Mode Control Technique wide input voltage variation causes duty cycle passes 50% of duty. So in Current Mode Control Technique wide input voltage variation is difficult to support and low current loads is difficult to control due to insufficient level changes at inductor current. In Current Mode Control, these facts require control algorithm to use slope compensation to prevent sub-cycle oscillations. Slope compensation is a slight adjustment of gain coefficients in control loop. Control loop uses an adjusted imaginary slope to determine the peak current according to error signal and previous duty cycle value derived from the control loop. Figure 4.6 shows the mechanism of slope compensation. Even we use this compensation slope, Current Mode Control Technique has bigger diffractions from goal working point, due to big tolerances in inductance, and the current over the inductance.

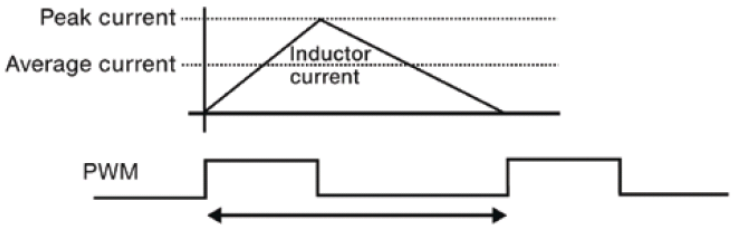


Figure 4.4 Peak and average current if duty is smaller than 50%.

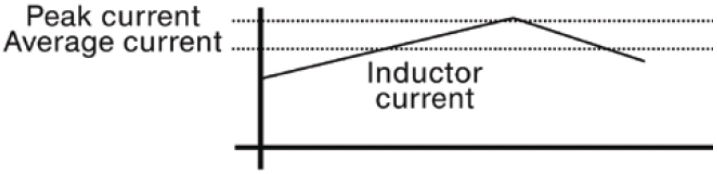


Figure 4.5 In duty cycles greater than 50%, average current is more than one-half of the peak current.

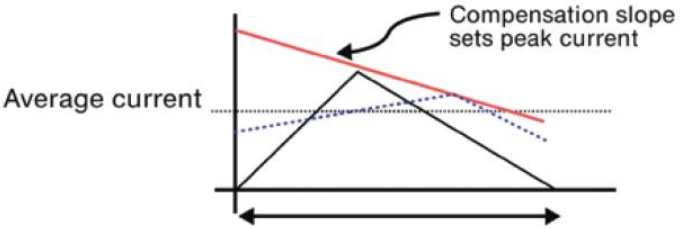


Figure 4.6 Imaginary compensation slope.

If we adjust PWM duty cycle of switching components according to current over inductor as in Current Mode Control Technique, we need to monitor the current over inductor through whole switching period, and we need sampled data from the current at every instant in order to determine the next PWM duty cycle information. We need fast conversions, so a very powerful ADC.

The accurate sensing of inductor current is difficult to achieve with high accuracy. Typically, low ohmage resistors are inserted in the current path and the voltage drop across the resistor is measured as an indication of the current. To minimize heat dissipation and voltage drops, the current sensing resistors are typically in the tens of milliohms range. The resultant voltage drops are in the millivolt range. Amplifying small signals in the presence of huge switching currents is a daunting task. Instead of measuring this small current at every instant, measuring at the instances that we wait

current is maximum is more beneficial. So we can attain the maximum value of the current at each on off cycle. This is correct if the SMPS system we are struggling is not a resonant type.

Both Voltage Mode Control Technique and Current Mode Control Technique have its weak points. In this study PWM duty cycle is determined mainly according to the output voltage, and current over inductor is monitored just at some instances, namely, at the end of on-time of the switching component. But there is some conversion time margin, measurement is not realized just at the end of the on time of the switching component. Measurement is realized slightly before the end of on time of the switching component.

This study assumes inductor current reaches its maximum level at the end of on-time of the switching component PWM signal. So this study can be inappropriate with Resonant Mode Power Supplies, in which peak point of the inductor current differs according to working frequency and the condition of the open loop system. Open loop system is input voltage, inductor, output filter and the load. In this study, sampled inductor current data is used to alter the on-time directly, regardless the state of the output voltage of the system. So ADC result of inductor current is the master. But inductor current participates in duty cycle formation only if current limit decided by the control loop is exceeded. So duty cycle is adjusted mainly according to the result derived by the ADC of output voltage. This study calls Modified Voltage Mode Control Technique to this technique.

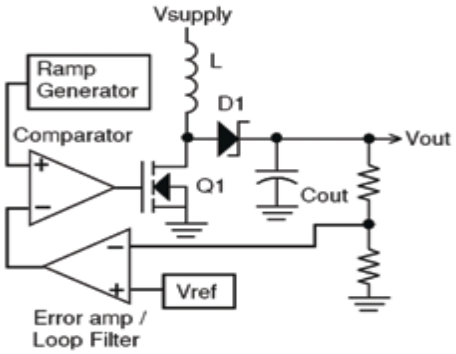


Figure 4.7 Voltage Mode Control Technique.

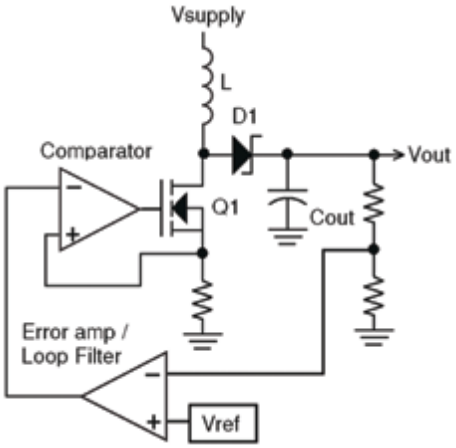


Figure 4.8 Current Mode Control Technique.

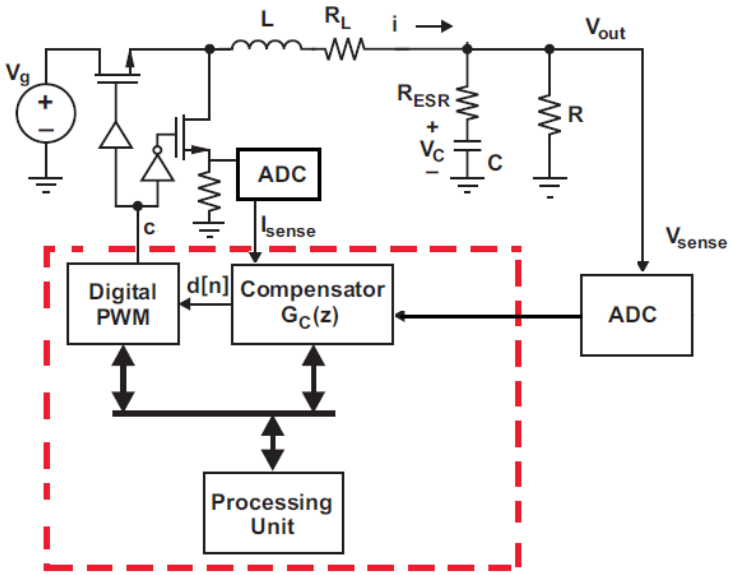


Figure 4.9 Modified-Voltage Mode Control Technique.

Modified Voltage Mode Control Technique of this study works as the following. present duty value, present frequency value, present current value, present output voltage value are stored in numeric variables. Desired output voltage value is entered by the user to another variable. After user starts the PWM switching, system starts from predefined initial values for all variables. At start up, initial frequency is 250 KHz, initial duty cycle is 5%. PWM signal sweeps from initial frequency to lower frequencies. Meanwhile duty cycle is also increased slightly, at each step. If the desired output voltage is reached during this sweeping period, device settles at that frequency and duty cycle. Operation of the device assumes open loop system is

steady. That is to mean, input voltage and load is fixed. Proposed device finds the optimum working point for specific passive elements, input and load condition. If desired output voltage can not be reached during sweeping period and output voltage begins to decrease, device again stops the sweeping and settles at the closest point to desired output voltage. If output voltage begins to decrease, that means switching frequency goes far away from maximum gain point of the open loop system gain curve. So it is not logical to further decrease the frequency to reach desired output voltage.

This study assumes SMPS systems should run at the right side of the maximum gain point of the gain curve and should be as far away from the maximum gain point of the observed from bode plot. So the device jumps to a bit right of the gain curve, after the goal output voltage is reached and sweeping ends. Quantity of this jump is determined according to frequency and duty cycle value at the end of sweeping. Duty cycle adjusted again to reach the desired voltage, after the jump. The device continues switching unless the user ends the operation. The device feedback loop can tolerate small input and load changes, but is not capable as a standard SMPS controller. Here, it should be understood that the device in this study is not a SMPS controller; SMPS transformer test device just finds the optimum operating point of a SMPS system for predefined working parameters, input voltage, output voltage, load and filters.

In case of test setup with a transformer which has 25 uH secondary, 300 uH primary and 10 uH leakage inductance, with an output filter capacitor which has 1000uF, and with a 220 mA load from 3.3V which is approximately 15 ohm load condition, a simulation is realized with Proteus simulation program and observed what are the duty cycle and switching frequency that work best with this sample system. If we look at the pode plot of the system given in Figure 4.16, it is logical to work left side of the maximum gain point if we want our system works as a current source.

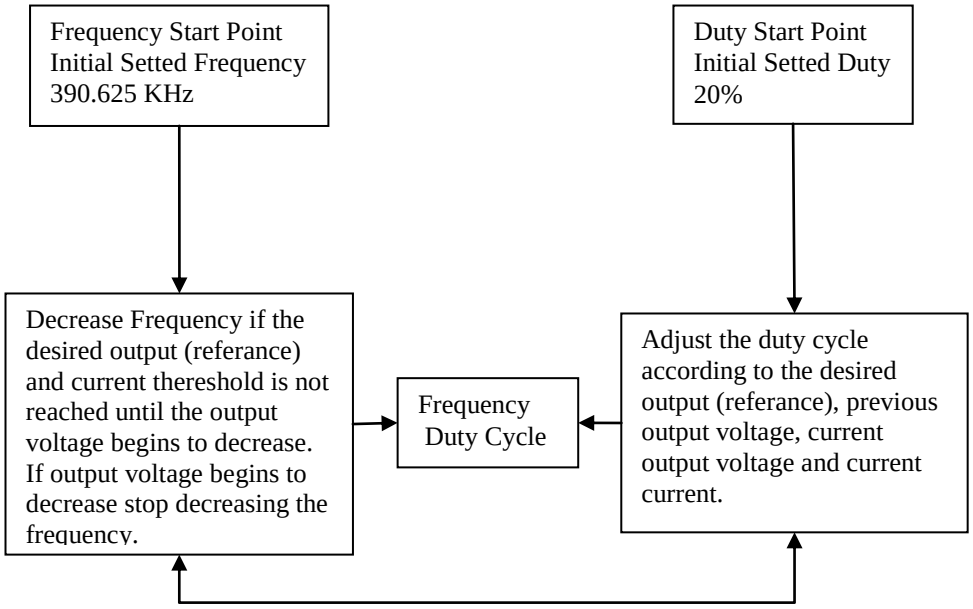


Figure 4.10 Frequency and duty cycle Adjustment Scenario

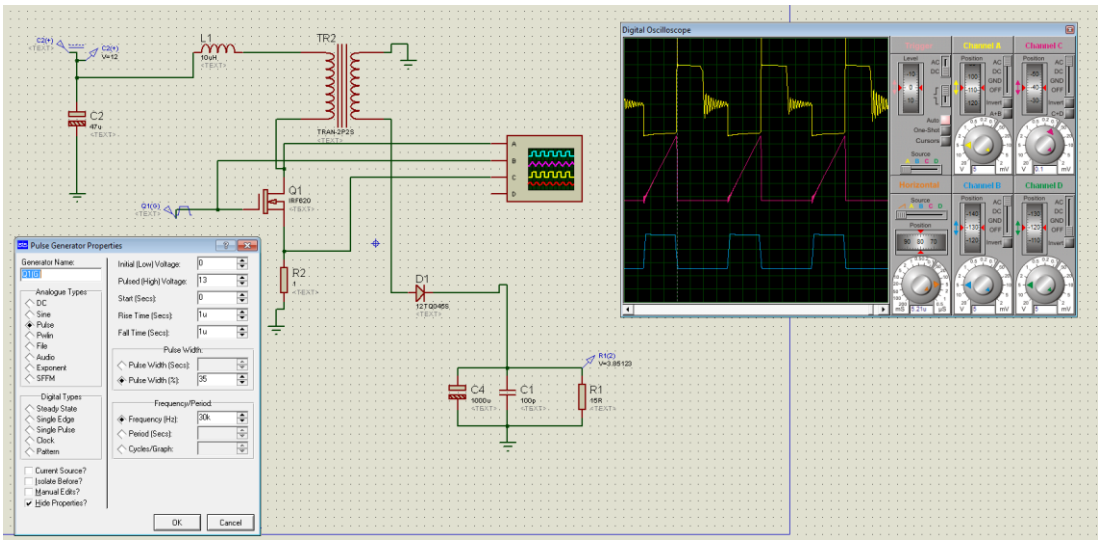


Figure 4.11 Sample test system tested at 30 KHz and 35% duty. Output is 3.86V.

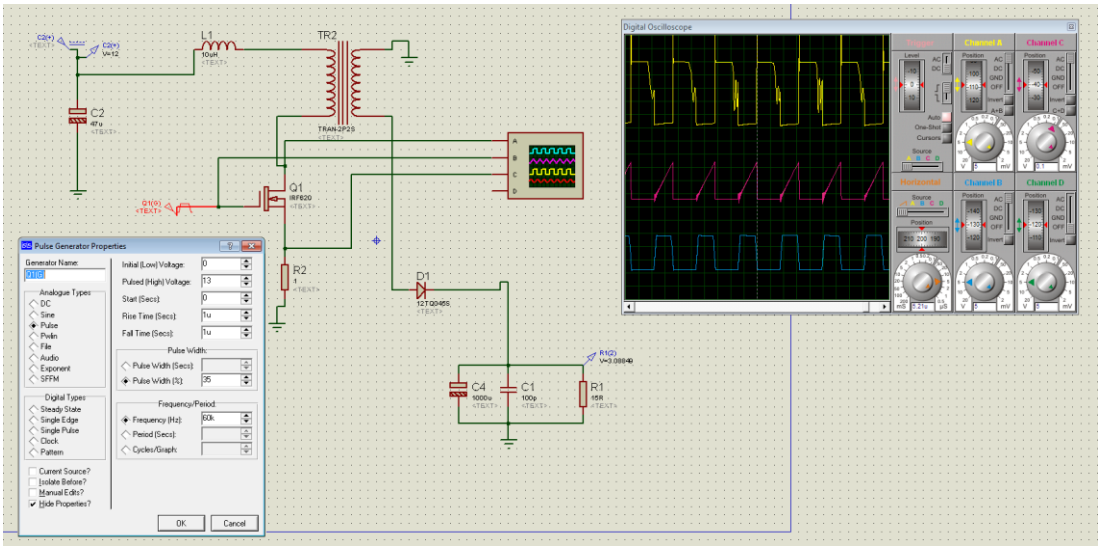


Figure 4.12 Sample test system tested at 60 KHz and 35% duty. Output is 3V.

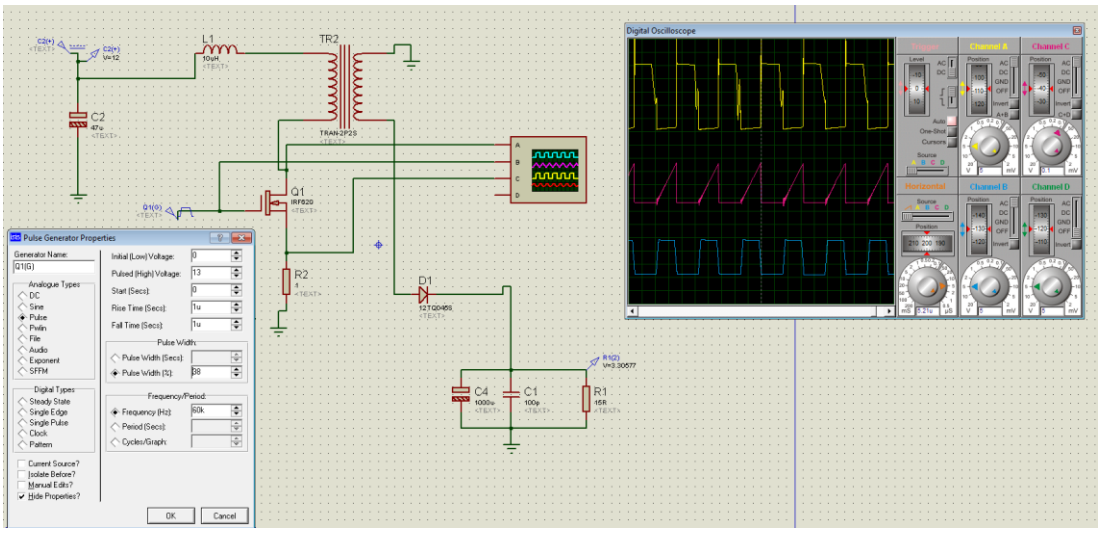


Figure 4.13 Sample test system tested at 60 KHz and 38% duty. Output is 3.3V.

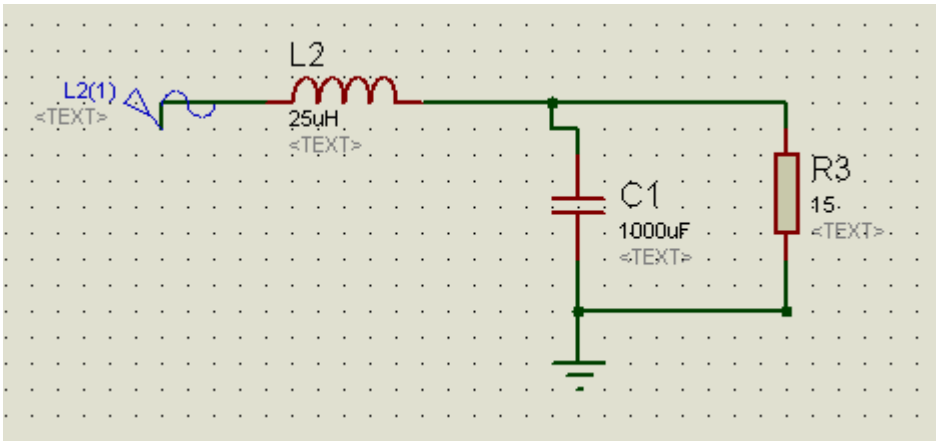


Figure 4.14 Secondary side approximation of the tested system. Bode plot is found according to this approximation.

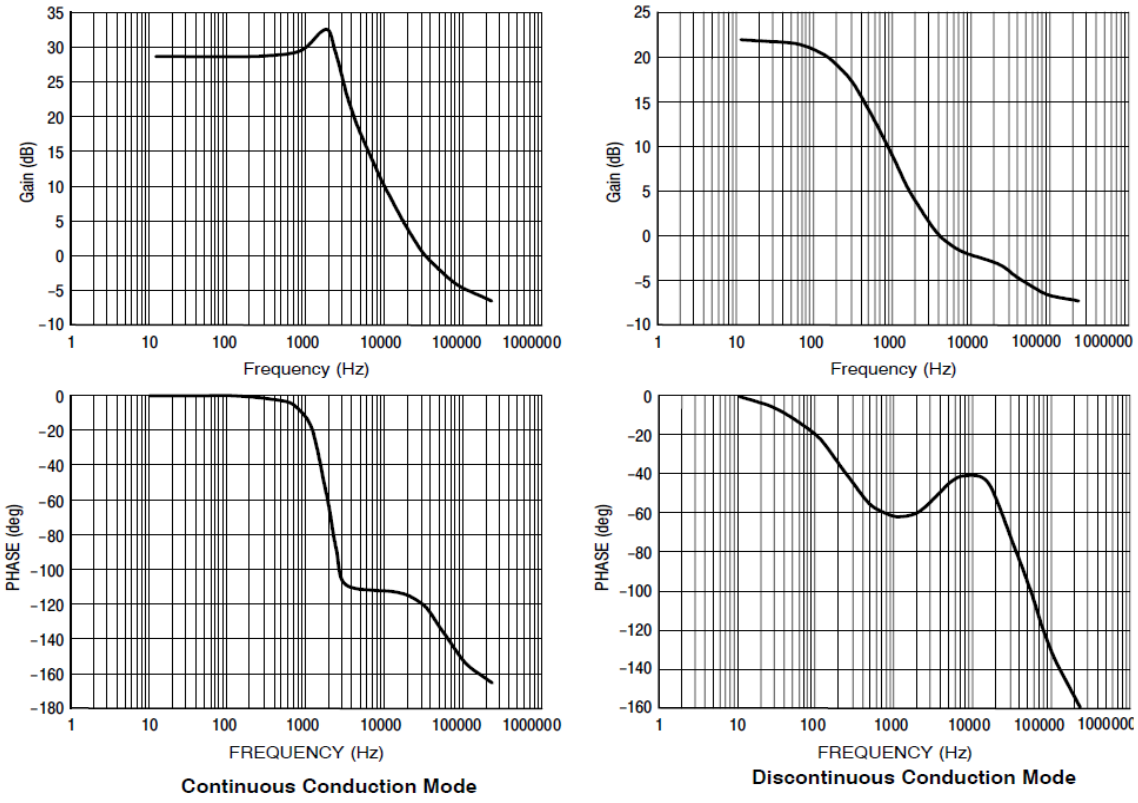


Figure 4.15 Bode plots of a general flyback system.

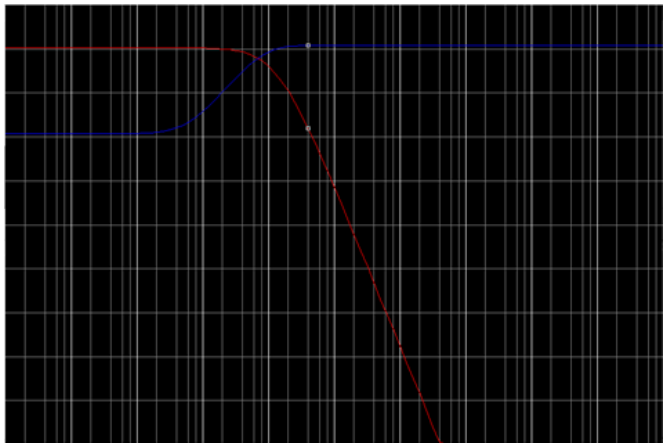


Figure 4.16 Bode plot of the secondary side approximation of the tested system.

4.3 Interfaces of SMPS Test Device to Tested SMPS System

Device has four signal connections to tested SMPS system and a reference ground connection. Signals are two PWM gate drive signals and one ADC input for output voltage level and another ADC input for inductor current level. Gate drivers are complements with dead times. For example for a standard flyback system just one PWM gate drive signal is used. For a half bridge system both gate drive signals are used.

4.3.1 ADC Interface

Device measures the output voltage and inductor current through ADCs, in order to seek the condition of tested SMPS system. Device utilizes two 12 bit, 30MSPS analog-to-digital converter (ADC) to measure these parameters. ADCs are Texas Instrument's THS1230IPW TSSOP ADC. The THS1230 is a CMOS, low-power, 12-bit, 30 MSPS ADC that operates with a 3.3-V supply. It has CMOS parallel interface. The analog input to the THS1230 is differential with a selectable gain of 0.5 or 1.0. Gain value is pin selectable. The internal reference can be bypassed to use an external reference to suit the dc accuracy and temperature drift requirements of the application, so the THS1230 provides a wide selection of voltage references to match the user's design requirements.

At the beginning of this study, a market investigation is performed and this ADC found suitable for this application. Application in the SMPS transformer test device requires a parallel interface between ADC and the PLD. Serial interface is difficult to implement over CPLD VHD code and consumes more time for data transfer. This ADC also can be run with 3.3 Volts, which is common for other blocks of the SMPS transformer test device. THS1230 has also enough sample rate for this study. 30 MSPS is suitable for the application of the SMPS transformer test device.

Normally analog control provides a very fine resolution in the output voltage. The output voltage can be adjusted to any arbitrary value, which is only limited by loop gain and noise levels. However because of the quantizing elements exist in the ADC and DPWM, the digital controller has a finite set of discrete levels in nature. Thus the quantization of A/D converter and DPWM is critical to both static and dynamic performance of power converters.

The need for a certain amount of accuracy in representing analog signals by their digital equivalents governs the ADC resolution or the ADC number of bits. Resolution of the A/D converter should be such that the output voltage error of power converter tightly falls within the allowed voltage range. That is the least significant bit (LSB) of the ADC (VLSB) has to be less than the allowed maximum scaled output voltage variation ΔV.

$$V_{LSB} = \frac{V_{\max}}{2^{N_{ADC}}} \le \Delta V \cdot G = \Delta V \cdot \frac{V_{ref}}{V_{out}}$$

Equation 4.1

Vref, Vout and Vmax are the reference, output and maximum output voltage respectively. Then the required resolution NADC of ADC with respect to a chosen reference voltage level can be acquired by Equation 5.2.

$$N_{ADC} \ge \text{int}\left[\log_2\left(\frac{V_{\max}}{V_{ref}} \cdot \frac{V_{out}}{\Delta V}\right)\right]$$

Equation 4.2

Where function int[ ] takes the upper rounded integer value of the product.

Equation 5.2 indicates the minimum number of bits of the ADC to meet output voltage regulation requirement of power converters. For example, a voltage regulator with 1.5V reference voltage, 5mV allowed voltage variation, if G=1 and the voltage scale range of ADC is 1.8V, then a minimum 9-bit resolution will be required for the ADC.

Hence any sensed voltage should be scaled down to Vref, and appropriately reflected in feedback gain while designing the control loop. In a particular SMPS application, the need for sensing output voltage or inductor current decides the minimum required resolution, since the resolution should be higher than the tolerable output voltage or inductor current ripple. The Higher the ADC resolution the faster would be the system response as errors in the loop can have higher resolution and can be quickly corrected.

The precision with which a digital controller positions the output voltage is determined by the resolution of the ADC module. For example, regulation resolution of at 5mV at Vin = 5V corresponds to ADC resolution of NADC = log2 (5V/5mV) ≈ 10bits.

Another important criterion for the choice of ADC is its conversion time and power consumption from time of measurement at the input to the availability of the digital word at its output register. Modern high speed ADCs still have around hundreds of nanoseconds of conversion time. The conversion time can also be interpreted as the maximum allowable sampling frequency fsamp of an ADC. There are three important effects of conversion time delay. Firstly, such a delay prevents immediate controller action due to this time delay and secondly, its presence is a limit to the sampling frequency and hence limits the bandwidth of the system. Finally for low-power high-frequency SMPS applications, the power consumption of ADC is becoming critical with the increase in sampling frequency (Guo,2009).

A wide choice of ADC architectures exist that differ in resolution, bandwidth, accuracy, and power requirements. The major conventional ADC devices that are designed for general industrial applications mainly have architectures of Parallel Flash ADC (Choudhury,2004), Successive Approximation (SAR) ADC (Mortezapour,2000), and Pipelined ADC. However, both SAR and pipelined ADC are operated with multiple stages, which introduce larger latency since they need several cycles to convert the analog signal, they are more robust and consume less power. Although multistage ADC topologies can have high sampling rate, they have larger latency due to either multiple comparisons or digital filtering. By contrast, the single stage flash architecture has the advantage of being very fast because the conversion occurs in a single cycle. The main disadvantage of the flash structure is that it requires a large number of comparators (2N-1 comparators for an N-bit ADC). A 10-bit full range ADC will require 1023 (210-1) comparators, which results in large silicon area and power consumption.

This Study's choice, THS1230 is a pipelined ADC. Though it's conversion time is not as better as parallel flash counterparts, it is enough for this application. And also because of logistic issues, THS1230 is used.

Digitized data sampled from output voltage and inductor current are stored and used by the control algorithm implemented in the CPLD's VHDL code. Because of the noise level of the board, least significant 5 bits are not taken in to account. ENOB of SMPS transformer test device is 5. Although trials to decrease noise level are performed, a noiseless ground can not be accomplished. This occurred most probably due to poor layout design. In designs with ADCs, one should care about the supply filtering and signal layer design. At the beginning of the layout design, lack of knowledge caused inproper layout considering ADC parts.

Due to unavailable least significant bits, maximum values of output voltage and inductor current is normalized to 7 most significant bits of ADCs. The output voltage given by the user, current output voltage and the current inductor current are represented by 7 bit arrays in VHD code.

4.3.2 PWM Gate Drive Interface

SMPS test device has two gate drive signals for the switching components of the tested SMPS system. Study assumes switching component is an important part of the system considering performance. Rise and fall time of switching component affects the effective on time, transformed power to the output and inductor performance. So switching component is thought as a part of the SMPS transformer and in order to test a transformer one should specify the switching component. SMPS test device uses two AD8565 opamps to produce a gate drive signal. This gate drivers amplify the gate drive outputs of the CPLD. AD8565 produces a 10V gate drive signal, and can charge and discharge 1nF capacitor in around 10 ns. So almost all N-type mosfets can be used with SMPS test device up to 1 MHz switching frequencies. But due to limits of CPLD and VHD code of the study theoretical limit of working frequency is 390 KHz. This can be changed using a faster reference clock for the CPLD. In this study a 25MHz clock is used. Maximum operating frequency is setted to 208 KHz as a maximum in VHD code.

4.3.3 Power Supply Interface

SMPS test device needs input supply, user should provide a supply between 3,3V and 14V. SMPS test device extracts maximum 1,25Watts or 250 mA if the input is 5V. This supply can also be provided from the tested SMPS system input supply, if it is below 14 V. User should arrange the required connections and external devices.

4.3.4 User Interfaces of SMPS Transformer Test Device

SMPS test device has control buttons and a LCD screen. From buttons user can enter the desired output voltage, start and stop the operation. Device works as explained in Figure 4.18. As it can be seen from the chart PWM gate drive signals are active until user cuts the input supply of the device or presses the On/Off button. Places of the buttons are given in Figure 4.17.

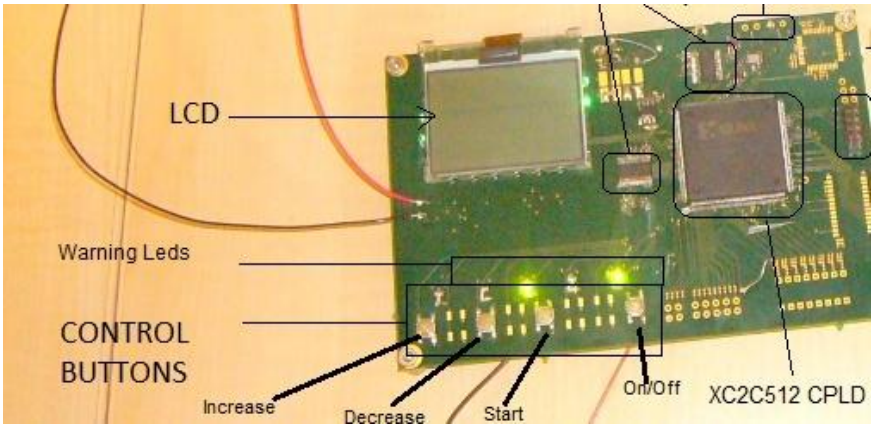


Figure 4.17 Control Buttons.

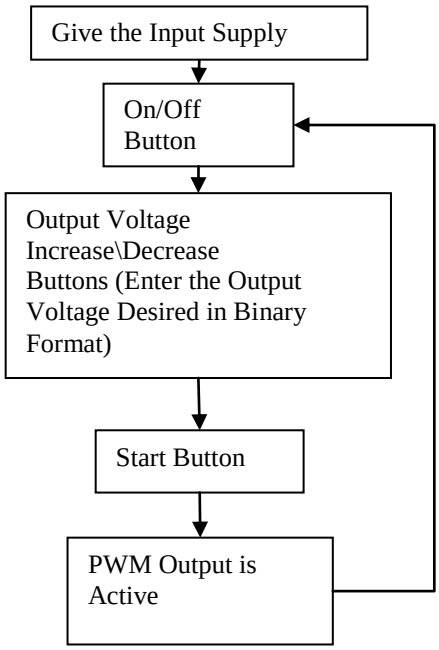


Figure 4.18 User control flow chart.

LCD screen shows the desired output voltage entered, working duty cycle and working frequency in binary format. Because CPLD has not enough source to realize a binary to decimal transformation, SMPS test device just uses the binary representations of the variables. Binary to decimal conversion requires divisions which are performed through concurrent multiplications and storing the solutions of each multiplication for the next step, a lot of source is needed. Some ready functions are available in arithmetic.lib library in VHDL, but these too requires too many source. Also the CPLD this study used, XC2C512 does not support these functions, so Xilinx ISE gave errors while realizing synthesizing with these functions.

OGM-96GB03-C-KE190 dot-matrix LCD from ORION DISPLAY TECHNOLOGY is used for SMPS test device. A picture of the LCD is in Figure 4.17. It has a serial control interface. LCD is controlled from Serial Input Clock (SLCK), Serial Input Data (SID), Register select (RS), Chip Select (CS) and Reset signals. OGM-96GB03-C-KE190 has a 8 bit data format both for control registers and display data.

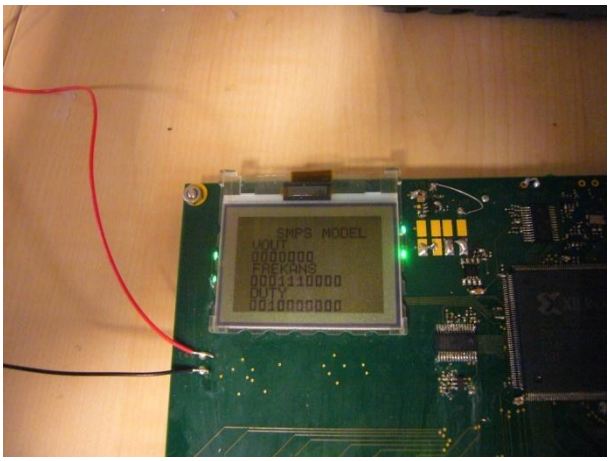


Figure 4.19 OGM-96GB03-C-KE190 dot-matrix LCD.

In VHD code, there is formed a LCD driver module to put any alphabetic or numeric data on the screen. This module always seeks the working frequency register, working duty cycle register and output voltage register, and puts these variables stored at that instant to the LCD. At the start up, this module also sets the instruction registers of the LCD for its operation format. Operation is given in Figure 4.20. OGM-96GB03-C-KE190 LCD uses S6B0724 LCD controller. Instruction set of S6B0724 LCD controller is given in Appendix. Knowledge of the instruction set can be beneficial to understand the operation.

4.3.5 SMPS Transformer Test Device VHD Code Structure

Operating code of SMPS Transformer Test Device is formed on VHDL platform Xilinx ISE Design Suit 10.1. The structure bases on states of the operation. Firstly, code waits user to open the device. Second, user should enter the desired output. After desired output is setted user should press the start button. After the start button,

PWM signals drives the switching elements of the system, and settles at an operation point according to the feedback coming from ADCs. Device continues to operation unless the user stops the device or power is cut.

Desired voltage is entered in binary format. SMPS transformer test device uses 7 bits to represent the output voltage. Vout is incremented in 30 mV steps. Thus in order to enter 3.3V at the output, user should enter 1011(decimal 11) to the LCD screen. This 30 mV step value comes from the feedback resistors and the ADC resolution.

Frequency and duty are also represented in binary formats. Frequency is found by dividing the decimal value on the screen to the 25 MHz. Duty is found by the division of the value found by multiplying the decimal value on the screen with 4 ns, to the inverse of the working frequency, which is the period.

Duty=(4ns * value on LCD screen) / (1/ working frequency)

Equation 5.3

Block diagram of VHD code of this study is presented in Figure 4.21. VHD code composes of five basic processes. These are desired output voltage setting process, operating frequency adjustment process, operating duty cycle adjustment process, frequency sweeo process at start up and LCD driver module. All these processes work at the same time concurrently. They share some same signals, they gives outputs to other or takes input from other function. After desired output voltage is set by the user, output voltage setting process starts the three lower processes, frequency adjustment process, frequency sweep process and duty cycle adjustment process. These three processes co-work to produce the PWM gate drive signal. Frequency sweep signal takes part only at start up, it does not do anything after steady state, sweep ends. LCD module start right after the user sets the desired output value and always seeks the operating frequency vector and operating duty cycle vector. It drives the LCD with the current data.

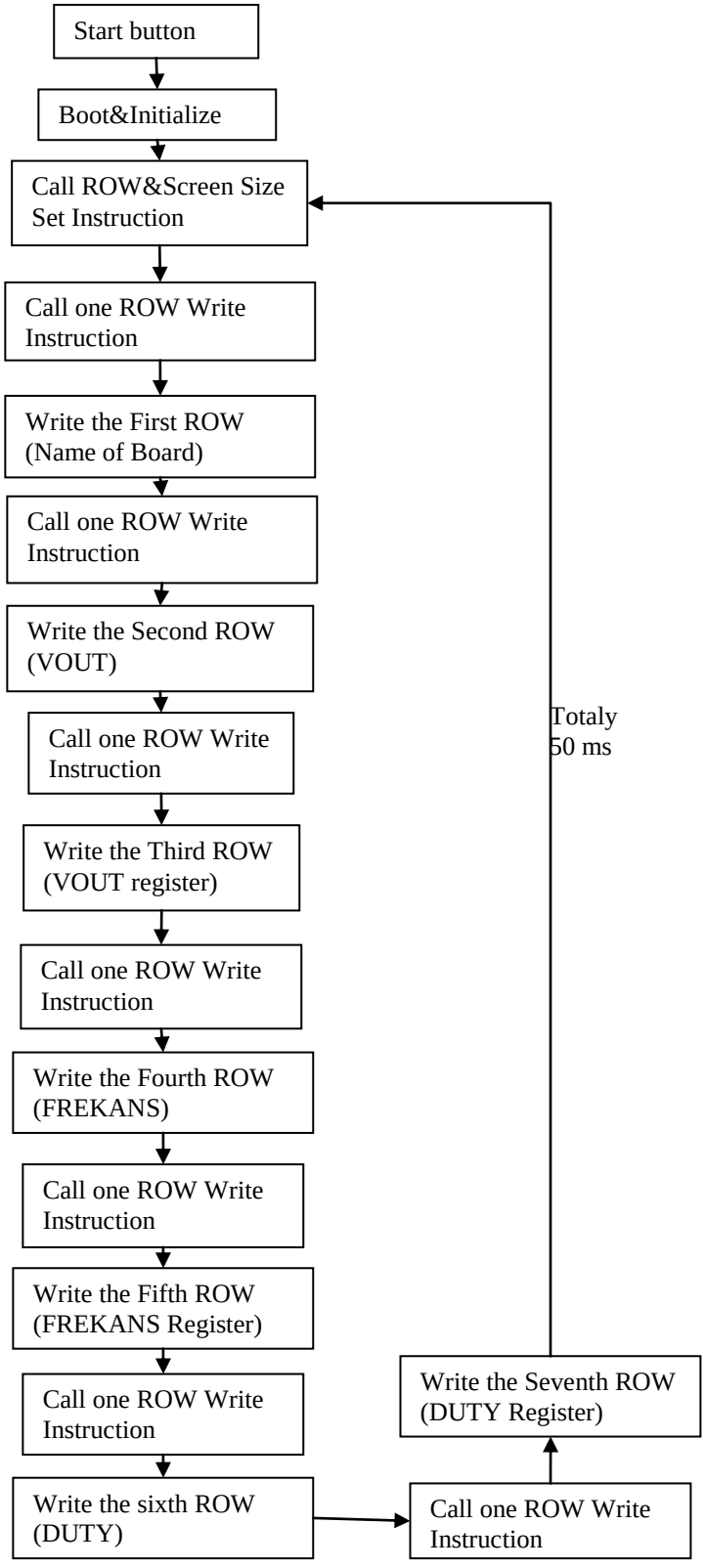


Figure 4.20 LCD driver module flow chart.

4.3.6 A SMPS System Available in Market is Tested with SMPS Transformer Test Device

Performance of the SMPS test device is checked over a sample SMPS board in Figure 4.22 which can be found in market. Sample SMPS board used in this test is a TV power supply board that works through 220VAC and provides one output which is 12V and 3A. Working frequency and the duty cycle of the sample SMPS board at 0,5A load is observed. Then SMPS controller of tested system is extracted and the switching mosfets are driven through the SMPS transformer test device. Oscilloscope outputs are recorded.

It is observed from this test that SMPS test device states a close operation point with the original SMPS controller of the board as in Figure 4.23 and Figure 4.24. While original board works at 33 KHz and 6% duty, SMPS test device states the transformer of the tested power supply should work at 29KHz and 4-5% duty, for 12V output and 0,5A load.

The start up performance of SMPS test device is investigated and there found a bug in VHD code. The PWM gate drive signals stop at a point at the start up, before starting the fast sweeping. The situation is observed in Figure 4.25. It is solved in time while the study goes on, but can not be tested with the tested TV power supply board. The bug is not observed with hand made sample SMPS sytem which is presented in next section.

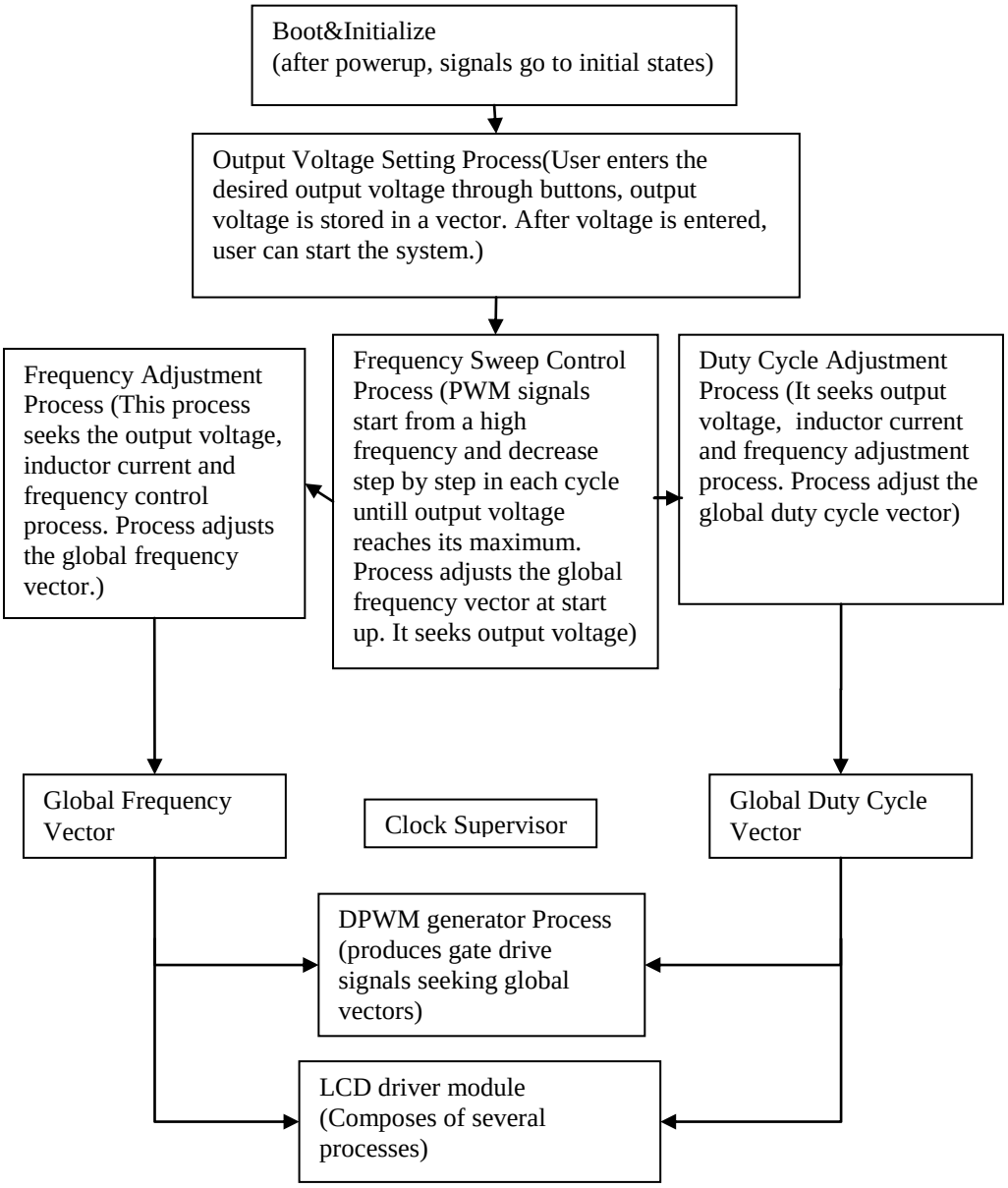


Figure 4.21 VHD code block diagram of this study.

4.3.7 A Sample SMPS System Made to Test SMPS Transformer Test Device at Limit Conditions

A sample SMPS system in Figure 4.26 is realized to test and find the limits of the SMPS transformer test device. A sample SMPS transformer is wounded with the specs 13V input and 3,3V output at 0,5A. Sample SMPS transformer is wounded to work at 40 % duty and 60 KHz.

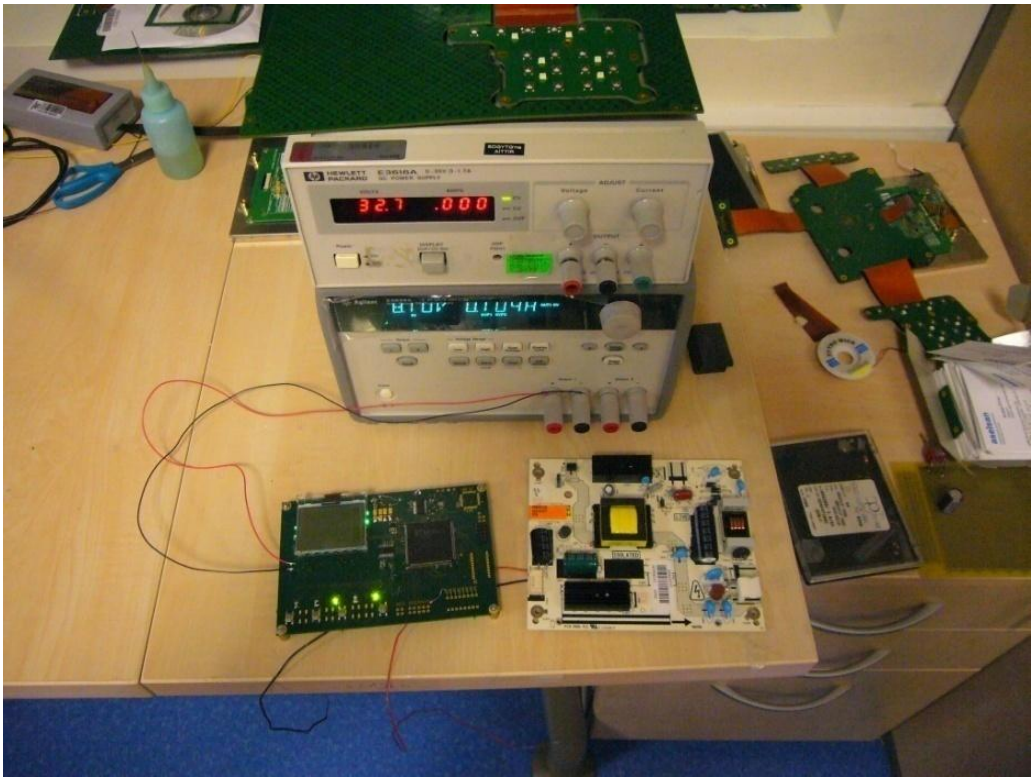


Figure 4.22 A SMPS System available in market is tested with SMPS Transformer Test Device.

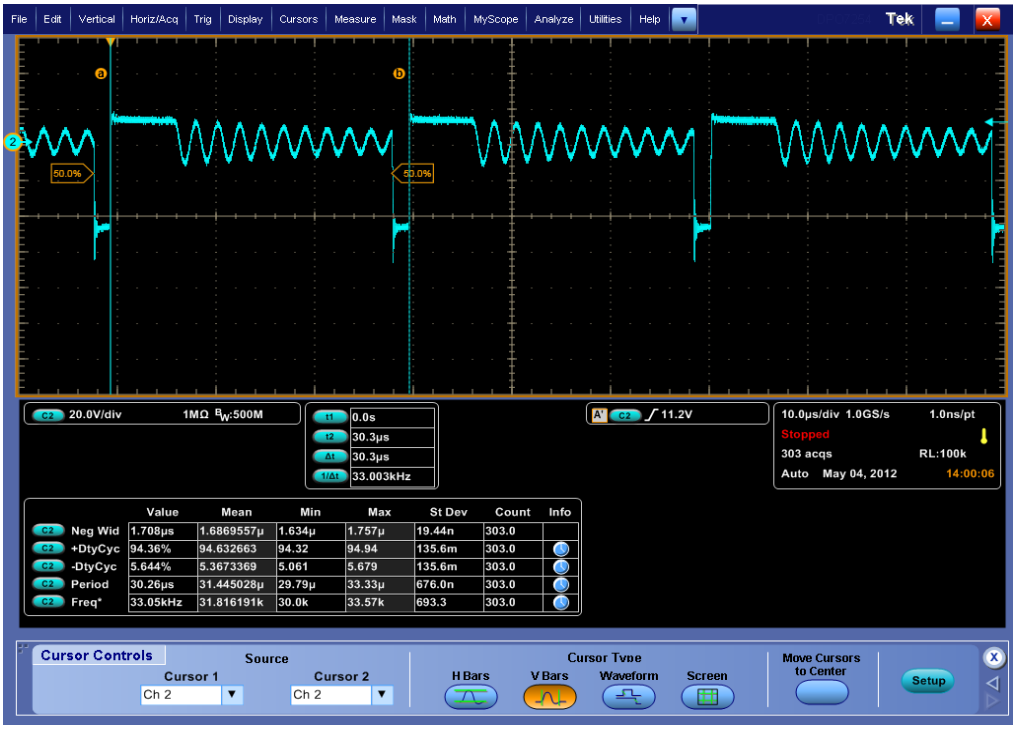


Figure 4.23 Tested TV power supply frequency and duty cycle at 0,5 A load with original SMPS controller.

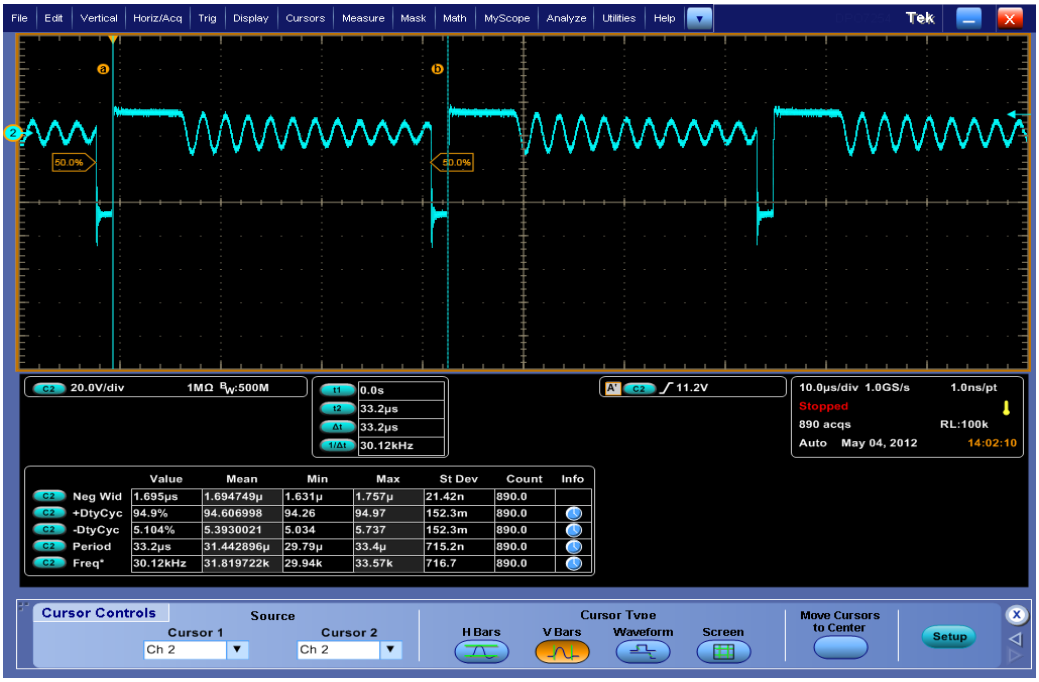


Figure 4.24 Tested TV power supply frequency and duty cycle at 0,5 A load while the mosfets are driven by SMPS transformer test device.

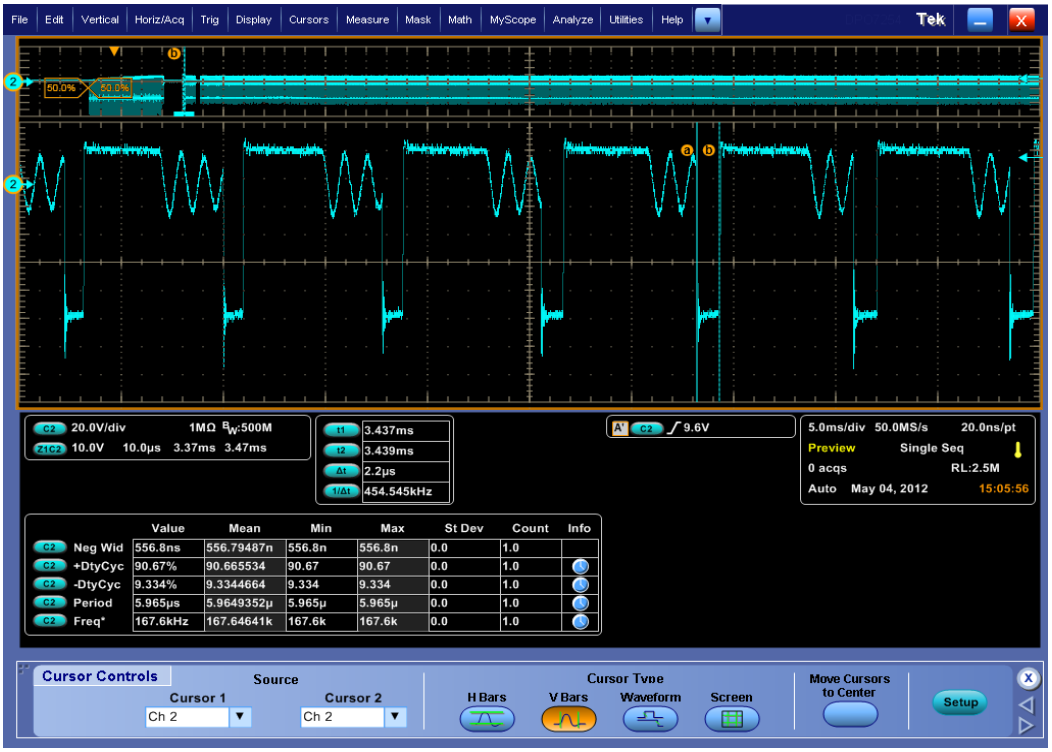


Figure 4.25 Tested TV power supply frequency and duty cycle at 0,5 A load while the mosfets are driven by SMPS test device- Start up, switching stops for a while sweeping continues.

According to the performance of the SMPS test device, it is observed that it works well with steady output. SMPS test device finds the optimum working points found from the calculations. There occurs some diffraction at the frequency, most probably due to sweeping algorithm of the code, but beside this, SMPS test device almost finds the calculated values.

It is observed through the tests that SMPS test device works at close points to the calculated values. Sample SMPS transformer is designed to work at 40% duty and 45 KHz to provide a 3,3V and 0,5 A load. But SMPS transformer test device makes SMPS transformer stabilizes at 34% duty and 40.8 KHz. The oscilloscope waveforms can be observed through Figure 4.27 and 5.28.

Another test is made at 3,3V and 1A. Sample SMPS transformer is expected to work at 45% duty and 32 KHz. Test result with SMPS transformer test device is 38% and 25 KHz. In order to clarify the effectiveness of the SMPS transformer test device, there will be made more tests with more SMPS systems but because of lack of time, there was not that opportunity

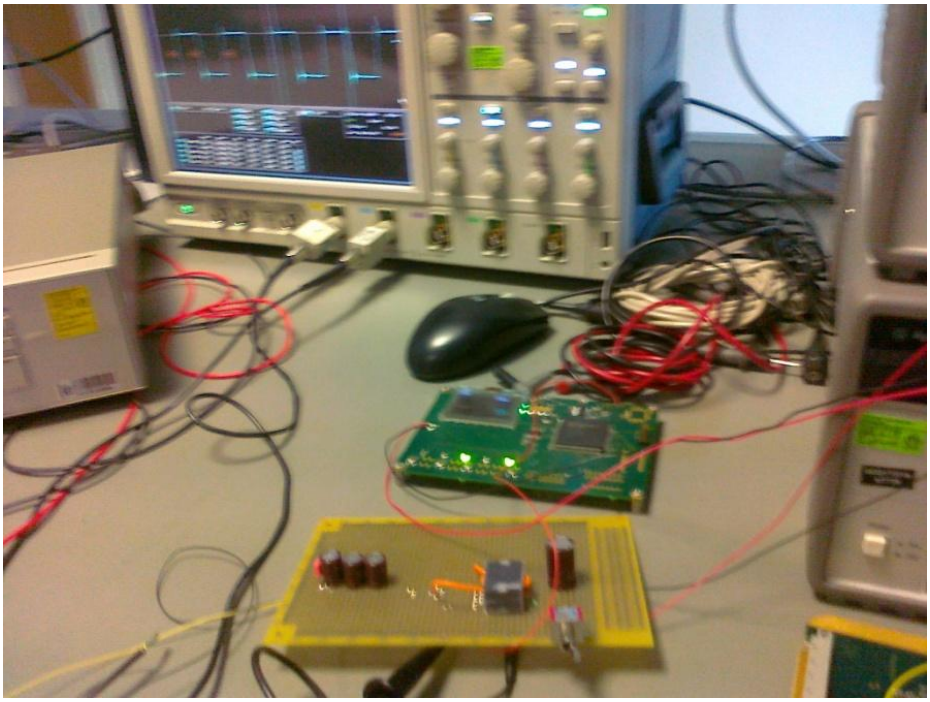


Figure 4.26 A sample SMPS is made and tested with SMPS transformer test device.

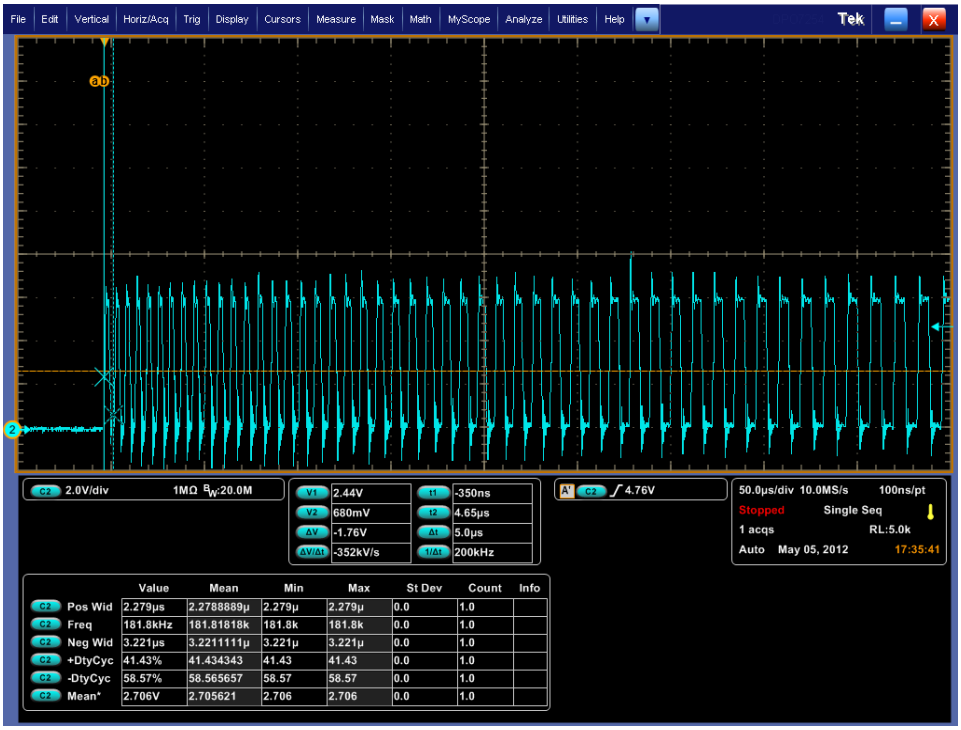


Figure 4.27 A sample SMPS is made and tested with SMPS transformer test device –PWM Gate Drive signals at start up with 3.3V output and 0,6 A load.

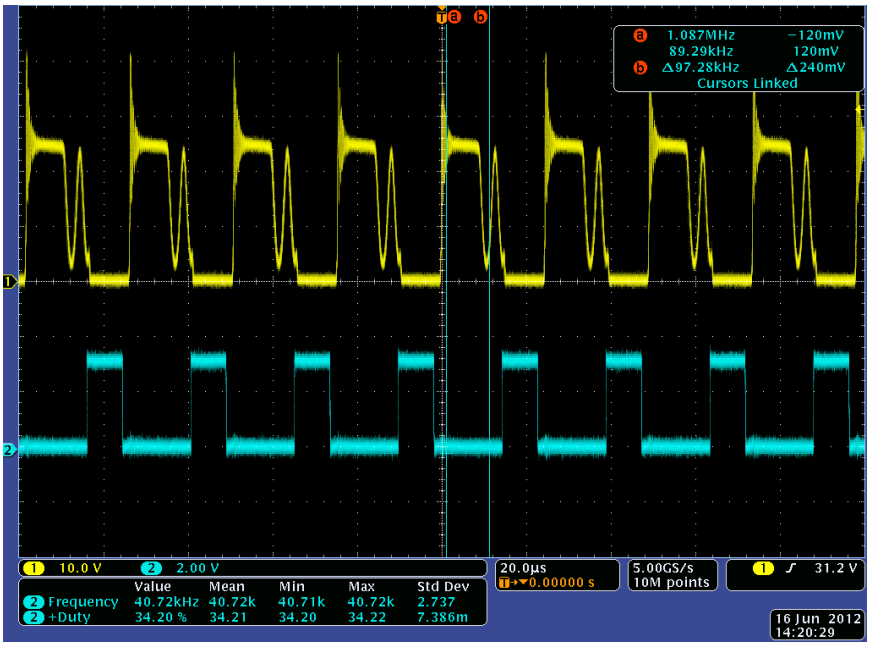


Figure 4.28 A sample SMPS is made and tested with SMPS transformer test device – PWM Gate Drive signals at steady state with 3.3V output and 0,6 A load.

CHAPTER FIVE
CONCLUSION AND FUTURE WORK

A method to test a SMPS transformer is studied through this thesis. A VHDL code is formed to control a SMPS system and show some information on a LCD and information LEDs, according to that SMPS system and operation parameters. In order to realize closed loop control, a digital control technique of SMPS is formed. A SMPS controller block is realized through this digital control technique.

Topics as programmable logic devices, VHDL designing, SMPS design fundamentals, ADC fundamentals, DPWM techniques and implementation constraints, LCD driving issues and PCB design issues with ADCs are investigated and applied. As a result, a device is realized and some tests are performed with this device. A commercial TV power supply is tested. This power supply is driven by proposed device just by extracting power supplly's analog controller. SMPS transformer test device settled at a close point to original analog controller's operation point. Another test is realized with a handmade SMPS transformer and system. SMPS transformer test device settled at close points to calculated operating points. It seems device successively finds the optimum working points of the tested systems. But there needs to be made more tests with more SMPS systems and SMPS transformers.

Proposed SMPS test device can be beneficial to shorten design duration of SMPS systems. Though information that SMPS test device provides can be found through SMPS system modeling and calculations, device can be beneficial to see the real world situation of the tested system.

There made other gainings from this study. How to use an ADC properly was a big observation for future studies. It is observed that due to inadequate PCB design, how you loose the ENOB of the ADC and what can be done in such a situation to make your system work. Another gaining is how to make a concurrent design within VHDL to increase the performance of the PLD and to decrease the used number of

source of the PLD. LCD driving concerns and character representation issues over an LCD are compromised. SMPS system design topics are remembered.

Beside those already made stuff, this study can be beneficial to be a starting point to digital control studies of SMPS. There are many new studies concerning digital control implementations with PLDs. This study focused on realizing a platform that can find the optimum operation point of a SMPS system for a specific system condition which means a specific input, output and filters. In order to realize this task, study used digital SMPS control techniques. But device proposed by this study is not a SMPS controller, study does not suggests a device that can be used as a SMPS controller. For a future work, by adjusting the control algorithm and increasing the control loop performance, a digital SMPS controller can be realized. Different digital control techniques can be investigated.

Because of lack of enough source in the PLD, just binary values of the parameters can be shown over the LCD. For a investigation, with a more powerful PLD, binary to decimal conversions can be realized before sending the data to LCD.

More features as full bridge topology control, RS-232 V.28 interface to PC and some application program that can be run over the PC, can be realized. So user can control the device over the PC. If such a system can be established, parametric sweep of a system can be realized in real world. A more realistic look to gain curve of the system, poles of the system, minimum bandwidth of the system, open circuit and short circuit performance of the system, and performance of the designed transformer at all possible working condition can easily be observed over a PC. This provides a big progress in SMPS design duration and provides more comprehensive tests with your system. As a result you will take more reliable systems in shorter times.

REFERENCES

Adragna, C. (1998). *Minimize Power Losses of Lightly loaded Flyback Converters With The L5991 PWM Controller.* ST Electronics. Retrieved April 10, 2012, from http://www.eetasia.com/ARTICLES/2000JUN/2000JUN15_AMD_AN3.PDF?SOURCES=DOWNLOAD

Altera (2008). *My first FPGA design tutorial.* Retrieved April 18, 2011, from http://www.altera.com/literature/tt/tt_my_first_fpga.pdf

Altium (2008). *FPGA design basics.* Retrieved April 12, 2011, from http://www.altium.com/community/trainingcenter/en/training-manuals.cfm

Bay, Ö.F. & Atacak, I. (2005). Power Factor Correction of a Switching Mode Power Supply by Using Neuro-fuzzy Controller. *Gazi University-Journal of Science, 18*. pp. 3-6.

Brown, S & Rose, J. (2004). *Architecture of FPGAs and CPLDs: A Tutorial.University of Toronto.* Retrieved February 14,2012 from http://www.eecg.toronto.edu/~jayar/pubs/brown/survey.pdf

Brown, A. & Vranesic, A. (1999). *VHDL Reference*. Retrieved May 12, 2012, from http://www.scribd.com/doc/38047023/VHDL-Reference

Choudhury, J. (2004). Efficient encoding scheme for ultra-fast flash ADC. Silicon Monolithic Integrated Circuits in RF systems, *2004 Topical Meeting on September 2004*, pp. 290-293.

Colorado University (2012). *The Flyback Converter. ECEN4517 Lecture notes.* Retrieved April 10, 2012, from http://ecee.colorado.edu/~ecen4517/materials/flyback.pdf

Counsil, J.A.(2000). *Switching Power Supply Tutorial*. Retrieved April 10, 2012, from http://www.rollanet.org/~rrars/switch.pdf

Erickson,R.,W.& Maksimović,D. (2001). *Fundamentals of Power Electronics.* NewYork: Kluwer Academic Puplishers

Gray , N. (2006). *ABCs of ADCs. National Semiconductor Application Notes.*

Guo, S. (2009). *High Performance Digital Controller for High-Frequency Low-Power Integrated DC/DC SMPS.* Retrieved August 30, 2011, from http://theses.insa-lyon.fr/publication/2009ISAL0033/these.pdf

Hagen, M. & Yousefzadeh, V. (2008). Applying Digital Technology to PWM Control Loop Designs. *Texas Instruments 2008/09 Power Supply Design Seminar*, SEM1800 , pp. 7-11.

Kenia, M., V. (2004). *Development of an Isolated Flyback Converter Employing Boundary-Mode Operation and Magnetic Flux Sensing Feedback*. Thesis of EEE of MIT. Massachutes: Massachutes Institute of Technology. Retrieved April 10, 2012, from http://dspace.mit.edu/bitstream/handle/1721.1/28415/56986239.pdf?sequence=1

Kharagpur, (2010). *Lesson 21-Introduction to Switched-Mode Power Supply (SMPS) Circuits. Version 2 EE IIT.* Retrieved February 18, 2012 from http://ecourses.vtu.ac.in/nptel/courses/Webcoursecontents/IIT%20Kharagpur/Power%20Electronics/PDF/L21%28DP%29%28PE%29%20%28%28EE%29NPTEL%29.pdf

Lidak, P. (1998).*Critical Conduction Mode, Flyback Switching Power Supply using MC33364.* Motorola Semiconductor Application Note, AN1594.

Mortezapour, S. (2000). 1-V, 8-Bit Successive Approximation ADC in Standard CMOS Process. IEEE Journal of Solid State Circuits (2000) Volume: 35, Issue: 4, Publisher, pp. 642-646.

Nakamura, K. (1995). An 85 mW, 10 b, 40 Msample/s CMOS Parallel-Pipelined ADC. IEEE Journal of Solid-State Circuits, Vol. 30, No. 3, pp. 173 - 183.

National Semiconductor. (2010). *Flyback Converter*. Retrieved April 10, 2012, from http://www.national.com/AU/design/courses/292/292_flyback_converter.pdf

Rozenblat, L. (2012). *Switching mode power supplies, Overview, Comparison and Selection Guide.* Retrieved April 10, 2012, from http://www.smps.us/topologies.html

Senouci, A. (2008). *Mentor Graphics*. Retrieved April 12, 2012, from http://130.203.133.150/viewdoc/summary;jsessionid=DCD6890497433BEAFD257BD27BF57978?doi=10.1.1.186.1627

Wikipedia (2012). *Programmable Logic Device*. Retrieved March 12, 2012, from http://en.wikipedia.org/wiki/Programmable_logic_device

Wuidart, L. (1999). *AN513/0393. ST Electronics*. Retrieved April 10, 2012, Retrieved April 10, 2012, from http://www.st.com/internet/com/TECHNICAL_RESOURCES/TECHNICAL_LITERATURE/APPLICATION_NOTE/CD00003910.pdf

Yousefzadeh,V.&Choudhury,S.(2008). Nonlinear Digital PID Controller for DC-DC Converters. *Applied Power Electronics Conference and Exposition, 2008*. APEC 2008. Twenty-Third Annual IEEE. 24-28 February, 2008, Retrieved from http://ieeexplore.ieee.org/xpl/login.jsp?tp=&arnumber=4522956&url=http%3A%2F%2Fieeexplore.ieee.org%2Fiel5%2F4510696%2F4522647%2F04522956.pdf

Zeidman, B.(2012). *Introduction to CPLD and FPGA Design*. Retrieved May 2, " http://independent.academia.edu/BobZeidman/Papers/1112903/Introduction_to_CPLD_and_FPGA_Design

Zhao, Z. & Prodic,A. (2007). *Continuous-Time Digital Controller for High-Frequency DC-DC Converter*. Thesis Archive of University of Toronto. Retrieved from http://energy.ele.utoronto.ca/~prodic/JP13.pdf

Xilinx (2012). *What is Programmable Logic?* Retrieved May 7, 2012, from http://www.xilinx.com/company/about/programmable.html

APPENDIXIES

1. Schematic of SMPS Transformer Test Device

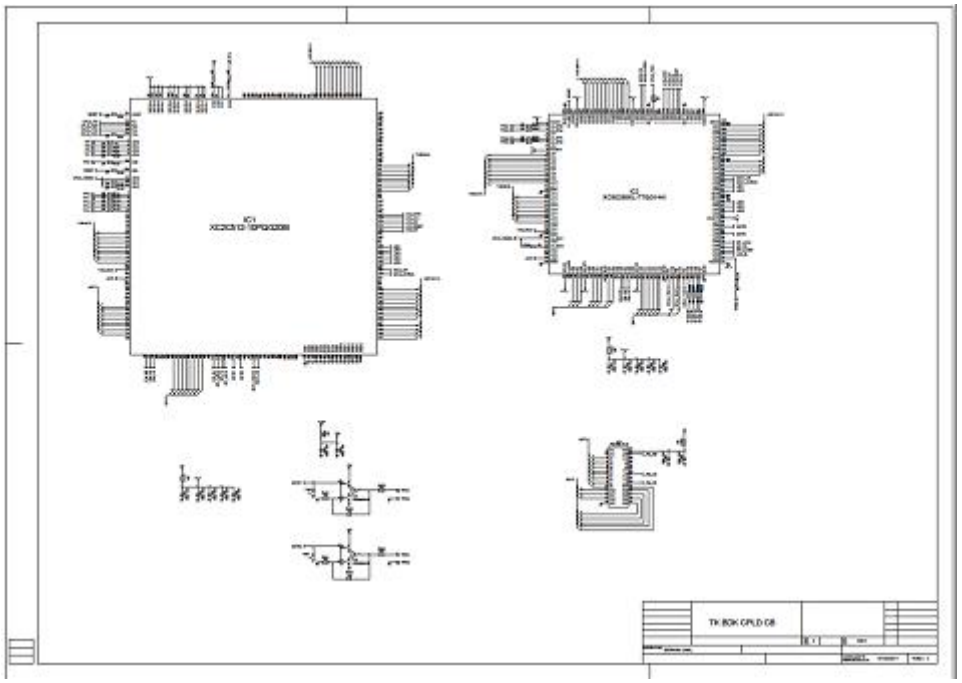


Figure A.1 Schematic of SMPS Transformer Test Device, 1. page

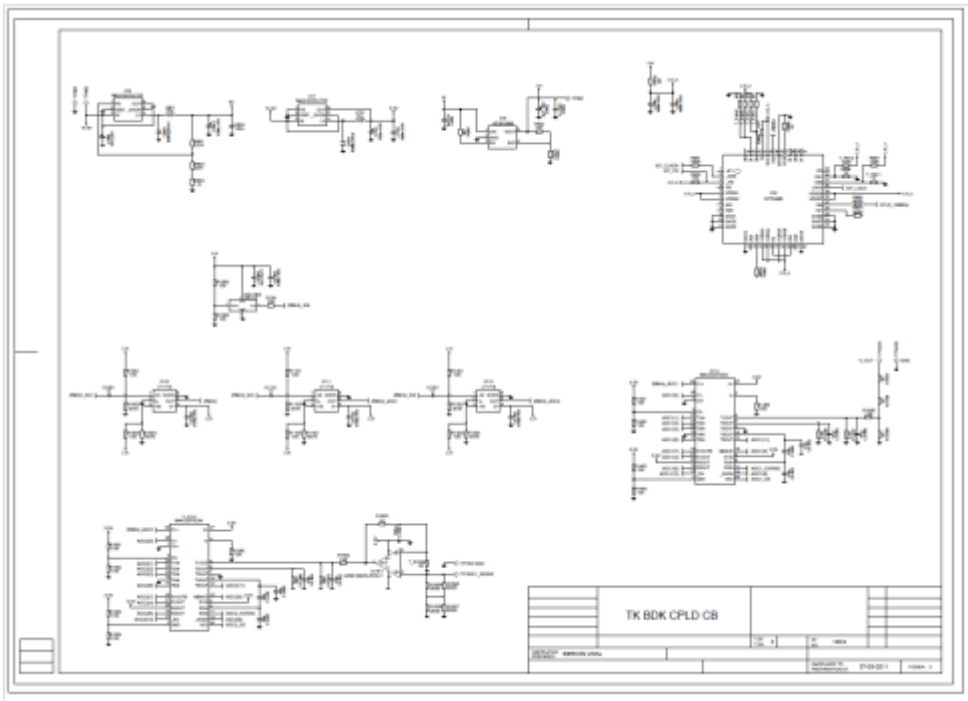


Figure A.2 Schematic of SMPS Transformer Test Device, 2. page

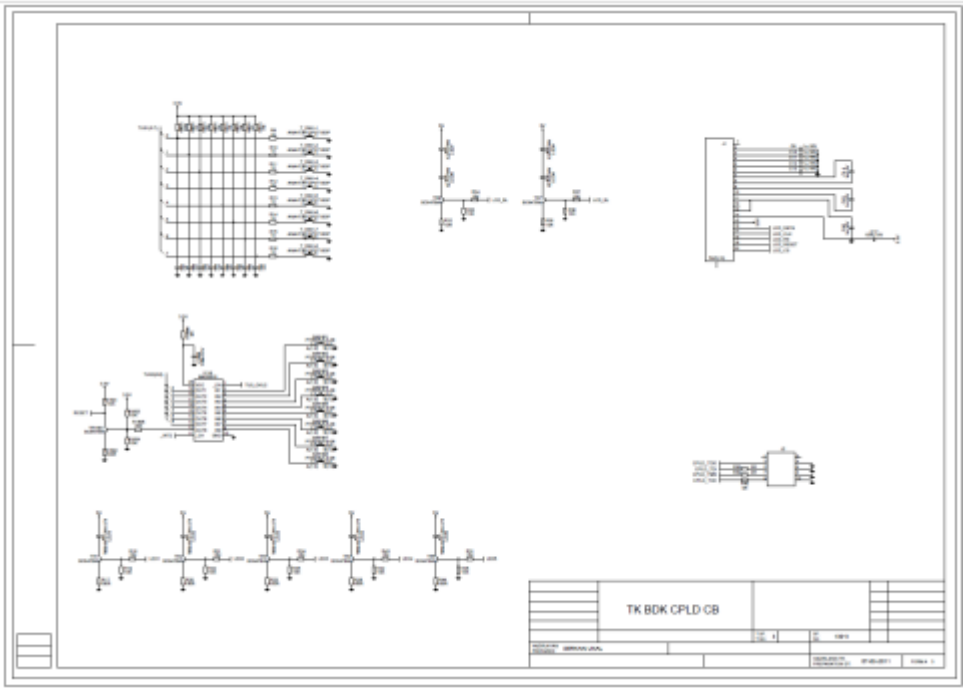


Figure A.3 Schematic of SMPS Transformer Test Device, 3. page

2. Mechanic Drawings of SMPS Transformer Test Device

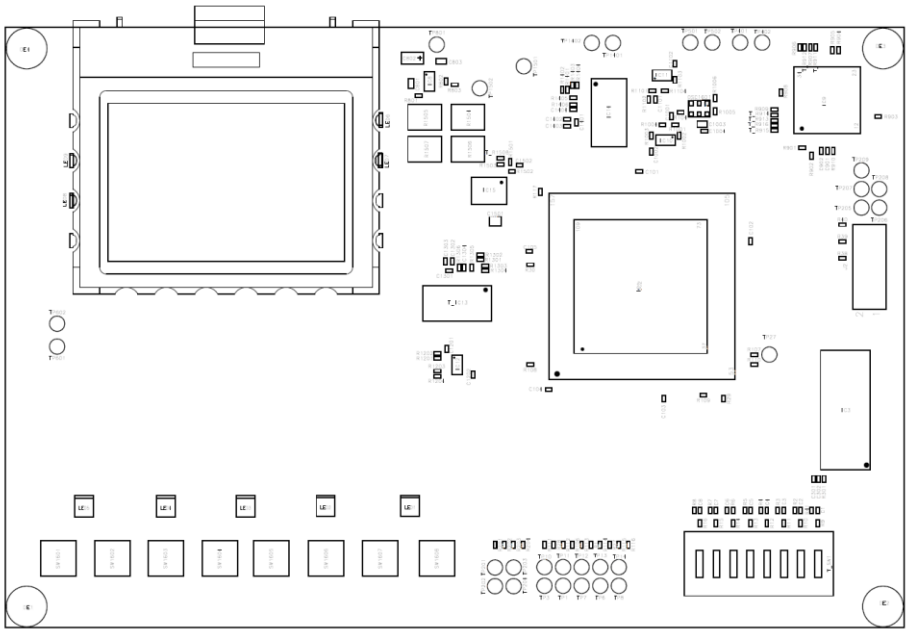


Figure A.4 Mechanic Drawings of SMPS Transformer Test Device, top side

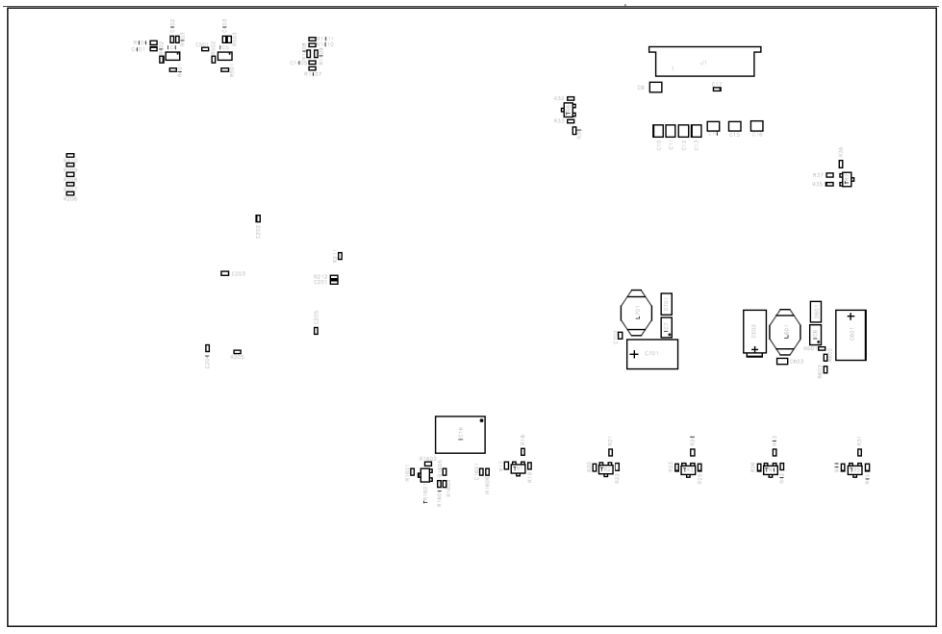


Figure A.4 Mechanic Drawings of SMPS Transformer Test Device, bottom side

3. S6B0724 LCD Controller Instruction Table

×: Don't care

Instruction	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
Display ON / OFF	0	0	1	0	1	0	1	1	1	DON	Turn on/off LCD panel When DON = 0: display OFF When DON = 1: display ON
Initial display line	0	0	0	1	ST5	ST4	ST3	ST2	ST1	ST0	Specify DDRAM line for COM0
Set page address	0	0	1	0	1	1	P3	P2	P1	P0	Set page address
Set column address MSB	0	0	0	0	0	1	Y7	Y6	Y5	Y4	Set column address MSB
Set column address LSB	0	0	0	0	0	0	Y3	Y2	Y1	Y0	Set column address LSB
Read status	0	1	BUSY	ADC	ONOFF	RESETB	0	0	0	0	Read the internal status
Write display data	1	0	Write data								Write data into DDRAM
Read display data	1	1	Read data								Read data from DDRAM
ADC select	0	0	1	0	1	0	0	0	0	ADC	Select SEG output direction When ADC = 0: normal direction (SEG0→SEG131) When ADC = 1: reverse direction (SEG131→SEG0)
Reverse display ON / OFF	0	0	1	0	1	0	0	1	1	REV	Select normal / reverse display When REV = 0: normal display When REV = 1: reverse display
Entire display ON / OFF	0	0	1	0	1	0	0	1	0	EON	Select normal/entire display ON When EON = 0: normal display. When EON = 1: entire display ON
LCD bias select	0	0	1	0	1	0	0	0	1	BIAS	Select LCD bias
Set modify-read	0	0	1	1	1	0	0	0	0	0	Set modify-read mode
Reset modify-read	0	0	1	1	1	0	1	1	1	0	release modify-read mode
Reset	0	0	1	1	1	0	0	0	1	0	Initialize the internal functions
SHL select	0	0	1	1	0	0	SHL	×	×	×	Select COM output direction When SHL = 0: normal direction (COM0→COM63) When SHL = 1: reverse direction (COM63→COM0)
Power control	0	0	0	0	1	0	1	VC	VR	VF	Control power circuit operation
Regulator resistor select	0	0	0	0	1	0	0	R2	R1	R0	Select internal resistance ratio of the regulator resistor
Set reference voltage mode	0	0	1	0	0	0	0	0	0	1	Set reference voltage mode
Set reference voltage register	0	0	×	×	SV5	SV4	SV3	SV2	SV1	SV0	Set reference voltage register
Set static indicator mode	0	0	1	0	1	0	1	1	0	SM	Set static indicator mode
Set static indicator register	0	0	×	×	×	×	×	×	S1	S0	Set static indicator register
Power save	-	-	-	-	-	-	-	-	-	-	Compound Instruction of display OFF and entire display ON

4. Glossary of Terms

ADC – Analog-to-Digital Converter. A device or circuit used to convert analog information to digital words.

BOM – Bill of Material.

CPLD – Complex Programmable Logic Device.

DAC – Digital-to-Analog Converter. A device or circuit used to convert digital words into analog voltages or currents.

DPWM – Digital Pulse Width Modulation.

DSP – Digital Signal Processor.

EEPROM – Electrically Erasable Programmable Read Only Memory.

ENOB – Effective Number Of Bits. A specification that helps to quantify dynamic performance of an ADC.

EMI/RFI – Electromagnetic Interference/Radio Frequency Interference. This is the radiation of EM (electromagnetic) energy that may interfere with other circuits and systems.

EPLD – Erasable Programmable Logic Device.

EPROM – Electrically Programmable Read Only Memory.

FPD – Field-Programmable Device.

FRAM – Ferroelectric Random-Access Memory.

FPGA –Field-Programmable Gate Array.

GAL – Generic Array Logic.

LCD – Liquid Crystal Display.

LSB – Least Significant Bit. The bit that has the least weight.

MOSFET – Metal–Oxide–Semiconductor Field-Effect Transistor.

MPGA – Mask-Programmable Gate Arrays.

NRE costs – Non-Recurring Engineering costs. Refers to the one-time cost to research, develop, design and test a new product.

PAL – Programmable Array Logic.

PCB – Printed Circuit Board.

PIC – Peripheral Interface Controller.

PID – Proportional/Integral/Derivative control.

PFC – Power Factor Correction.

PLD – Programmable Logic Device.

PROM – Programmable Read-Only Memory.

PSRR – Power Supply Rejection Ratio. A measure of how well a circuit rejects a signal on its power supply.

PWM – Pulse Width Modulation.

Skin Effect – The phenomenon by which high frequency current flow is restricted to the surface, or skin, of a conductor.

SMPS – Switch Mode Power Supply.

SRAM – Static Random-Access Memory.

THD – Total Harmonic Distortion.