DOKUZ EYLÜL UNIVERSITY
GRADUATE SCHOOL OF NATURAL AND APPLIED SCIENCES

ANALOG CIRCUIT DESIGN USING CURRENT MODE ACTIVE ELEMENTS

by
Hasan SÖZEN

January, 2012
İZMİR

ANALOG CIRCUIT DESIGN USING CURRENT MODE ACTIVE ELEMENTS

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M. Sc. THESIS EXAMINATION RESULT FORM

We have read the thesis entitled **"ANALOG CIRCUIT DESIGN USING CURRENT MODE ACTIVE ELEMENTS"** completed by **HASAN SÖZEN** under supervision of **ASSIST. PROF. DR. SELÇUK KILINÇ** and we certify that in our opinion it is fully adequate, in scope and in quality, as a thesis for the degree of Master of Science.

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Hasan SÖZEN

ANALOG CIRCUIT DESIGN USING CURRENT MODE ACTIVE ELEMENTS

ABSTRACT

Design of high frequency and low voltage circuits is one of the most important issues in many analog signal processing systems. The classical operational amplifier suffers from limited gain-bandwidth product and low slew rate, and hence fails to respond to these necessities. In order to correspond to the demands for high frequency and low voltage operation in analog circuits, designers have made plenty of attempts. Among these is the current mode approach. In the past years, current mode active elements have begun to receive a great interest as new alternatives. Current mode circuits have been receiving considerable attention due to their potential advantages such as inherently wide bandwidth, higher slew rate, wider dynamic range, simpler circuitry, low voltage operation and low power consumption. In this thesis, analog circuit design using current mode active elements is investigated. New applications of inverting second generation current conveyor (ICCII), and inverting current feedback operational amplifier (ICFOA), both of which can be considered as current mode active elements, are presented. First order all-pass filter, second order filter and oscillator circuits using these elements are given. CMOS realizations for the newly introduced ICFOA and its application are included. The workability of the circuits is verified using PSPICE simulations.

Keywords: analog circuit design, integrated circuits, current mode active elements, inverting second generation current conveyors, inverting current feedback operational amplifiers

AKIM MODLU AKTİF ELEMANLAR KULLANARAK ANALOG DEVRE TASARIMI

ÖZ

Yüksek frekans ve düşük voltajlı devrelerin tasarımı birçok analog sinyal işleme sistemlerinde en önemli konulardan biridir. Klasik işlemsel kuvvetlendirici sınırlı kazanç - bant genişliği çarpımı ve düşük yükselme oranına maruz kalmakta ve dolayısıyla bu gereksinimlere cevap verememektedir. Analog devrelerdeki yüksek frekans ve düşük voltaj çalışma taleplerini karşılamak için, tasarımcılar birçok girişimde bulunmuştur. Bunların içinde akım modlu yaklaşım vardır. Geçmiş yıllarda, akım modlu aktif elemanlar yeni alternatifler olarak büyük ilgi görmüşlerdir. Akım modlu devreler, kendiliğinden geniş bant aralığı, daha büyük yükselme oranı, daha geniş dinamik aralığı, daha basit devre yapısı, düşük voltajda çalışmaları ve düşük güç tüketimi gibi potansiyel avantajlarından dolayı önemli ölçüde ilgi görmektedirler. Bu tezde, akım modlu aktif elemanlar kullanılarak analog devre tasarımı incelenmiştir. Akım modlu aktif eleman olarak değerlendirilebilen eviren ikinci kuşak akım taşıyıcı (ICCII) ve eviren akım geri-beslemeli işlemsel kuvvetlendiricinin (ICFOA) yeni uygulamaları sunulmuştur. Bu elemanları kullanan birinci derece tüm-geçiren süzgeç, ikinci derecede süzgeç ve osilatör devreleri verilmiştir. Yeni ileri sürülen ICFOA'nın CMOS gerçeklemeleri ve uygulaması dahil edilmiştir. Devrelerin çalışabilirliği PSPICE simülasyonları kullanılarak doğrulanmıştır.

Anahtar Kelimeler: analog devre tasarımı, tümdevreler, akım modlu aktif elemanlar, eviren ikinci kuşak akım taşıyıcılar, eviren akım geri-beslemeli işlemsel kuvvetlendiriciler

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CHAPTER ONE
INTRODUCTION

The classical operational amplifier (op-amp) suffers from limited gain-bandwidth product problems and from low slew rate at its output. The limited gain-bandwidth product of the op-amp affects the parameters of the circuits. Therefore, it remains unsatisfactory at higher frequencies (Budak, 1974).

The current mode approach is one of the attempts which have been made in order to correspond to the demands for high frequency and low power supply voltage operation in analog circuits. To achieve high performance analog circuits in CMOS technology, signals have been represented with current instead of voltage. One of the most promising solutions to high frequency and low voltage operation is thought to be current signal processing (Takagi, 2001). By this approach, current mode circuits began to receive a great attention as a new alternative to voltage mode circuits. A current mode circuit may be taken to mean any circuit in which current is used as the active variable in preference to voltage, either throughout the whole circuit or only in certain critical areas (Wilson, 1990).

Current mode circuits have been receiving considerable attention due to their potential advantages such as inherently wide bandwidth, higher slew rate, wider dynamic range, simpler circuitry, low voltage operation and low power consumption (Toumazou, Lidjey & Haigh, 1990). Furthermore, current mode circuits are suitable for integration with CMOS technology and thus have become more and more attractive in electronic circuit design in recent years (Toker, Kuntman, Çiçekoğlu & Dişçigil, 2002).

In the past, analog circuit design using current mode active elements have been exploited in a very wide range of application areas. This trend might be thought to be started by the invention of the current conveyors. These elements are considered to be the alternatives of classical op-amps to be used in analog electronic circuits. To overcome the certain limitations of the op-amp in analog circuits, many

new building blocks that are suitable for current mode circuits have been introduced. Among these current conveyors are very famous.

The first generation current conveyor (CCI) was introduced as a new circuit building block by Smith & Sedra in 1968 (Smith & Sedra, 1968). Two years later, the second generation current conveyor (CCII) and its applications were presented by the same authors (Sedra & Smith, 1970). The third generation current conveyor, which corrects the mistake in the current sensing function of the CCI, was proposed by Fabre in 1995 (Fabre, 1995). Afterwards, many derivatives of current conveyors have been proposed in the literature. These include inverting second generation current conveyor (ICCII) (Awad & Soliman, 1999), differential voltage current conveyor (DVCC) (Elwan & Soliman, 1997), differential difference current conveyor (DDCC) (Chiu, Liu, Tsao & Chen, 1996), modified current conveyor, dual output current conveyor, multiple output current conveyor, etc. There are many filter and oscillator applications of these building blocks reported in scientific journals and symposium proceedings (Chen, 2009; Ibrahim, Kuntman, Ozcan, Suvak & Cicekoglu, 2004; Ibrahim, Minaei & Kuntman, 2006; Soliman, 2010a, 2010b; Özoğuz, Toker & Çiçekoğlu, 2000). Some of these circuits are current mode meaning that the signal of interest is in current form. Actually, the family of current conveyors is more suitable for implementing current mode transfer functions. On the other hand, these active elements have also been used for voltage mode circuits. Later, the CCII element has been modified to have another output port with low output impedance, which is suitable for taking out voltage signals. The resulting element is called current feedback operational amplifier (CFOA). It is more convenient for implementing voltage transfer functions.

One important element within the derivatives of current conveyors is the ICCII. This building block could especially be useful in the synthesis of all-pass and notch filters due to the relationship between its input terminals. As oppose to the CCII element, the input ports of ICCII are at the opposite potentials. This feature makes it possible to have a minus sign in the numerator of the resulting transfer function. In order to have more proper active element for voltage mode applications, the idea

used for implementing the classical CFOA can be used in such a way that the high impedance output terminal of ICCII is buffered to obtain another output terminal. We call this element as inverting current feedback operational amplifier (ICFOA) and introduce it as a new active building block.

In this thesis, analog circuit design using current mode active elements is investigated. New applications of ICCII and ICFOA, both of which can be considered as current mode active elements, are presented. The employed active elements are described in Chapter 2. First order all-pass filter and oscillator circuits using ICCII are presented in Chapter 3. CMOS realizations for newly introduced ICFOA element and its application are included in Chapter 4. The functionality of the proposed circuits is tested using PSPICE program. Conclusions are drawn in Chapter 5.

CHAPTER TWO
CURRENT MODE ACTIVE ELEMENTS

2.1 Current Conveyors

A.S. Sedra, under the supervision of Prof. K.C. Smith, began to work on a thesis project; its goal was the design of programmable instrument for incorporation in a system for computer controlled experiments. For this project a voltage controlled waveform generator had to be designed. He designed a circuit, but the control variable was current, not a voltage as required. So there was a problem to solve. He had to convert voltage to current. At that time the known solution was to use a grounded base PNP transistor and connect its emitter via a resistor to the control voltage. But this simple voltage to current convertor has some problems due to the transistor's V_{EB}. The variation of V_{EB} makes the control characteristic nonlinear and a lateral shift in frequency-voltage characteristic of the waveform. To create a better voltage to current converter, a more complex circuit had been designed. This circuit has five transistors as connected in Figure 2.1 (Sedra, Roberts & Gohh, 1990).

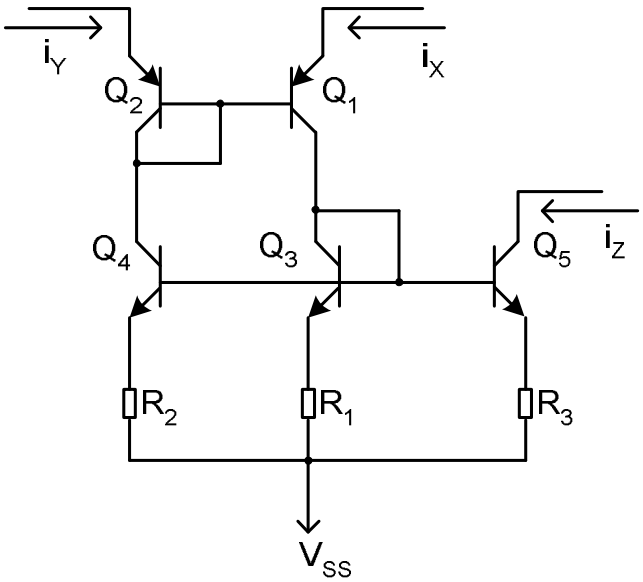

Figure 2.1 Voltage to current convertor (Sedra, Roberts & Gohh, 1990).

In this figure, Q_1 is the current source transistor and its emitter was connected via a resistor to control voltage. Q_2 transistor is the compensating diode-connected transistor and its emitter was connected to ground. Transistors Q_3, Q_4 and Q_5 form a current mirror with two outputs. In this circuit, Q_1 and Q_2 form a current mirror. Therefore, a current that equals to emitter current of Q_1 transistor is provided to Q_2 transistor and V_{EB} voltage values for these transistors become equal. So the voltage at the emitter of Q_1 becomes equal to zero. The mirror supplies an equal current at the collector of Q_5 at a high impedance level. This circuit provides a nice solution to the problem of creating a precise voltage to current convertor (Sedra, Roberts & Gohh, 1990).

In February 1968, A.S. Sedra attended the International Solid-State Circuit Conference in Philadelphia and inspired by two papers which were presented by Barrie Gilbert and G. Wilson. Barrie Gilbert's paper includes a technique, which has become a classic, for wideband amplification of current signals. G. Wilson's paper includes a novel current mirror configuration, now known as Wilson current mirror (Sedra, Roberts & Gohh, 1990).

In the voltage to current convertor circuit in Figure 2.1, Y need not to be grounded but can be connected to a voltage V_Y. Then an equal voltage would appear at X independent of the current supplied to X. Thus this circuit exhibits a virtual short circuit at X. Moreover, current flowing through Y equals to the current supplied to X independent of V_Y. Thus this circuit exhibits a virtual open circuit at Y. Finally, the current supplied to X is conveyed to the output terminal Z where the impedance level is very high. So the circuit shown in Figure 2.1 can be thought as a realization of a three port network that named as CCI as shown in Figure 2.2. This three port relation can be expressed by the following matrix representation:

$$\begin{bmatrix} I_y \\ V_x \\ I_z \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} V_y \\ I_x \\ V_z \end{bmatrix} \tag{2.1}$$

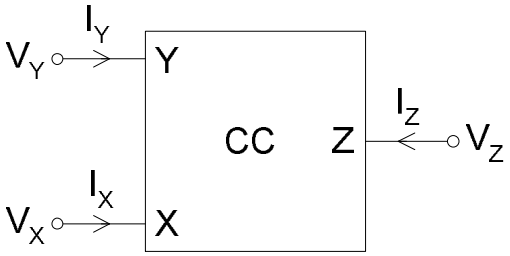

Figure 2.2 Black box representation of the current conveyor.

To imagine the relations of the port voltages and currents described above, the nullator-norator representation shown in Figure 2.3 can be used. In this figure, the single ellipse represents the norator element and has constitutive equations V=0, I=0. Double ellipses represent the nullator element and have an arbitrary voltage-current relationship. The dependent current sources are used to convey the current at port X to port Y and Z (Sedra, Roberts & Gohh, 1990).

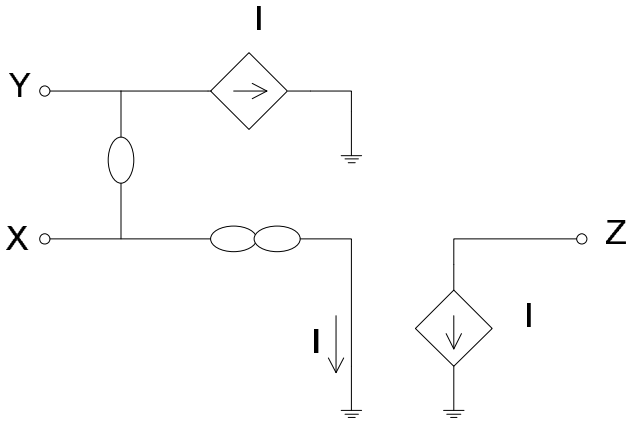

Figure 2.3 Nullator-norator representation of CCI (Sedra, Roberts & Gohh, 1990).

The performance of the circuit realization for CCI in Figure 2.1 can be improved by using more complex current mirrors. Furthermore, the polarity of the current which conveyed to high impedance output Z, can be inverted by an additional current mirror stage.

In 1960s, CCI could not be produced in IC form due to its high quality PNP devices. A CMOS current conveyor shown in Figure 2.4 was fabricated due to complementary devices were available in CMOS technology (Sedra, Roberts & Gohh, 1990).

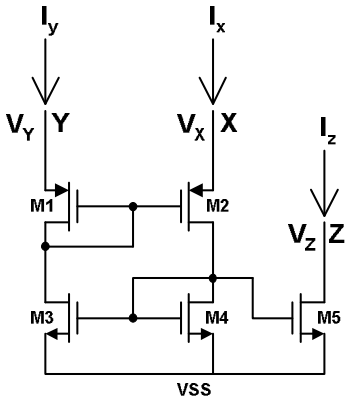

Figure 2.4 First order CMOS implementation of CCI (Sedra, Roberts & Gohh, 1990).

An early application for the current conveyor was using it as an oscilloscope current probe based on the Hall-effect to measure the current on the line. For this application the circuit must be broken to insert the Y and X terminals of current conveyor to measure the current. In this application very impressive result had taken. The frequency range of operation extending from DC to 100MHz was measured and the input impedance was less than 1Ω. Another early application of the CCI was its use as a negative impedance converter as shown in Figure 2.5 and Figure 2.6. For these applications terminal Z is grounded and the resistor to be converted is connected either between X and ground or between Y and ground. If a resistor connected between X and ground the input impedance looking into Y is a negative impedance value of the connected impedance between X and ground. On the other hand if a resistor connected between Y and ground the input impedance looking into X is a negative impedance value of the connected impedance between Y and ground (Sedra, Roberts & Gohh, 1990).

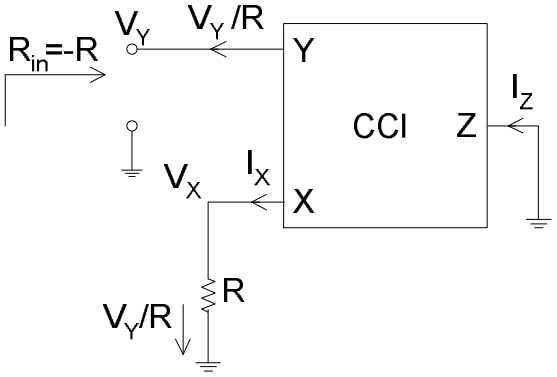

Figure 2.5 CCI implementation of a negative impedance converter (Sedra, Roberts & Gohh, 1990).

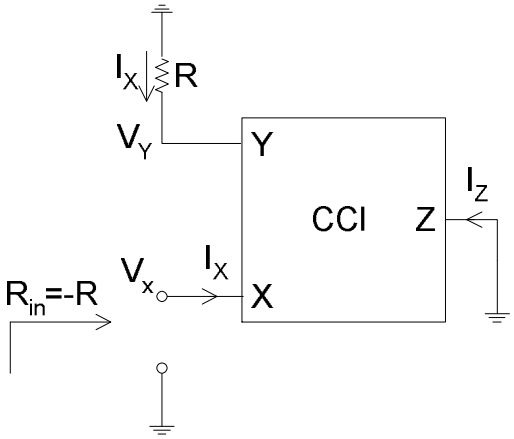

Figure 2.6 CCI implementation of a negative impedance converter (Sedra, Roberts & Gohh, 1990).

CCII was designed to increase the versatility of CCI in 1970. In this new version current conveyor, current does not flow in terminal Y. This new version current conveyor introduced at first at IEEE International Symposium on Circuit Theory in 1970 (Sedra & Smith, 1970). This building block has since proven to be more useful than CCI. The black box representation can be shown as in Figure 2.2 like CCI. The terminal behavior of CCII can be described by the following matrix representation:

$$\begin{bmatrix} I_y \\ V_x \\ I_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_y \\ I_x \\ V_z \end{bmatrix} \tag{2.2}$$

It is clear from the matrix equation given above that terminal Y exhibits infinite input impedance. The voltage at terminal X follows the voltage applied to terminal Y. The current supplied to terminal X is conveyed to terminal Z, which has high impedance. In the above equation the plus (+) and minus (–) signs shows the polarity of the current at terminal Z. For plus (+) sign the current conveyor is represented as CCII+ and for minus (–) sign the current conveyor is represented as CCII–. The nullor-norator representation of CCII can be shown as in Figure 2.7 (Sedra, Roberts & Gohh, 1990).

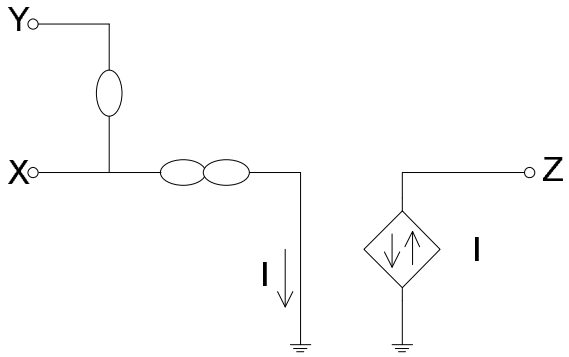

Figure 2.7 Nullor-norator representation of CCIIs (Sedra, Roberts & Gohh, 1990).

The similarity and difference between CCI and CCII nullor-norator representation is that: The nullor-norator representation of CCII has bidirectional dependent current source to represent the polarity of the current at terminal Z and the dependent current source which shows the current in terminal Y does not exist in nullor-norator representation for CCII owing to no current flows through terminal Y. In the case of a CCII–, the dependent current source is redundant. The current flowing into terminal X must flow out of terminal Z. Therefore the nullor-norator representation for CCII– can be shown as in Figure 2.8 (Sedra, Roberts & Gohh, 1990).

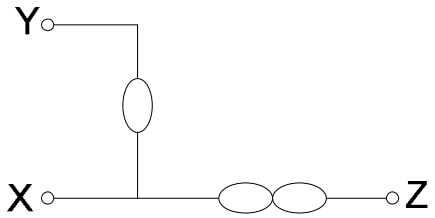

Figure 2.8 Nullor-norator representation of CCII– (Sedra, Roberts & Gohh, 1990).

The inventors of the current conveyors attempted to interest Microsystems International Limited in the current conveyor with no success. So their attention was directed to devising CCII realization by op-amps. Their view was that, due to the op-amp is a voltage mode device, it is not the most convenient for realizing CCII. Then a lot of implementations for CCII have been reported. Some of these utilize op-amps alone, others utilize IC op-amps together with BJT IC arrays, and others yet utilize CMOS technology, resulting in fully integrated conveyors. Also several bipolar realizations for CCII– have been reported. CCII can be thought as a bipolar or MOS. NMOS transistor and a CCII– can be compared as shown in Figure 2.9. When the NMOS transistor is ideal, its V_{GS} voltage value would approach to zero. Hence, if a voltage is applied to the gate, this would result in an equal voltage at the source. While the gate terminal would approximate an open circuit as the conveyor terminal Y, the source terminal would exhibit zero input impedance as the conveyor terminal X. In ideal behavior of NMOS, when a current is applied to the source, this current will be conveyed to the drain, impedance of which approaches to infinite. This operation is the same as the CCII– (Sedra, Roberts & Gohh, 1990).

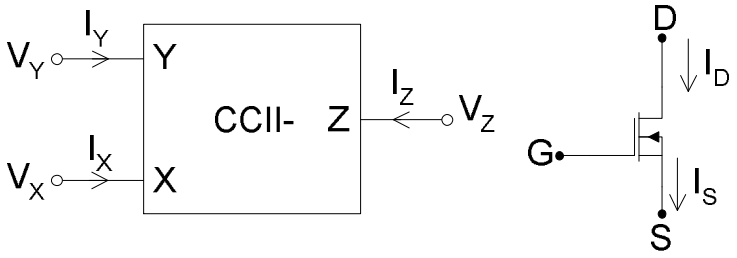

Figure 2.9 Comparison of CCII– and NMOS transistor (Sedra, Roberts & Gohh, 1990).

To improve the ideality of the NMOS that has been shown in Figure 2.9, the NMOS transistor can be placed in negative feedback loop of an op-amp as shown in Figure 2.10. This structure results better performance than the one in Figure 2.9 (Sedra, Roberts & Gohh, 1990).

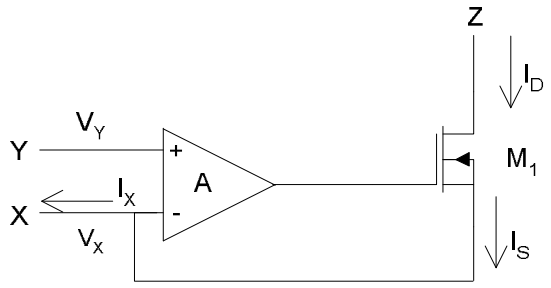

Figure 2.10 CCII– using a super-transistor (Sedra, Roberts & Gohh, 1990).

It is obvious from Figure 2.10 that the current flows out of terminal X. An alternative realization for CCII– can be made by replacing the NMOS by a PMOS transistor, which allows the current flowing into terminal X. Hence a bidirectional current flow can be obtained by connecting complementary MOS transistor in the negative feedback loop of an op-amp as shown in Figure 2.11. This structure is CCII+. To obtain CCII– two additional current mirrors have to be included as shown in Figure 2.12 (Sedra, Roberts & Gohh, 1990).

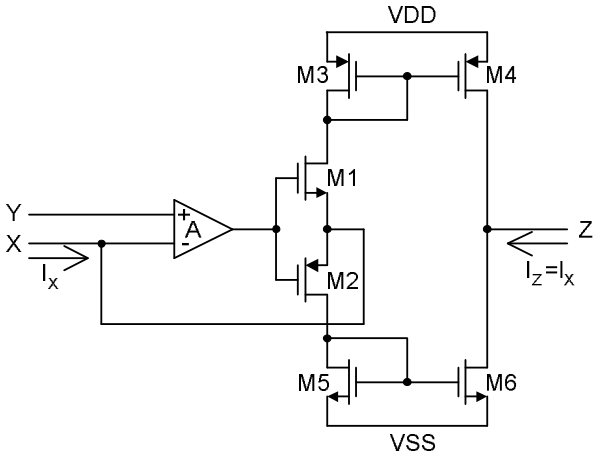

Figure 2.11 CCII+ using complementary MOS (Sedra, Roberts & Gohh, 1990).

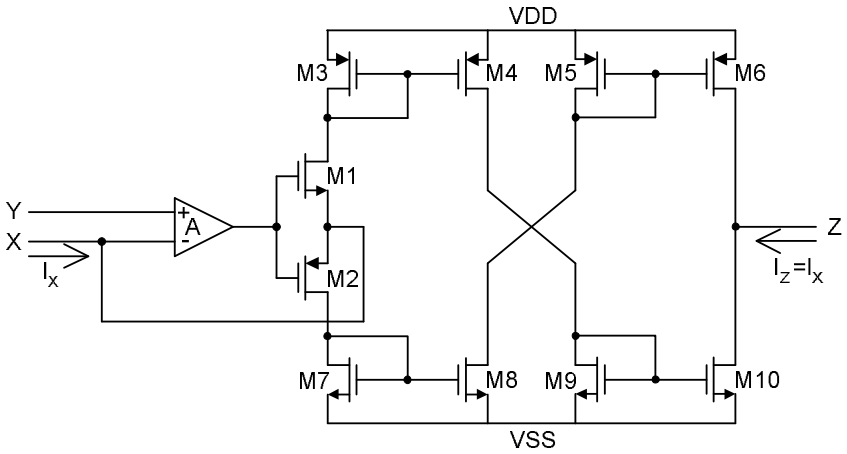

Figure 2.12 CCII– using complementary MOS (Sedra, Roberts & Gohh, 1990).

2.2 Inverting Second Generation Current Conveyor (ICCII)

Sedra and Smith have defined only two types of CCII in 1970 and these types of CCII can be described as combined voltage follower and current follower. The missing two types of CCII family ICCII+ and ICCII– have been defined according to polarity of the voltage follower as an adjoint of CCII (Awad & Soliman, 1999). The circuit symbol of ICCII element is shown in Figure 2.13. The terminal behaviors of the positive type ICCII are given by the following set of equations.

$$\begin{aligned} I_Y &= 0 \\ V_X &= -V_Y \\ I_Z &= I_X \end{aligned} \tag{2.3}$$

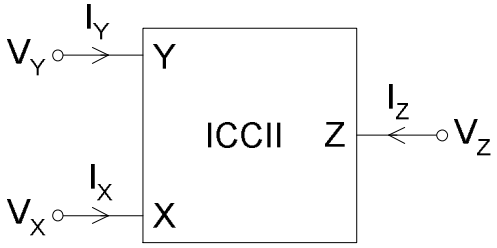

Figure 2.13 Circuit symbol of ICCII.

ICCII+ and ICCII– can be illustrated by their mirror and nullor-mirror representation as shown in Figure 2.14 and Figure 2.15 respectively (Awad & Soliman, 1999). The current mode circuits which are obtained from their voltage mode counterparts after replacing each building block with its adjoint and then interchanging the excitation and the response can be designed by utilizing adjoint theorem (Roberts & Sedra, 1989). A CMOS realization for ICCII– is given in Figure 2.16 (Awad & Soliman, 1999).

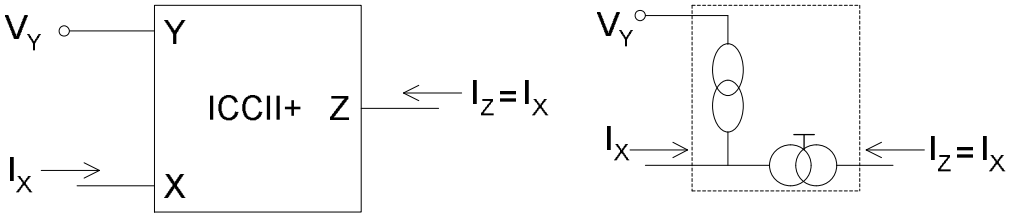

Figure 2.14 Circuit symbol of ICCII+ and its mirror representation (Awad & Soliman, 1999).

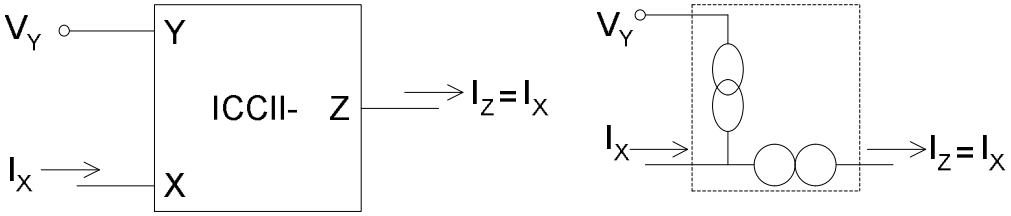

Figure 2.15 Circuit symbol of ICCII- and its nullor-mirror representation (Awad & Soliman, 1999).

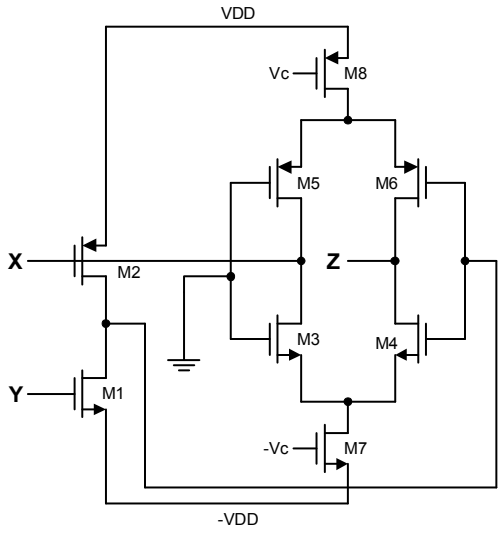

Figure 2.16 The ICCII– CMOS realization (Awad & Soliman, 1999).

The ideal model of ICCII element can be given as in Figure 2.17. The port relations in Equation (2.3) are provided by the dependent current sources.

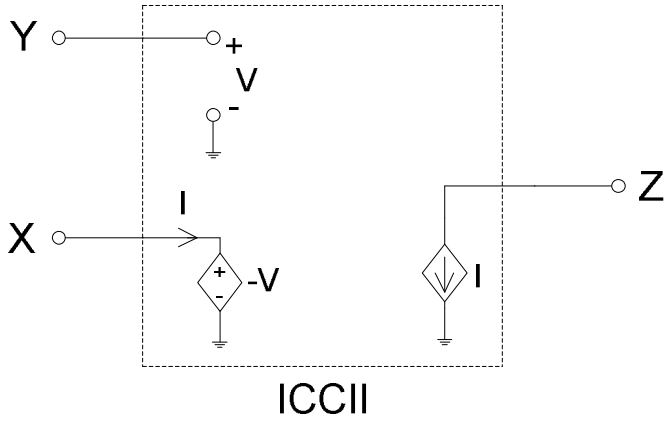

Figure 2.17 Ideal model of ICCII.

2.3 Inverting Current Feedback Operational Amplifier (ICFOA)

The CCII element has been widely used in the field of analog signal processing since its discovery. Many CCII based configurations synthesizing voltage mode and current mode filtering functions have been presented in the literature (Toumazou, Lidjey & Haigh, 1990; Chen, 2010). Due to its high-impedance output terminal, CCII is more convenient for current mode filters although it has also found applications in voltage mode circuits. Afterwards, another output terminal has been added to this element which is obtained by voltage buffering the high-impedance output terminal. The resulting active element has been called as CFOA. The CFOA has also found many applications (Soliman, 1996) and it has been manufactured commercially, e.g. Analog Devices' AD844 (AD844 Datasheet, n.d.). It can also be used as a classical op-amp with the advantage of constant gain-bandwidth product. Its low-impedance output terminal gives the possibility to cascade voltage mode circuits.

On the other hand, the ICCII element has been introduced to give further possibilities to the analog designers (Awad & Soliman, 1999). Its only difference from CCII is that the input terminals are at opposite potentials. This feature can

especially be useful in the synthesis of all-pass and notch filters. Some applications of ICCII have been reported in the literature (Ibrahim, et al., 2004; Soliman, 2008). As with CCII, it is not very suitable for voltage mode circuits due to the absence of low-impedance output terminal. The proposed new active building block, called ICFOA, is obtained by adding another output terminal to the ICCII with voltage buffering the high-impedance output terminal as it is done for the classical CFOA (Sözen & Kılınç, 2011).

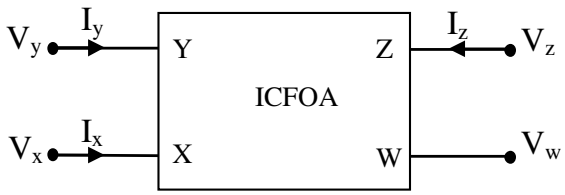

Figure 2.18 Circuit symbol of ICFOA.

The circuit symbol of ICFOA is given in Figure 2.18. Its port relations are defined by the following set of equations

$$\begin{aligned} I_y &= 0 \\ V_x &= -V_y \\ I_z &= \pm I_x \\ V_w &= V_z \end{aligned} \tag{2.7}$$

where the positive sign in $I_z = \pm I_x$ indicates the positive type inverting current feedback operational amplifier (ICFOA+) and the negative sign indicates the negative type inverting current feedback operational amplifier (ICFOA–).

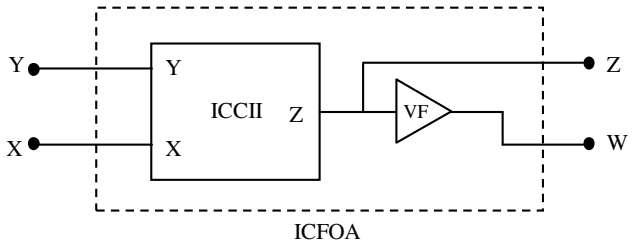

Figure 2.19 Implementation of ICFOA using an ICCII and a voltage follower (VF).

ICFOA can be obtained from ICCII by connecting a voltage follower as shown in Figure 2.19. Therefore, the CMOS realization of ICFOA can be constructed using a CMOS ICCII as a core followed by a CMOS voltage buffer. There are several different ways of implementing ICCII in CMOS presented in the literature (Awad & Soliman, 1999; Sobhy & Soliman, 2007). Furthermore, DVCC and DDCC elements can also be used as ICCII by grounding the appropriate Y terminals (Chiu, et al., 1996; Elwan & Soliman, 1997). A CMOS voltage buffer, e.g. in Manetakis & Toumazou (1996), can be connected to the output terminal of ICCII to complete the CMOS realization of ICFOA. Ideal model of ICFOA can be given as in Figure 2.20. The port relations in Equation (2.7) are provided by the dependent current sources.

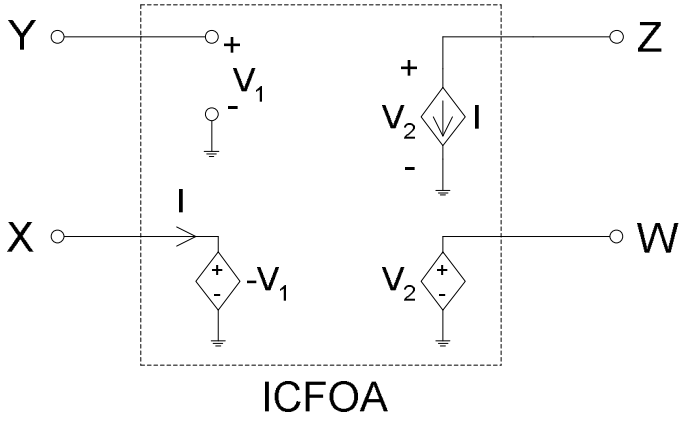

Figure 2.20 Ideal model of ICFOA.

CHAPTER THREE
ANALOG CIRCUIT DESIGN USING ICCII

3.1 ICCII Based First Order All-pass Filters

All-pass filters are important parts of many electronic circuits and systems. They are generally used for introducing a frequency dependent delay while keeping the amplitude of the input signal constant over the desired frequency range (Schaumann & VanValkenburg, 2001; Öztayfun, Kılınç, Çelebi & Çam, 2008). Other types of active circuits such as quadrature oscillators and high-Q band-pass filters are also realized by using all-pass filters (Schaumann & VanValkenburg, 2001; Toker, Özoğuz, Çiçekoğlu & Acar, 2000). Many first order all-pass filter realizations using different active building blocks have been reported in the literature (Öztayfun, et al., 2008; Toker, et al., 2000; Çiçekoğlu, Kuntman & Berk, 1999). On the other hand, the ICCII has been introduced as a new active element to give further possibilities to the analog designers (Awad & Soliman, 1999). Some ICCII based circuits are reported in the literature (Awad & Soliman, 1999; Minaei, Yuce, Cicekoglu, 2006; Soliman, 2008; Ibrahim et al., 2004; Chen, Lin & Yang, 2006; Özoğuz, Toker & Çiçekoğlu, 2000). It has few applications to the realization of first order all-pass filters (Ibrahim, et al., 2004; Chen, Lin & Yang, 2006; Özoğuz, Toker & Çiçekoğlu, 2000). In Ibrahim et al. (2004), four different voltage mode all-pass filters have been presented. Chen, Lin & Yang (2006) has introduced an ICCII based configuration which provides both inverting and non-inverting first order all-pass filtering functions simultaneously from the same topology (Chen, Lin & Yang, 2006). First order all-pass sections employing ICCIIs have been used for the synthesis of a current mode universal filter in Özoğuz, Toker & Çiçekoğlu (2000). None of these filters contain a grounded capacitor. In this section, an ICCII based configuration, which realizes six different first order all-pass filters, is presented. All realizations are canonic since they include only one capacitor as a dynamical element. One of them is especially advantageous as it employs a grounded capacitor. The functionality of the circuits has been shown by simulation and experimental results.

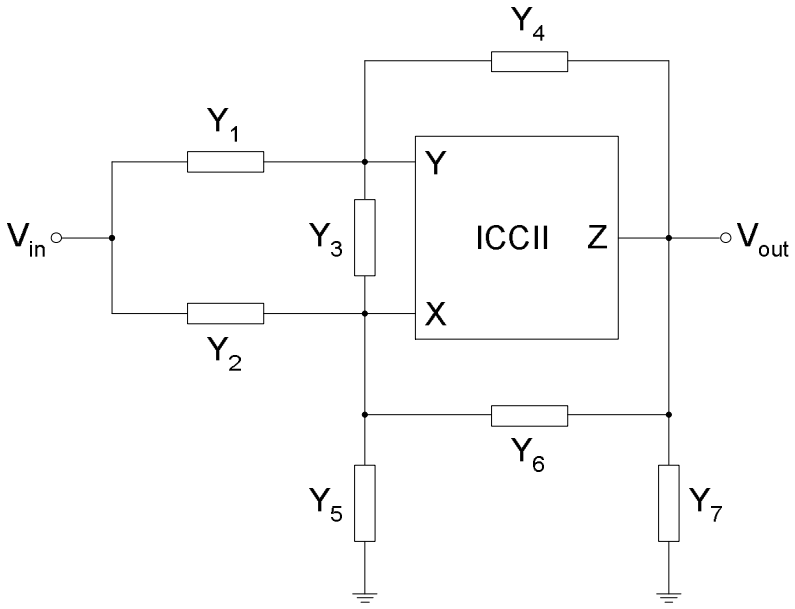

Figure 3.1 Filter configuration.

The configuration to be used in the synthesis of the first order all-pass filters is given in Figure 3.1 (Sözen & Kılınç, 2012). Routine analysis of this configuration yields the following transfer function

$$\frac{V_{out}}{V_{in}} = -\frac{Y_2(Y_1 + 2Y_3 + Y_4) + Y_1(Y_2 + 2Y_3 - Y_4 + Y_5 + 2Y_6)}{(Y_4 + 2Y_6 + Y_7)(Y_1 + 2Y_3 + Y_4) + Y_4(Y_2 + 2Y_3 - Y_4 + Y_5 + 2Y_6)} \tag{3.1}$$

Using various combinations for the admittances (Y's), six different first order all-pass filters can be obtained from this configuration as given in Table 3.1. The first two filters (circuits 1 and 2) correspond to the ones presented in Ibrahim, et al. (2004). Transfer function for the circuits 1-to-4 is

$$T_1(s) = \frac{V_{out}}{V_{in}} = \frac{s - \frac{1}{RC}}{s + \frac{1}{RC}} \tag{3.2}$$

and their phase relation can be given by

$$\varphi_1(\omega) = 180° - 2\arctan(\omega RC) \tag{3.3}$$

The remaining two filters, i.e. circuits 5 and 6, have the following transfer function

$$T_2(s) = \frac{V_{out}}{V_{in}} = -\frac{s - \frac{1}{RC}}{s + \frac{1}{RC}} \tag{3.4}$$

and phase relation

$$\varphi_2(\omega) = -2\arctan(\omega RC) \tag{3.5}$$

Therefore, both inverting and non-inverting types of first order all-pass filters can be realized with the configuration of Figure 3.1. The only one that contains a grounded capacitor is the circuit 5 in Table 3.1.

Table 3.1 Admittance combinations for the realization of the first order all-pass filters (Sözen & Kılınç, 2012)

Circuit No	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7
1	sC	1/R	0	∞	0	0	0
2	∞	0	0	sC	0	1/(2R)	0
3	∞	0	0	sC	1/R	0	1/R
4	∞	1/(2R)	0	sC	0	0	1/R
5	1/R	0	0	1/R	sC	0	0
6	2/R	0	sC/2	1/R	0	0	0

If the non-idealities for voltage and current tracking errors β and α respectively of ICCII (i.e. $I_Y=0$, $V_X=-\beta V_Y$, $I_Z=\alpha I_X$) are taken account for Figure 3.1, its transfer function becomes

$$\frac{V_{out}}{V_{in}} = \frac{Y_1Y_4 - \alpha\left(Y_2(Y_1+Y_3+Y_4)+Y_1Y_3\right) - \alpha\beta(Y_2Y_3+Y_1(Y_2+Y_3+Y_5+Y_6)) - \beta(Y_1Y_6)}{Y_4(Y_6+Y_7)+\alpha\left(Y_6(Y_1+Y_3+Y_4)+Y_3Y_4\right)+\alpha\beta\left(Y_3Y_6+Y_4(Y_2+Y_3+Y_5+Y_6\right) + \beta\left(Y_3(Y_4+Y_6+Y_7)+Y_4Y_6\right)+(Y_1+Y_3)(Y_4+Y_6+Y_7)} \quad (3.6)$$

Transfer functions and phase relations for the circuits including non-idealities are shown as in Table 3.2 and Table 3.3 respectively.

Table 3.2 Transfer functions for non-ideal case

Circuit No	Transfer Functions
1	$T_1(s) = \dfrac{s-\alpha\dfrac{1}{RC}}{s+\alpha\beta\dfrac{1}{RC}}$
2	$T_2(s) = \dfrac{s-(\beta+\alpha\beta)\dfrac{1}{2RC}}{s+(1+\alpha)\dfrac{1}{2RC}}$
3	$T_3(s) = \dfrac{s-\alpha\beta\dfrac{1}{RC}}{s+\dfrac{1}{RC}}$
4	$T_4(s) = \dfrac{s-(\alpha+\alpha\beta)\dfrac{1}{2RC}}{s+\dfrac{1}{RC}}$
5	$T_5(s) = -\dfrac{s-\dfrac{1}{\alpha\beta RC}}{s+\dfrac{1}{\alpha\beta RC}}$
6	$T_6(s) = -\dfrac{s-\dfrac{2}{RC(\alpha+\alpha\beta)}}{s+\dfrac{4}{RC(\alpha+\alpha\beta+\beta+1)}}$

Table 3.3 Phase relations for non-ideal case

Circuit No	Phase Relations
1	$\varphi_1(\omega) = 180° - arctan\left(\frac{\omega RC}{\alpha\beta}\right) - \arctan\left(\frac{\omega RC}{\alpha}\right)$
2	$\varphi_2(\omega) = 180° - arctan\left(\frac{2\omega RC}{1+\alpha}\right) - \arctan\left(\frac{2\omega RC}{\alpha\beta+\beta}\right)$
3	$\varphi_3(\omega) = 180° - arctan\left(\omega RC\right) - \arctan\left(\frac{\omega RC}{\alpha\beta}\right)$
4	$\varphi_4(\omega) = 180° - arctan\left(\omega RC\right) - \arctan\left(\frac{2\omega RC}{\alpha+\alpha\beta}\right)$
5	$\varphi_5(\omega) = -2\,arctan\left(\omega\alpha\beta RC\right)$
6	$\varphi_6(\omega) = -arctan\left(\frac{\omega RC(\alpha+\alpha\beta+\beta+1)}{4}\right) - \arctan\left(\frac{\omega RC(\alpha+\alpha\beta)}{2}\right)$

If the non-idealities for parasitic admittances, which exist in practice, are taken into account, filter configuration of Figure 3.1 can be shown as in Figure 3.2. Its transfer function becomes

$$\frac{V_{out}}{V_{in}} = \frac{\begin{array}{l}(Y_1(G_X - Y_4)((Y_2 + Y_3 + Y_5 + Y_6 + sC_X + G_X)(Y_1 + Y_3 + Y_4 + sC_Y + G_Y) \\ + Y_3(G_X - Y_3)) - (Y_1(G_X - Y_3) - Y_2(Y_1 + Y_3 + Y_4 + sC_Y + G_Y))((G_X - Y_6) \\ (Y_1 + Y_3 + Y_4 + sC_Y + G_Y) + Y_3(G_X - Y_4)))\end{array}}{\begin{array}{l}((Y_4(G_X - Y_3) - Y_6(Y_1 + Y_3 + Y_4 + sC_Y + G_Y))((G_X - Y_6) \\ (Y_1 + Y_3 + Y_4 + sC_Y + G_Y) + Y_3(G_X - Y_4)) \\ - ((Y_2 + Y_3 + Y_5 + Y_6 + sC_X + G_X)(Y_1 + Y_3 + Y_4 + sC_Y + G_Y) + Y_3(G_X - Y_3)) \\ (Y_4(G_X - Y_4) + (Y_4 + Y_6 + Y_7 + sC_Z + G_Z)(Y_1 + Y_3 + Y_4 + sC_Y + G_Y)))\end{array}} \quad (3.7)$$

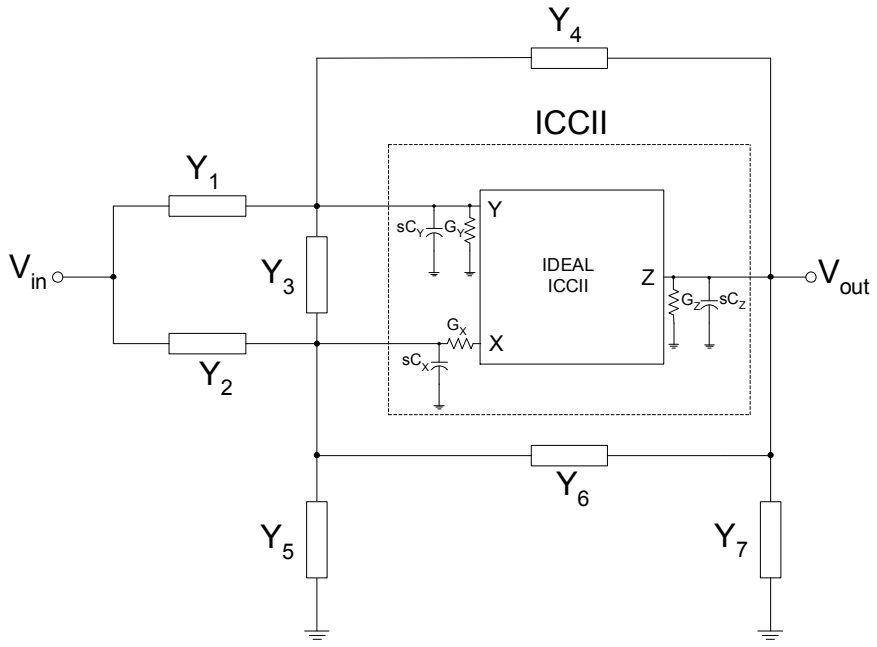

Figure 3.2 Filter configuration including parasitic admittances.

Transfer functions for the circuits 1-to-6 in Table 3.1 with parasitic admittances can be given by the following equations.

$$T_1 = \frac{s^2 CC_X + s[C(G+G_X)] - GG_X}{\begin{aligned} &s^2[C_X(C+C_Y+C_Z)] + s[C_X(G_X+G_Y+G_Z) + (G+G_X)(C+C_Y+C_Z)] \\ &+ G(G_X+G_Y+G_Z) + G_X(G_Y+G_Z) \end{aligned}} \tag{3.8}$$

$$T_2 = \frac{s^2 CC_X + s[C(G_X+\frac{G}{2}) - C_X G_X] - GG_X}{\begin{aligned} &s^2[C_X(C+C_Z)] + s[\frac{G}{2}(C+C_X+C_Z) + G_X(C+C_Z) + C_X G_Z] \\ &+ G_X(G+G_Z) + G_Z\frac{G}{2} \end{aligned}} \tag{3.9}$$

$$T_3 = \frac{s^2 CC_X + s[C(G+G_X) - C_X G_X] - GG_X}{\begin{aligned} &s^2[C_X(C+C_Z)] + s[C_X(G+G_Z) + (C+C_Z)(G+G_X)] \\ &+ G_X(G+G_Z) + G(G+G_Z) \end{aligned}} \tag{3.10}$$

$$T_4 = \frac{s^2 CC_X + s[C(\frac{G}{2} + G_X) - C_X G_X] - GG_X}{s^2[C_X(C + C_Z)] + s[C_X(G + G_Z) + (C + C_Z)(\frac{G}{2} + G_X)] + (\frac{G}{2} + G_X)(G + G_Z)} \tag{3.11}$$

$$T_5 = -\frac{G[s(C + C_X)(G_X - G) - GG_X]}{\begin{aligned} &s^3(C + C_X)C_Y C_Z + s^2[C_Z(C + C_X)(2G + G_Y) + C_Y((C + C_X)(G + G_Z) \\ &+ C_Z G_X)] + s[(C + C_X)(G^2 + G_Y(G + G_Z) + G(G_X + 2G_Z)) \\ &+ C_Z G_X(2G + G_Y) + C_Y G_X(G + G_Z)] + G_X[G(G + 2G_Z) + G_Y(G + G_Z)] \end{aligned}} \tag{3.12}$$

$$T_6 = -\frac{2G[sC_X(G_X - G) + sC(G_X - \frac{G}{2}) - GG_X]}{\begin{aligned} &s^3[\frac{CC_Z}{2}(C_X + C_Y) + C_X C_Y C_Z] + s^2[C_X C_Z(3G + G_Y) \\ &+ C_X C_Y(G + G_Z) + (C(C_X + C_Y))(\frac{G}{2} + \frac{G_Z}{2}) \\ &+ CC_Z(\frac{3G}{2} + \frac{G_Y}{2} + G_X) + C_Y C_Z G_X] \\ &+ s[C_X(G_Y G_Z + G(2G + G_X + G_Y + 3G_Z)) \\ &+ C(G(\frac{3G_Z}{2} + \frac{G_Y}{2} + G) + G_X(2G + G_Z) + \frac{G_Y G_Z}{2}) \\ &+ C_Z G_X(3G + G_Y) + C_Y G_X(G + G_Z)] \\ &+ G_X G_Y(G + G_Z) + GG_X(2G + 3G_Z) \end{aligned}} \tag{3.13}$$

The first order all-pass filter has been simulated using PSPICE program. In the simulation, the CMOS realization of ICCII presented in Ibrahim & Kuntman (2002), has been used together with 0.35µm CMOS process parameters. Supply voltages were taken as ±2.5V. In the simulation, circuit 5 that has been given in Table 3.1, is used as all-pass filter. Simulated magnitude and phase responses of the first order all-pass filter are shown in Figure 3.3. We used R=1kΩ and C=100pF as the passive element values. Simulation results give the natural frequency as 1.58MHz, which is very close to the theoretical one (1.59MHz).

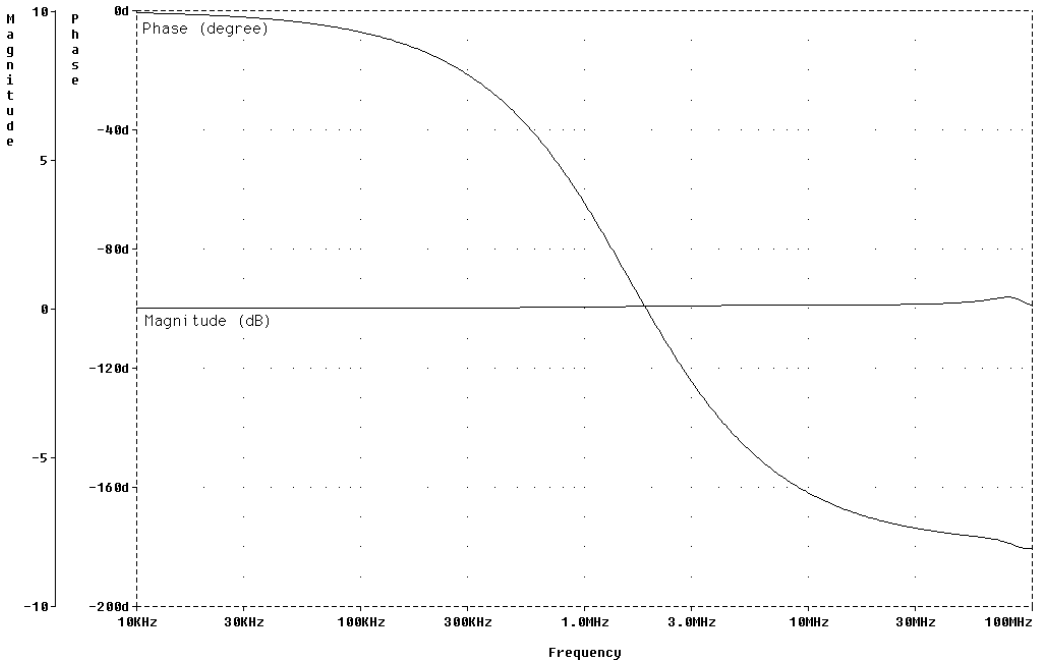

Figure 3.3 Simulated magnitude and phase responses of the first order all-pass filter.

The first order all-pass filter has also been tested experimentally. ICCII element has been implemented using Analog Devices' AD844 integrated circuit as shown in Figure 3.4. Supply voltages were taken as ±5V. Buffered output of the AD844 has been used for the cascade connection in the experimental setup of the quadrature oscillator. In the experiments, all resistor and capacitor values were taken as 1kΩ and 10nF, respectively. Figure 3.5 shows the input (1V peak, 50kHz) and output waveforms of the first order all-pass filter. As it is expected, the output waveform has been shifted by −145.5 degrees (theoretically −144.7 degrees) while keeping the amplitude almost unchanged.

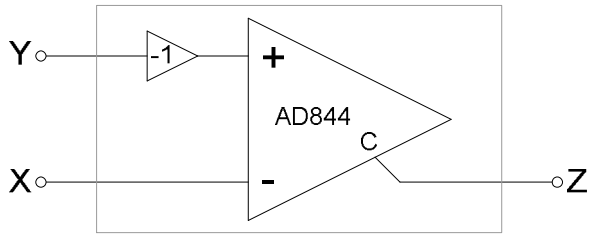

Figure 3.4 Implementation of ICCII.

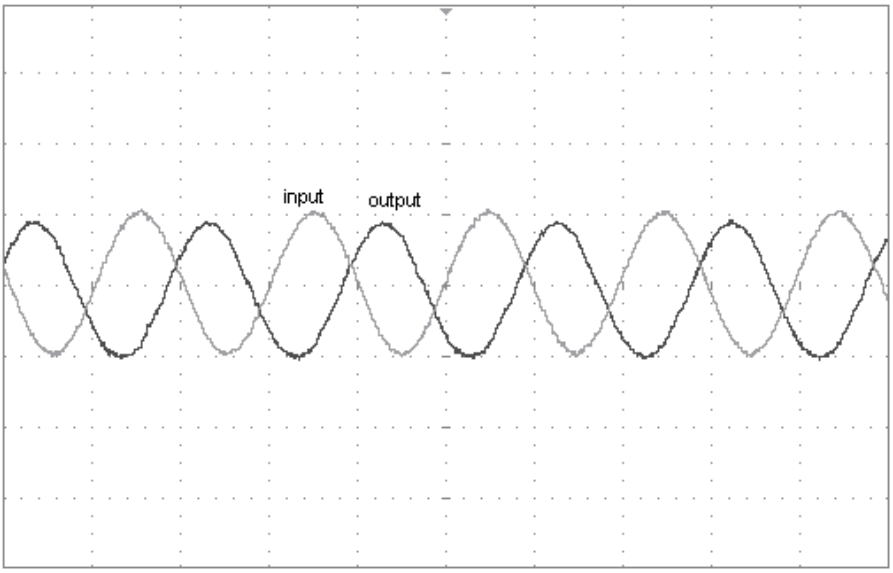

Figure 3.5 Experimental waveforms of the all-pass filter (Volt/Div=1V, Time/Div=10μs).

3.2 ICCII Based Quadrature Oscillator

It is a well-known fact that a sinusoidal quadrature oscillator can be realized using an all-pass section and an integrator (Haritantis, 1985) as shown in Figure 3.6. Using this block diagram, ICCII based quadrature oscillator can be implemented. To this end, the presented first order all-pass filter circuit 5 which has been given in Table 3.1 and an ICCII based integrator, which can be realized by the circuit of Figure 3.7, are used together with voltage buffers for cascade connection. For providing a sinusoidal oscillation, the loop gain of the circuit is set to unity at $s = j\omega$, i.e.

$$\left[-\frac{s-1/(R_1C_1)}{s+1/(R_1C_1)}\right]\left[-\frac{1}{sR_2C_2}\right]\Bigg|_{s=j\omega} = 1 \qquad (3.14)$$

From Equation (3.14) oscillation condition and frequency can be found respectively as

$$R_1C_1 = R_2C_2 \qquad (3.15)$$

$$\omega_0 = \sqrt{\frac{1}{R_1 C_1 R_2 C_2}} \tag{3.16}$$

For simplicity, if we choose $R_1 = R_2 = R$ and $C_1 = C_2 = C$, oscillation condition is satisfied and oscillation frequency becomes

$$\omega_0 = \frac{1}{RC} \tag{3.17}$$

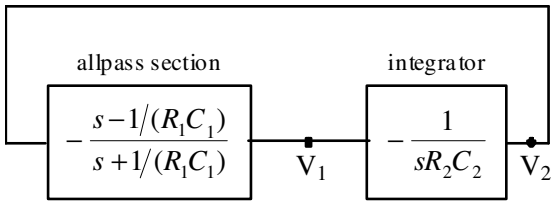

Figure 3.6 Block diagram for quadrature oscillator.

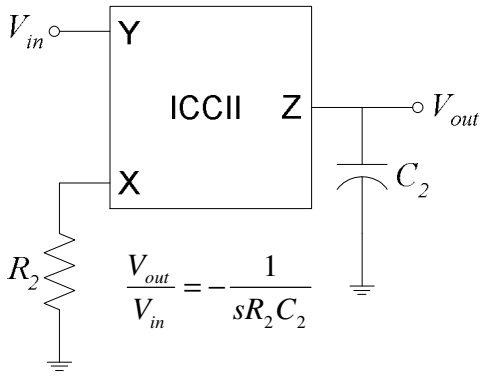

Figure 3.7 ICCII based integrator circuit.

The quadrature oscillator has also been simulated using PSPICE program. The simulated output waveforms of the quadrature oscillator are shown in Figure 3.8 where all resistor and capacitor values were taken as 1kΩ and 100pF, respectively. They oscillate at a frequency of 1.57MHz which is again near to the theoretical oscillation frequency (1.59MHz).

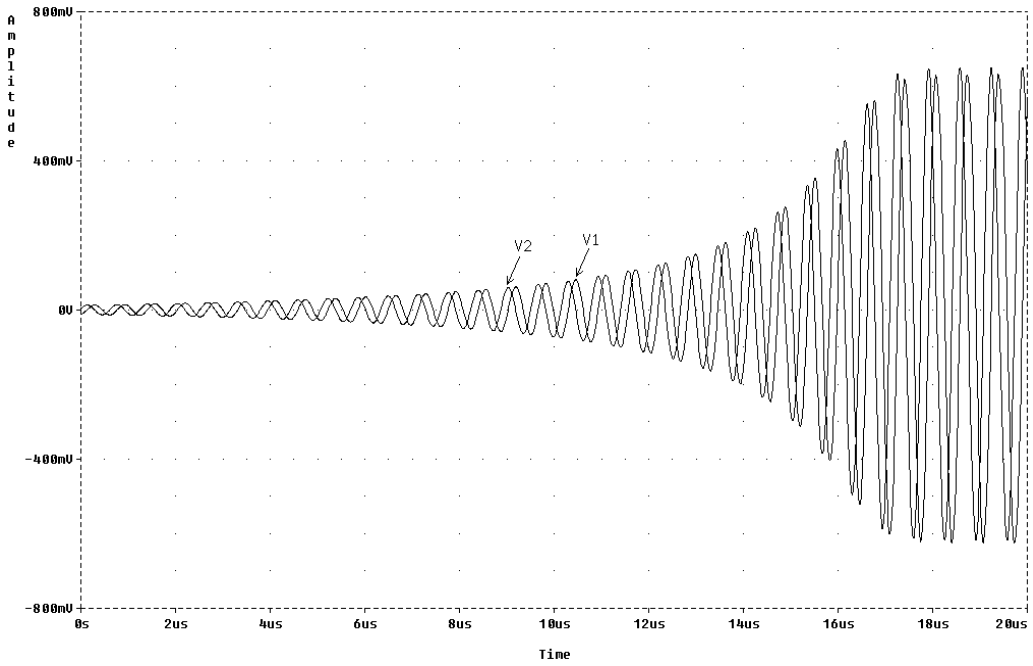

Figure 3.8 Simulated waveforms of the quadrature oscillator.

The quadrature oscillator has also been tested experimentally using the AD844 implementation of the ICCII element. Figure 3.9 shows the experimental waveforms of the quadrature oscillator. They oscillate at a frequency of 16.3kHz (theoretical one is 15.9kHz) with 90 degrees phase difference between them.

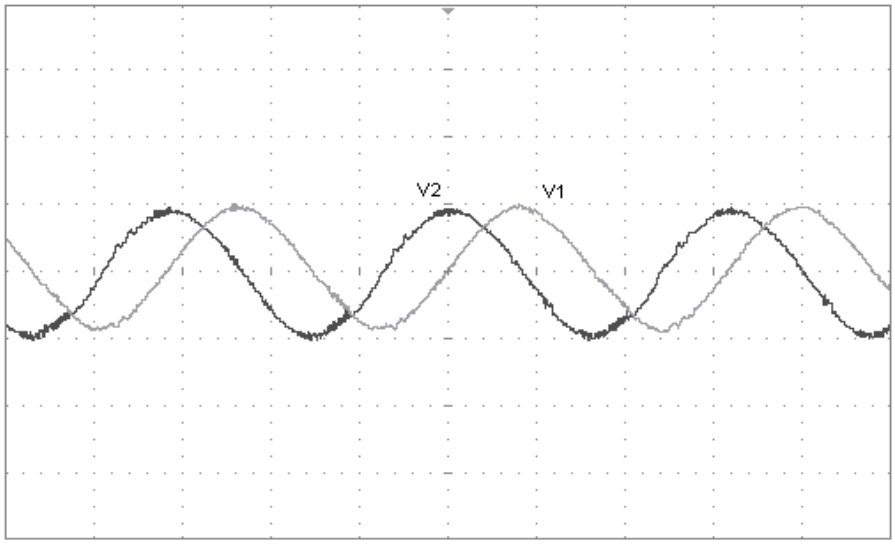

Figure 3.9 Experimental waveforms of the oscillator (Volt/Div=1V, Time/Div=20μs).

CHAPTER FOUR
ANALOG CIRCUIT DESIGN USING ICFOA

4.1 CMOS Realizations of ICFOA

In this section, the proposed CMOS realizations for ICFOA element are given.

4.1.1 The First CMOS ICFOA+ Design

A CMOS realization of ICFOA+ is shown in Figure 4.1. It is obtained by cascading the DDCC based ICCII in Ibrahim & Kuntman (2002), (with grounded Y_1 and Y_3 terminals) and the buffer in Manetakis & Toumazou (1996). The performance of the proposed CMOS realization is simulated using SPICE program with 0.35µm MOSIS CMOS process parameters. The aspect ratios of the MOS transistor in the circuit are given in Table 4.1. The supply voltages (VDD, VSS) are taken as ±2.5V and bias voltage is VB=–1.7V (Sözen & Kılınç, 2011).

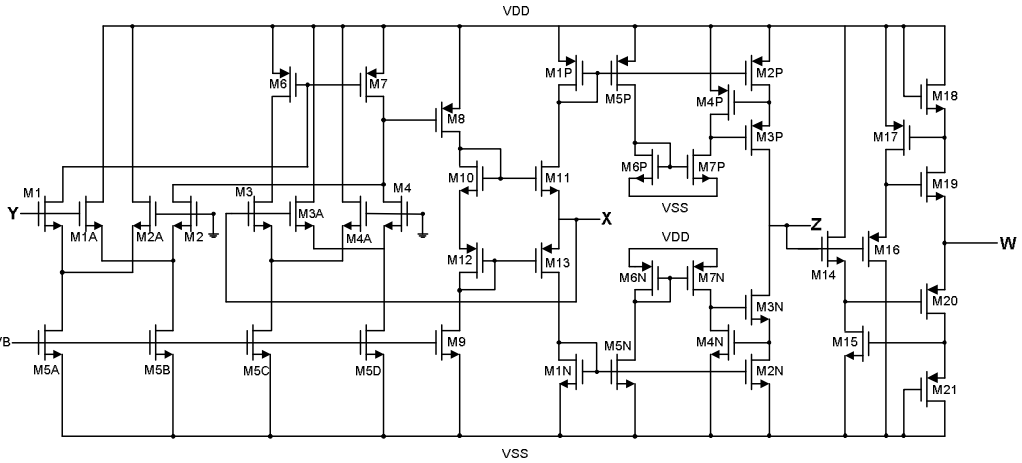

Figure 4.1 The first CMOS ICFOA+ design.

Table 4.1 Transistor dimensions of the first CMOS ICFOA+

TRANSISTORS	W(μm)	L(μm)
M1-M4	0.5	2.5
M1A-M4A	30	2.5
M5A,M5B,M5C,M5D	7	0.5
M6-M7	2	0.5
M8	5	0.5
M9	1	0.5
M10-M11	5	0.5
M12-M13	10	0.5
M14-M15	35	0.35
M16	105	0.35
M17	108	0.35
M18	40.7	0.35
M19	28	0.35
M20	87.5	0.35
M21	117	0.35
M1P-M3P	20	0.5
M4P	0.5	0.5
M5-M7P	2	0.5
M1N-M3N	10	0.5
M4N	0.5	0.5
M5N-M7N	1	0.5

Figure 4.2 shows the DC relation between Y and X terminal voltages. The input voltage is applied on terminal Y and the output voltage is obtained on terminal X with an infinite resistance connected at the X and terminal Z being grounded. Figure 4.3 shows I_X-I_Z DC characteristic of the circuit. A linear current flowing over a wide current range can be seen from this figure. Figure 4.4 shows the DC relation between the voltages at W and Z terminals, V_W and V_Z. As it is seen from the figure these voltages show a linear relation as expected for a wide range of voltage.

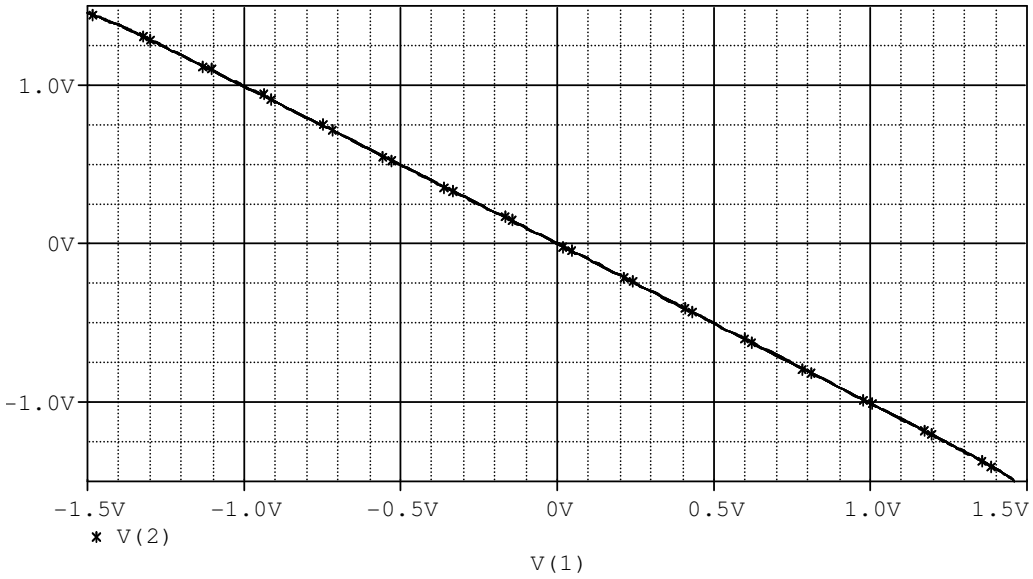

Figure 4.2 DC characteristic between V_X and V_Y

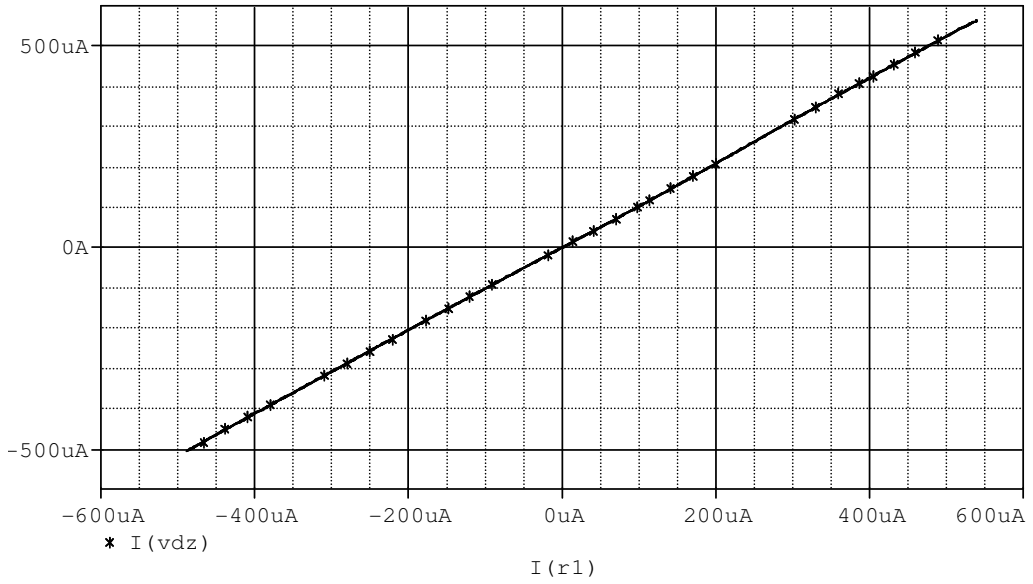

Figure 4.3 DC characteristic between I_Z and I_X

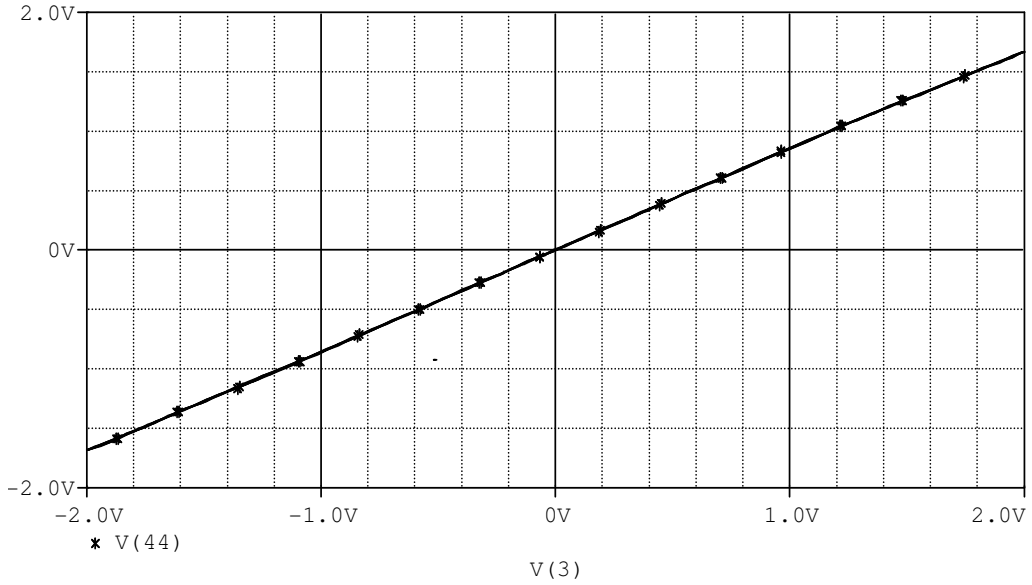

Figure 4.4 DC characteristic between V_W and V_Z.

Figure 4.5 shows the AC characteristic between X and Y voltages. It is seen from this figure that the relation between these voltages given in Equation (2.7) is verified up to 100MHz. In the same way, Figure 4.6 shows the I_X-I_Z AC characteristic. It illustrates that the relation between I_X-I_Z up to 100MHz as it is expected. Figure 4.7 shows the V_W-V_Z AC characteristic and illustrates the relation between the voltages at Z and W terminals. These figures confirm that the proposed CMOS ICFOA+ works properly.

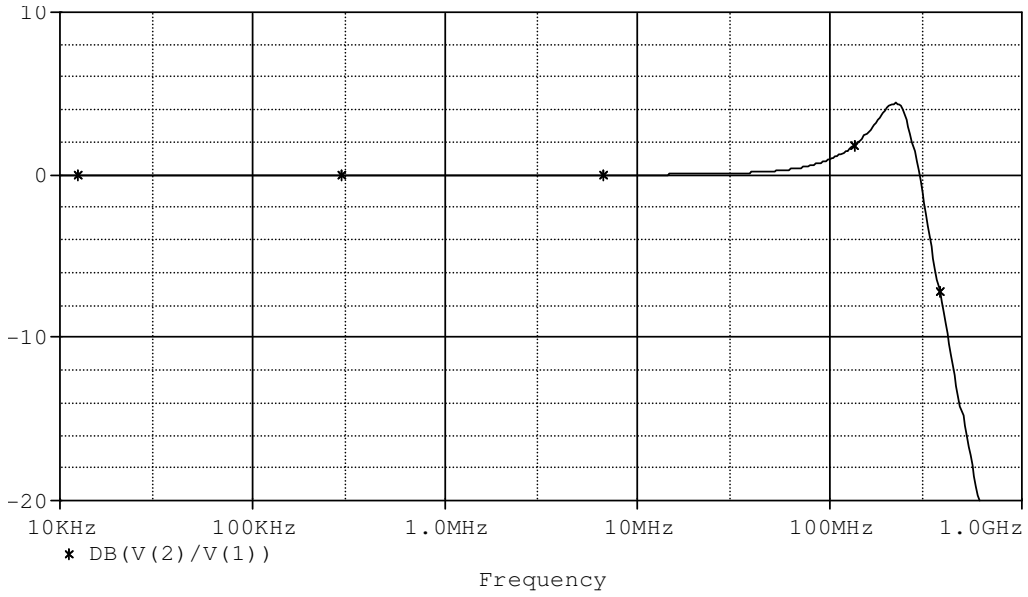

Figure 4.5 AC characteristic between V_X and V_Y.

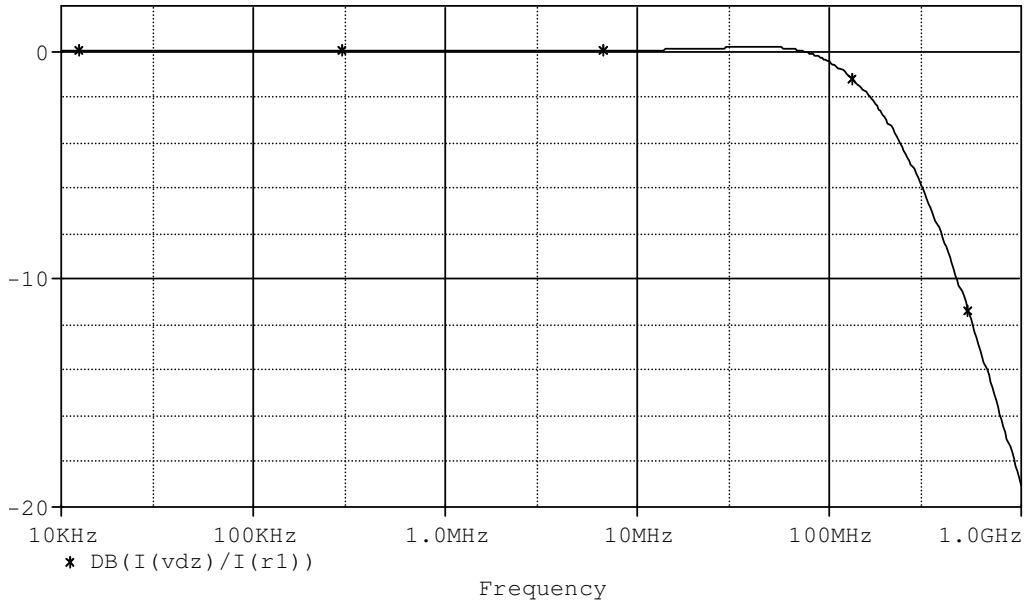

Figure 4.6 AC characteristic between I_Z and I_X.

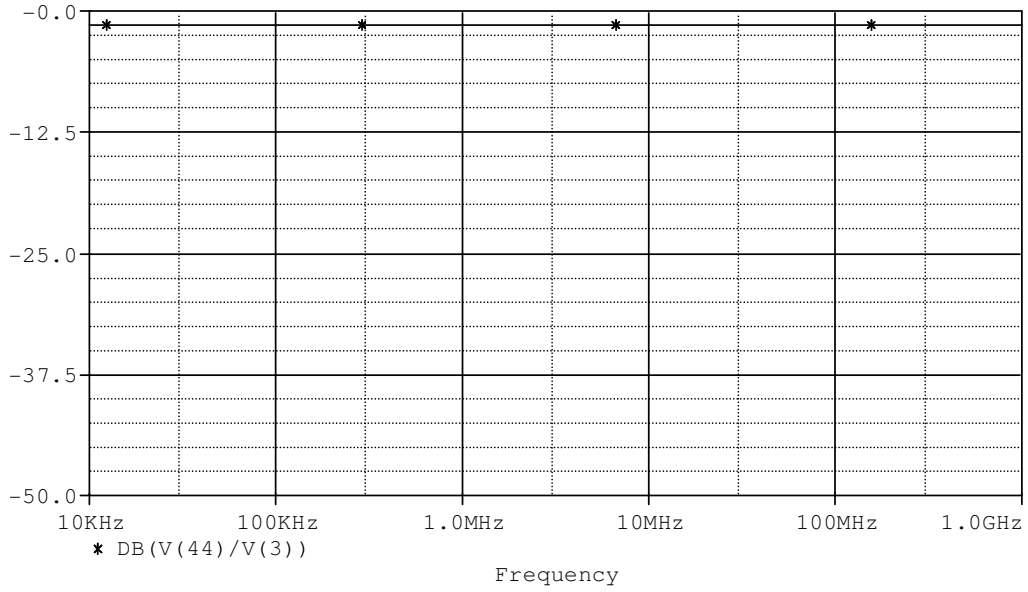

Figure 4.7 AC characteristic between V_W and V_Z.

Figure 4.8 shows the frequency responses of the impedance at terminal X. The resistance value at terminal X between 1Hz-100kHz is 63Ω, at 1MHz, 10MHz and 100MHz is 84Ω, 514Ω, 1.28kΩ, respectively. These values show that the resistance value is small for low frequencies as expected. Figure 4.9 shows the frequency responses of the impedance at terminal Y. The resistance value at terminal Y at 1Hz, 10Hz, 100Hz, 1kHz, 10kHz, 100kHz, 1MHz, 10MHz, 100MHz is 2.2825TΩ, 228.250GΩ, 22.825GΩ, 2.2825GΩ, 228MΩ, 22.825MΩ, 2.2825MΩ, 228.248kΩ, 22.810kΩ, respectively. These values verify the feature of this port; its input current approaches to zero. Figure 4.10 shows the frequency responses of the impedance at terminal Z. The resistance value at terminal Z at 1Hz, 10Hz, 100Hz, 1kHz, 10kHz, 100kHz, 1MHz, 10MHz, 100MHz is 219.461GΩ, 139.198GΩ, 17.856GΩ, 1.79GΩ, 209.480MΩ, 21MΩ, 2.1MΩ, 209kΩ, 20.219kΩ, respectively. Similarly these values verify the feature of this port; the high impedance output. Figure 4.11 shows the frequency responses of the impedance at terminal W. The resistance value at terminal W from 1Hz to 500MHz is 179.7Ω. These values verify the feature of this port; the low impedance output.

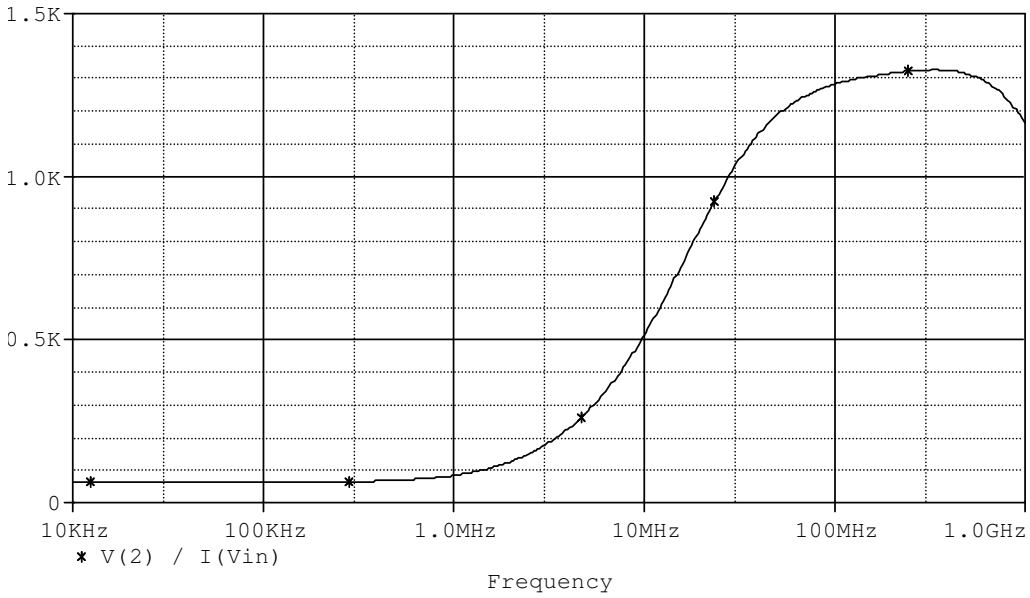

Figure 4.8 Impedance when looking at terminal X.

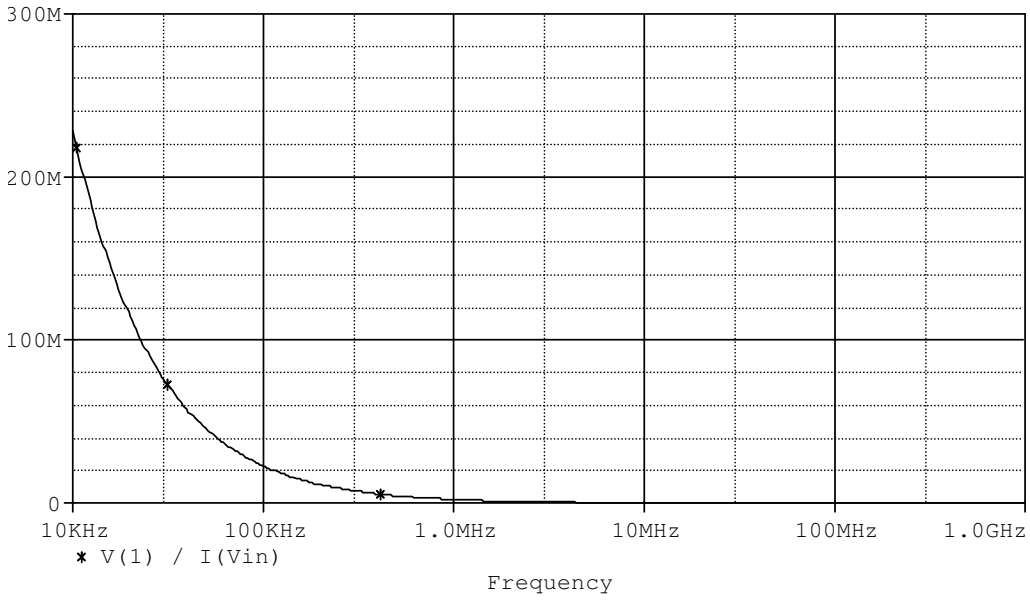

Figure 4.9 Impedance when looking at terminal Y.

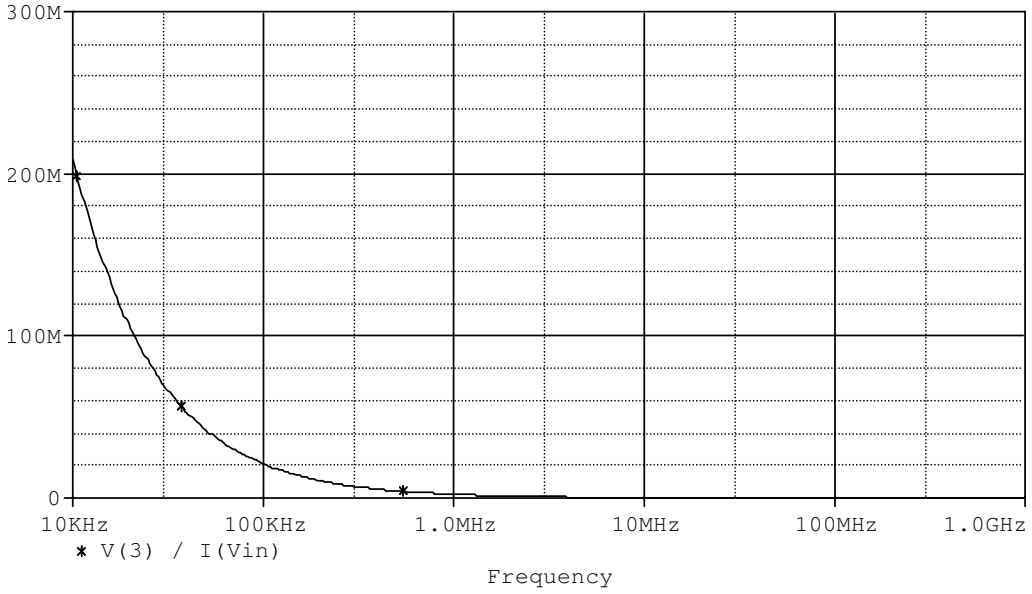

Figure 4.10 Impedance when looking at terminal Z.

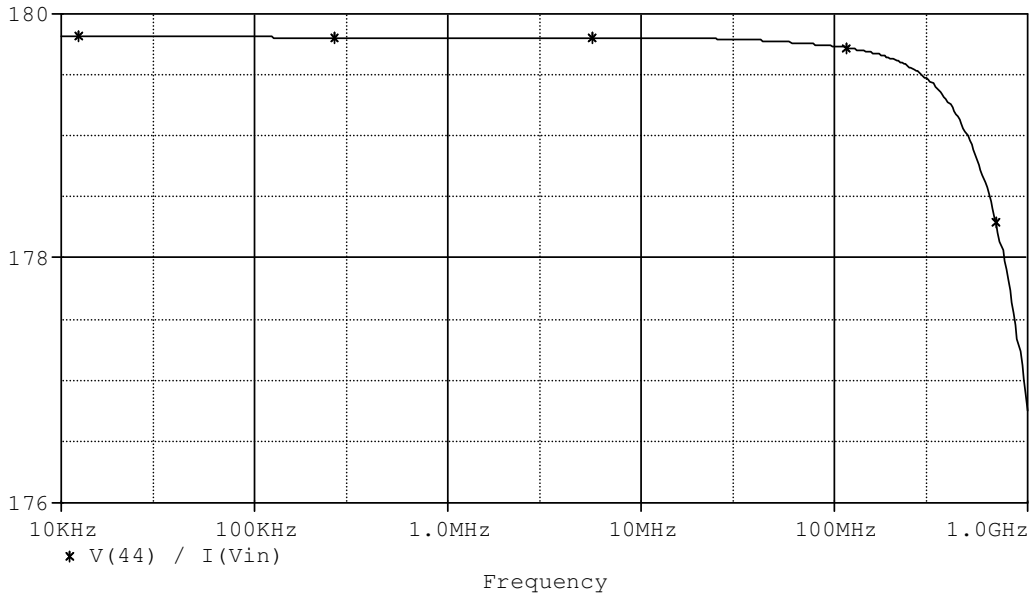

Figure 4.11 Impedance when looking at terminal W.

4.1.2 The Second CMOS ICFOA+ Design

Another CMOS realization of ICFOA+ is shown in Figure 4.12. It is obtained by cascading the DDCC based ICCII in Ibrahim & Kuntman (2002), (with grounded Y_1 and Y_3 terminals) and the buffer in Gupta & Senani (2005). The performance of the

proposed CMOS realization is simulated using SPICE program with 0.35µm CMOS process parameters. The aspect ratios of the MOS transistor in the circuit are given in Table 4.2. The supply voltages (VDD, VSS) are taken as ±2.5V, and bias voltages are VB=–1.7V, VC=–2.0139V.

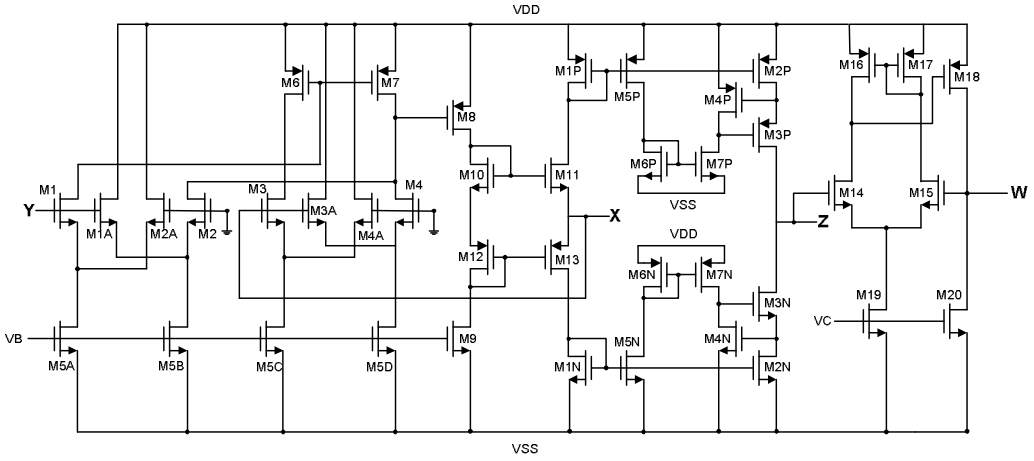

Figure 4.12 The second CMOS ICFOA+ design.

Table 4.2 Transistor dimensions of the second CMOS ICFOA+

TRANSISTORS	W(µm)	L(µm)
M1-M4	0.5	2.5
M1A-M4A	30	2.5
M5A,M5B,M5C,M5D	7	0.5
M6-M7	2	0.5
M8	5	0.5
M9	1	2
M10-M11	5	0.5
M12-M13	10	0.5
M14	35	0.35
M15-M16	24	0.35
M17	60	1.5
M18	15	1.5
M19-M20	10	1.5
M1P-M3P	20	0.5
M4P	0.5	0.5
M5-M7P	2	0.5
M1N-M3N	10	0.5
M4N	0.5	0.5
M5N-M7N	1	0.5

Figure 4.13 shows the DC relation between Y and X terminal voltages. The input voltage is applied on terminal Y and the output voltage is obtained on terminal X

with an infinite resistance connected at the X and terminal Z being grounded. Figure 4.14 shows I_X-I_Z DC characteristic of the circuit. A linear current flowing over a wide current range can be seen from this figure. Figure 4.15 shows the DC relation between the voltages at W and Z terminals, V_W and V_Z. As seen from the figure these voltages show a linear relation as expected for a wide range of voltage.

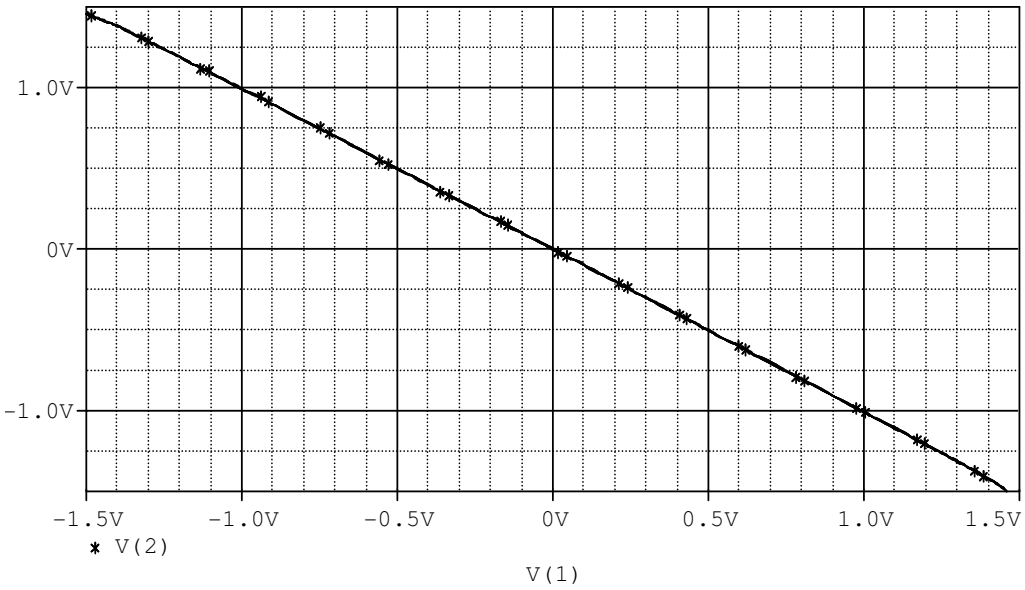

Figure 4.13 DC characteristic between V_X and V_Y.

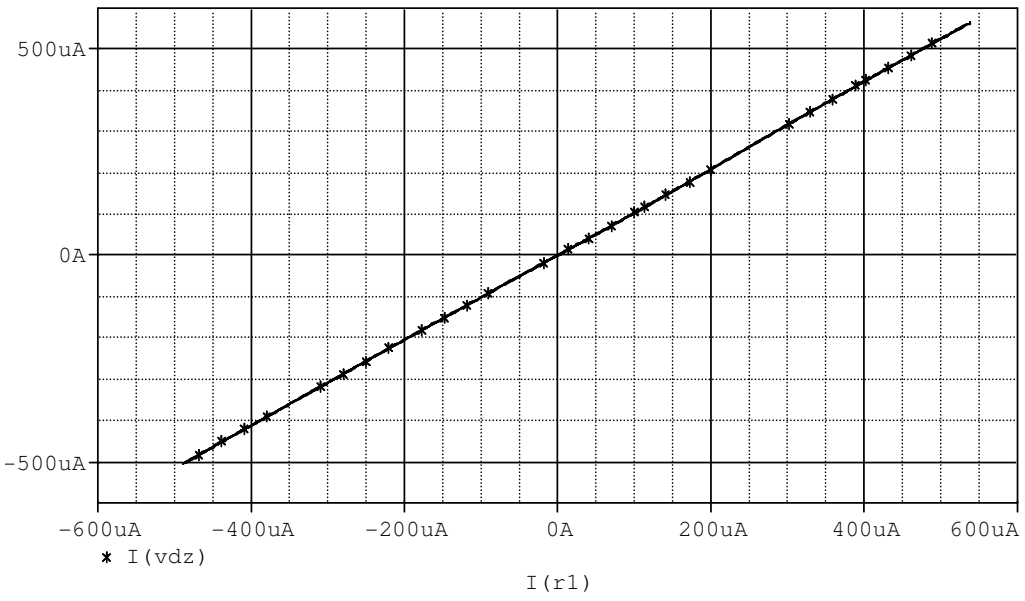

Figure 4.14 DC characteristic between I_Z and I_X.

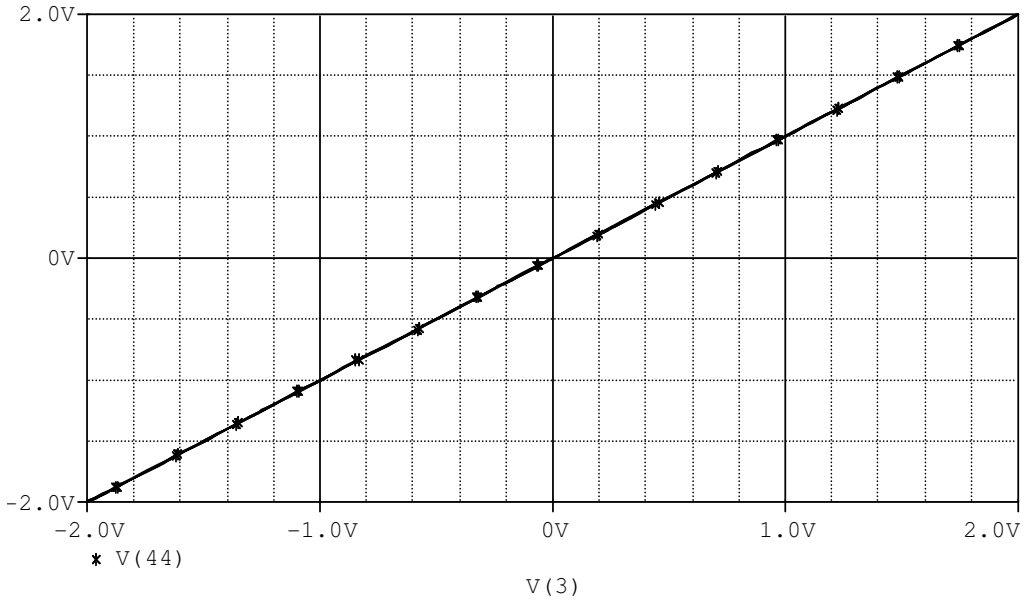

Figure 4.15 DC characteristic between V_W and V_Z.

Figure 4.16 shows the AC characteristic between X and Y voltages. It is seen from this figure that the relation between these voltages given in Equation (2.7) is verified up to 50MHz. In the same way, Figure 4.17 shows the I_X-I_Z AC characteristic. It illustrates that the relation between I_X-I_Z up to 40MHz as it is expected. Figure 4.18 shows the V_W-V_Z AC characteristic and illustrates the relation between the voltages at Z and W terminals. These figures confirm that the proposed CMOS ICFOA+ circuit works properly.

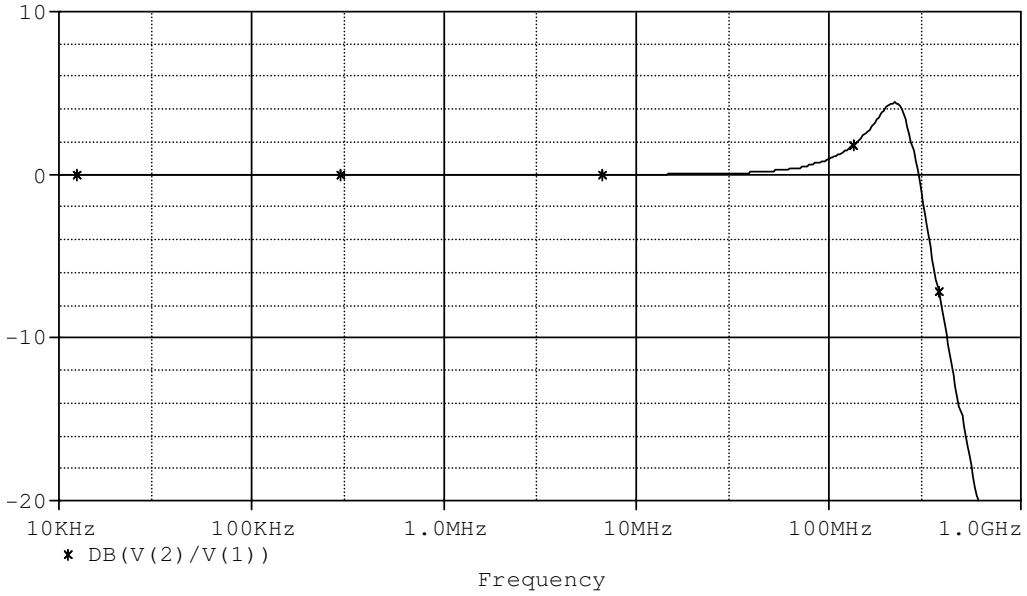

Figure 4.16 AC characteristic between V_X and V_Y.

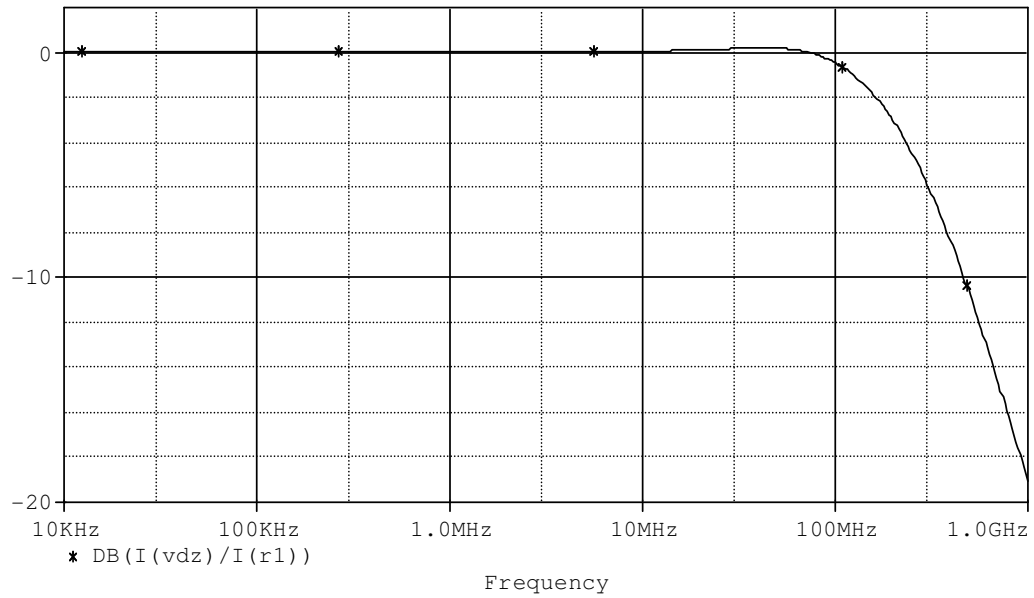

Figure 4.17 AC characteristic between I_Z and I_X.

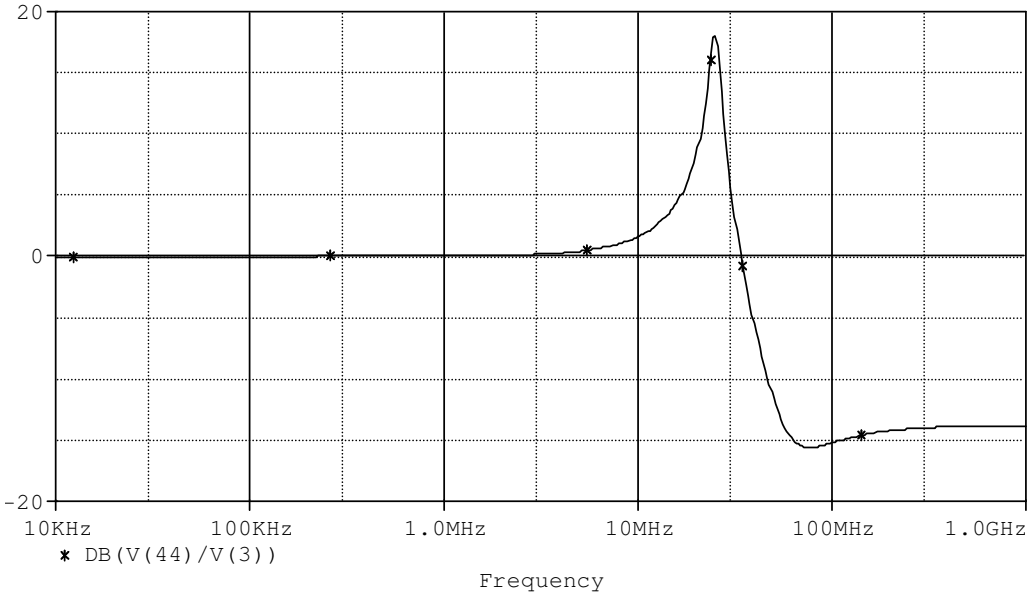

Figure 4.18 AC characteristic between V_W and V_Z.

Figure 4.19 shows the frequency responses of the impedance at terminal X. The resistance value at terminal X between 1Hz-100kHz is 63Ω, at 1MHz, 10MHz and 100MHz is 84Ω, 514Ω, 1.28kΩ respectively. These values show that the resistance value is small for low frequencies as expected. Figure 4.20 shows the frequency responses of the impedance at terminal Y. The resistance value at terminal Y at 1Hz, 10Hz, 100Hz, 1kHz, 10kHz, 100kHz, 1MHz, 10MHz, 100MHz is 2.2825TΩ, 228.250GΩ, 22.825GΩ, 2.2825GΩ, 228MΩ, 22.825MΩ, 2.2825MΩ, 228.248kΩ, 22.810kΩ, respectively. These values verify the feature of this port; its input current approaches to zero. Figure 4.21 shows the frequency responses of the impedance at terminal Z. The resistance value at terminal Z at 1Hz, 10Hz, 100Hz, 1kHz, 10kHz, 100kHz, 1MHz, 10MHz, 100MHz is 258.359GΩ, 239.298GΩ, 62.6GΩ, 6.6GΩ, 645MΩ, 64MΩ, 6.4MΩ, 655kΩ, 55kΩ, respectively. Similarly these values verify the feature of this port; the high impedance output. Figure 4.22 shows the frequency responses of the impedance at terminal W. The resistance value at terminal W between 1Hz-1MHz is 1.5kΩ at10MHz and 100MHz is 5.7kΩ and 10.8kΩ respectively. These values verify the feature of this port; the low impedance output.

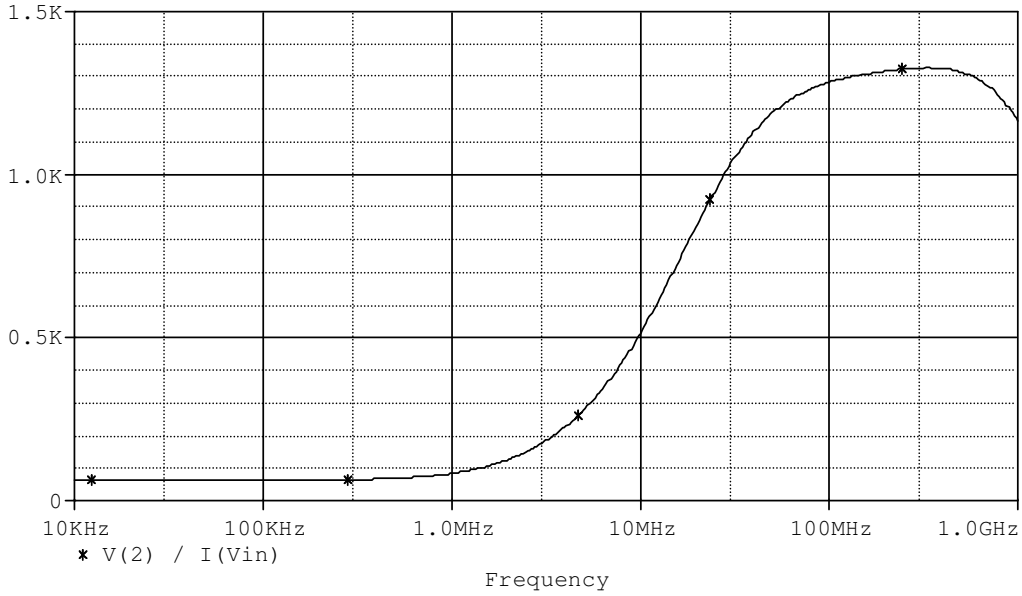

Figure 4.19 Impedance when looking at terminal X.

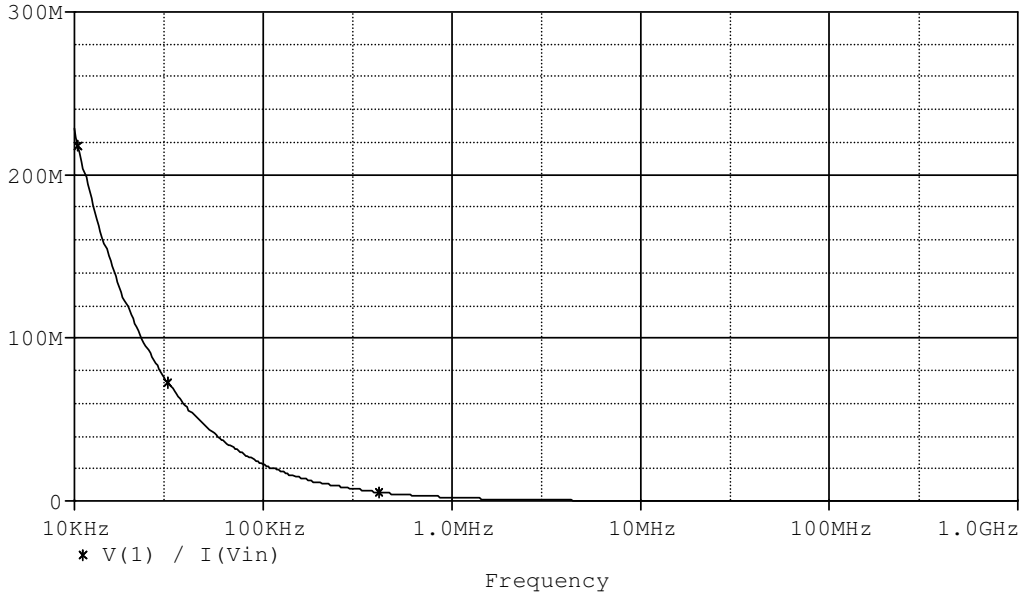

Figure 4.20 Impedance when looking at terminal Y.

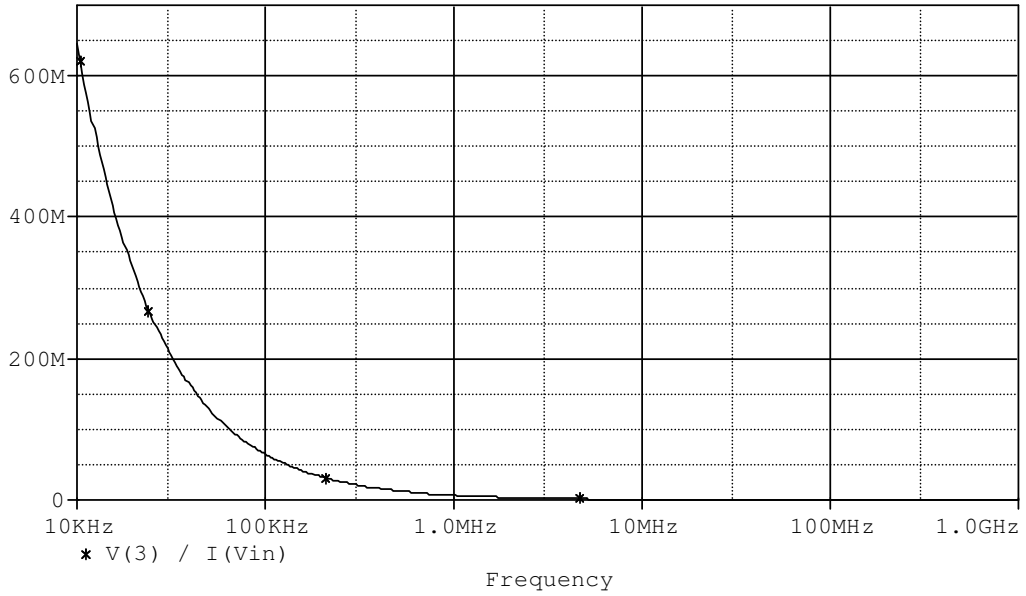

Figure 4.21 Impedance when looking at terminal Z.

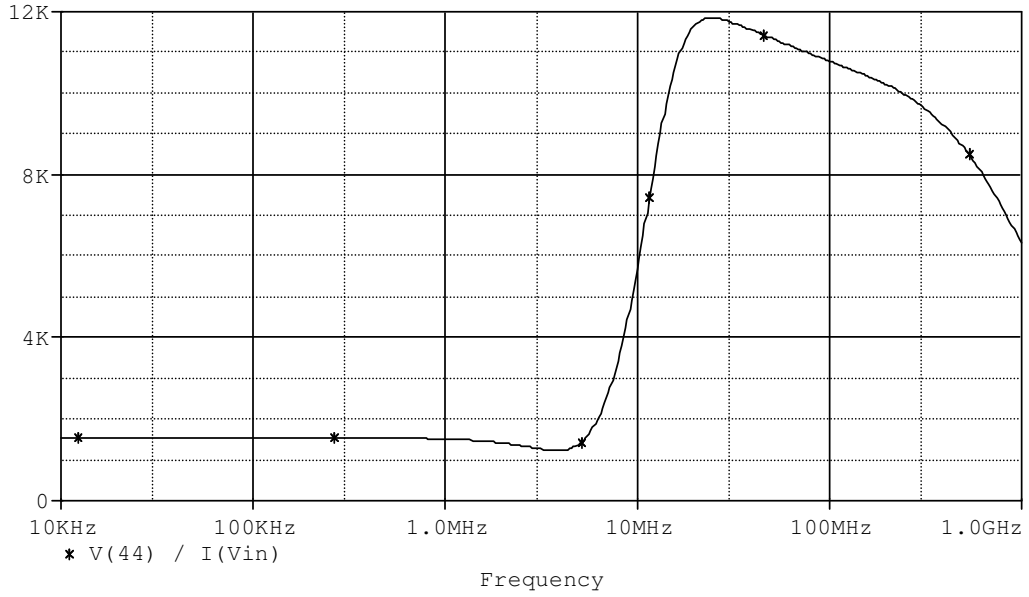

Figure 4.22 Impedance when looking at terminal W.

4.1.3 The Third CMOS ICFOA+ Design

Another CMOS realization of ICFOA+ is obtained by cascading the DVCC in Ibrahim, Minaei & Kuntman (2006), (with grounded Y_1 terminal and removing some transistors) and the buffer in Gupta & Senani (2005) as shown in Figure 4.23. The

performance of the proposed CMOS realization is simulated using SPICE program with 0.35µm and 0.5 µm CMOS process parameters. The aspect ratios of the MOS transistor in the circuit are given in Table 4.3. The supply voltages (VDD, VSS) are taken as ±2.5V, and bias voltages are VB=–1.32V, VC=–2.0139V.

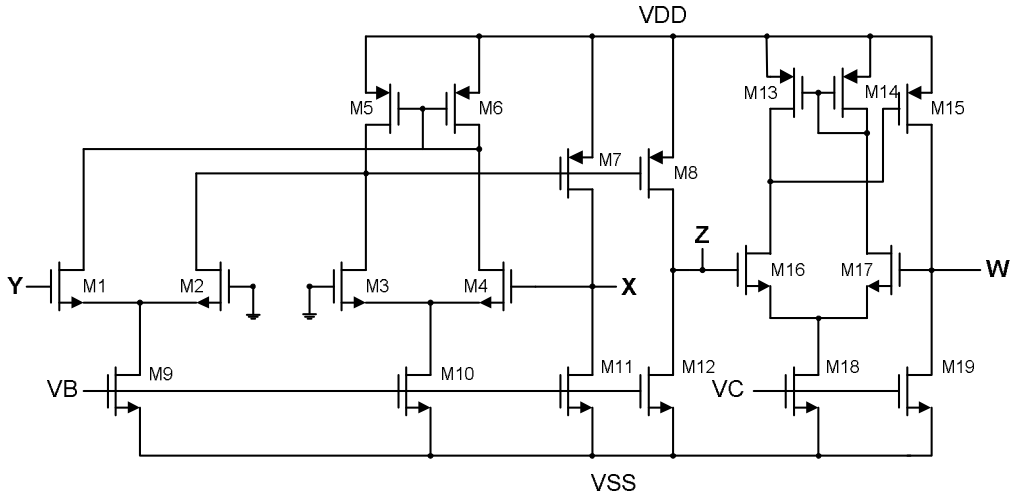

Figure 4.23 The third CMOS ICFOA+ design.

Table 4.3 Transistor dimensions of the third CMOS ICFOA+

TRANSISTORS	W(µm)	L(µm)
M1	0.55	0.5
M2	0.86	0.5
M3-M4	0.6	0.5
M5	20.5	0.5
M6	13	0.5
M7-M8	10	0.5
M9	16	2
M10	15	2
M11-M12	153.5	2.5
M13	24	0.35
M14	60	1.5
M15	15	1.5
M16	35	0.35
M17	24	0.35
M18-M19	10	1.5

Figure 4.24 shows the DC relation between Y and X terminal voltages. The input voltage is applied on terminal Y and the output voltage is obtained on terminal X with an infinite resistance connected at the X and terminal Z being grounded. Figure

4.25 shows I_X-I_Z DC characteristic of the circuit. A linear current flowing over a wide current range can be seen from this figure. Figure 4.26 shows the DC relation between the voltages at W and Z terminals, V_W and V_Z. As seen from the figure these voltages show a linear relation as expected for a wide range of voltage.

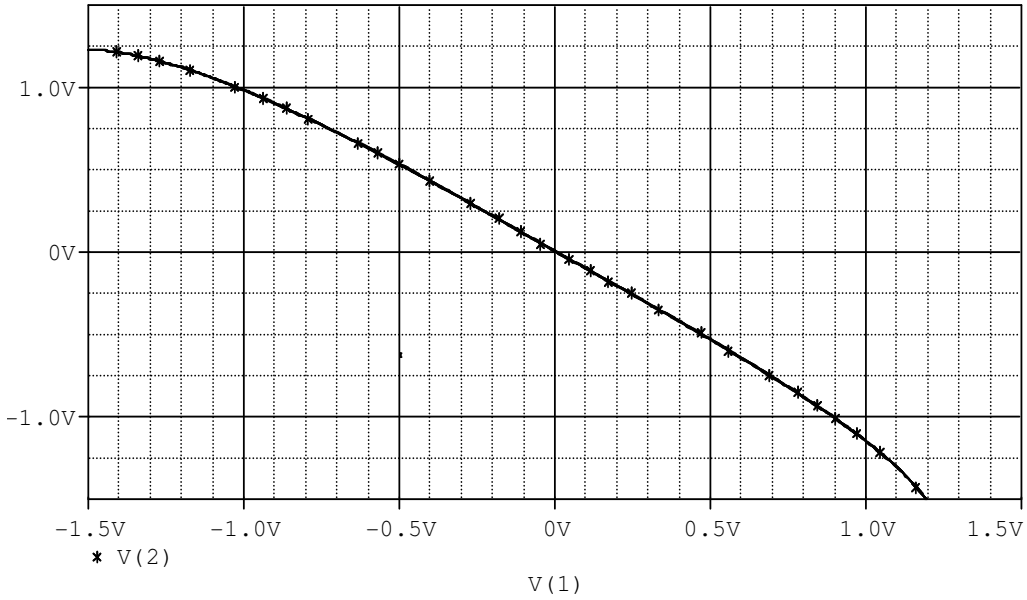

Figure 4.24 DC characteristic between V_X and V_Y.

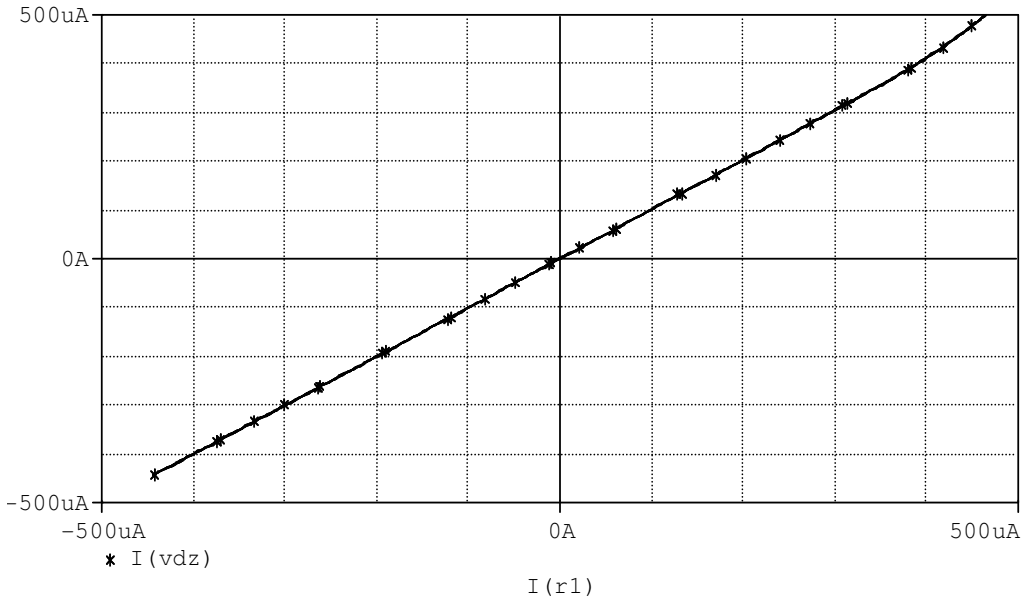

Figure 4.25 DC characteristic between I_X and I_Z.

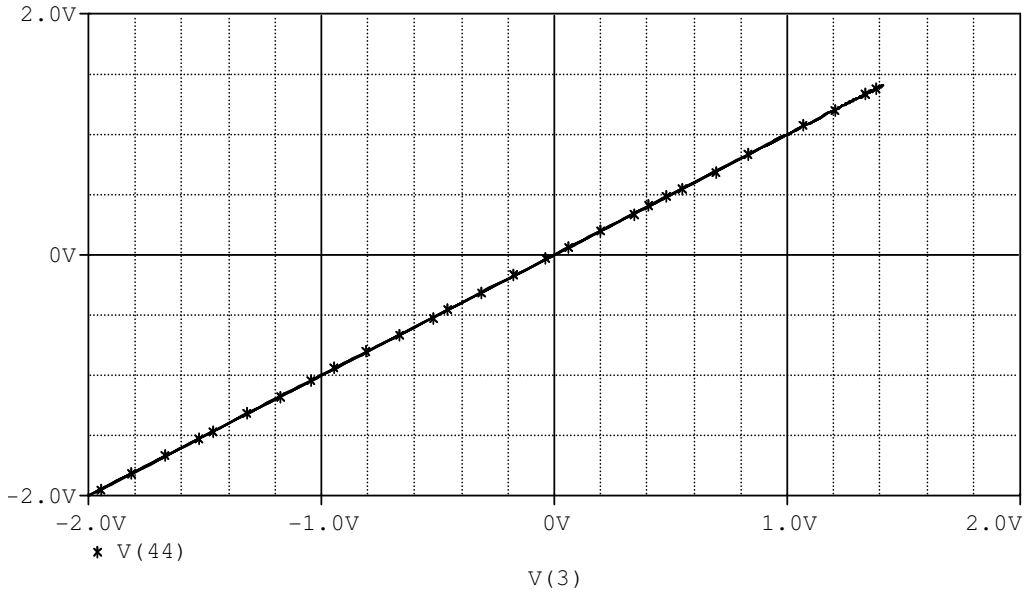

Figure 4.26 DC characteristic between V_W and V_Z.

Figure 4.27 shows the AC characteristic between X and Y voltages. It is seen from this figure that the relation between these voltages given in Equation (2.7) is verified up to 50MHz. In the same way Figure 4.28 shows the I_X-I_Z AC characteristic. It illustrates that the relation between I_X-I_Z up to 40MHz as it is expected. Figure 4.29 shows the V_W-V_Z AC characteristic and illustrates the relation between the voltages at Z and W terminals. These figures confirm that the proposed CMOS ICFOA+ circuit works properly.

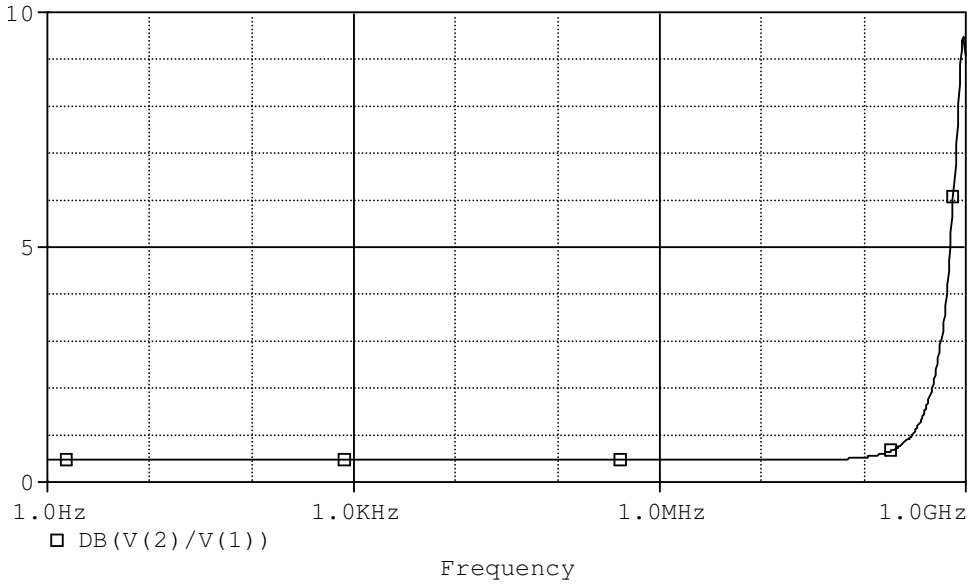

Figure 4.27 AC characteristic between V_X and V_Y.

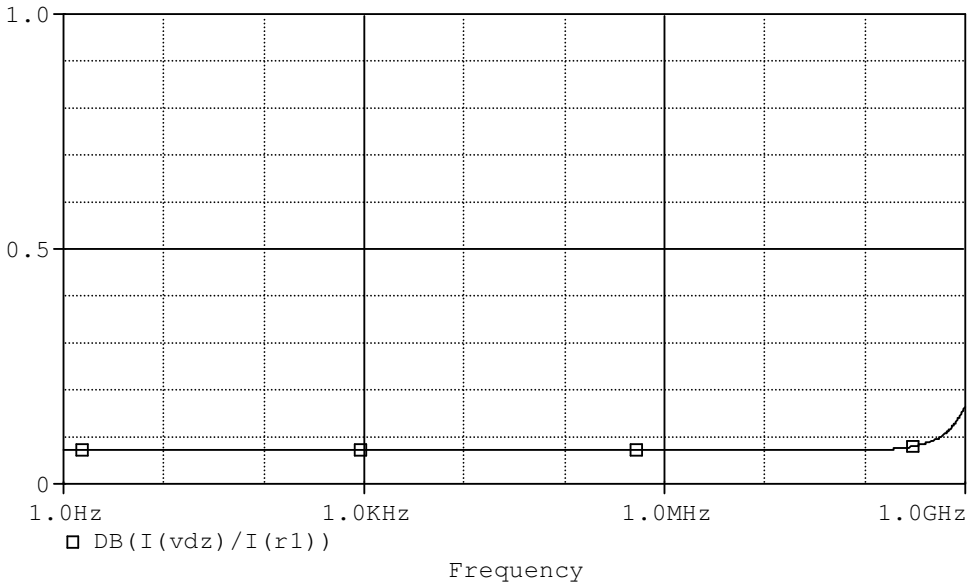

Figure 4.28 AC characteristic between I_Z and I_X.

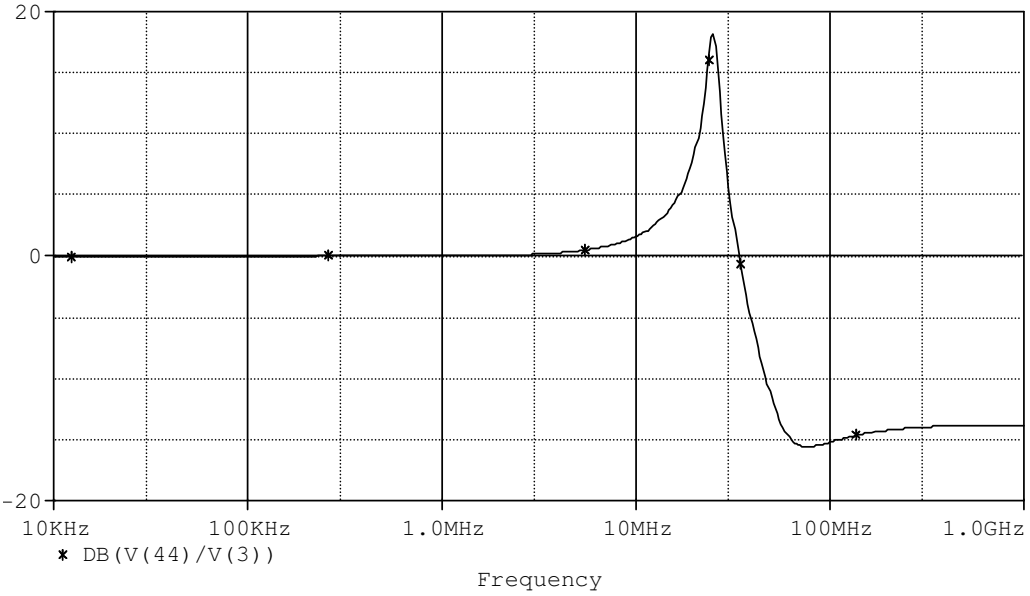

Figure 4.29 AC characteristic between V_W and V_Z.

Figure 4.30 shows the frequency responses of the impedance at terminal X. The resistance value at terminal X between 1Hz-100MHz is 169Ω, at 10MHz and 100MHz is 200Ω, 1kΩ, respectively. These values show that the resistance value is small for low frequencies as expected. Figure 4.31 shows the frequency responses of the impedance at terminal Y. The resistance value at terminal Y at 1Hz, 10Hz, 100Hz, 1kHz, 10kHz, 100kHz, 1MHz, 10MHz, 100MHz is 345TΩ, 34TΩ, 3.4TΩ, 345GΩ, 34.5GΩ, 3.4GΩ, 342MΩ, 34MΩ, 3.4MΩ, respectively. These values verify the feature of this port; its input current approaches to zero. Figure 4.32 shows the frequency responses of the impedance at terminal Z. The resistance value at terminal Z between 1Hz-1MHz is 126kΩ, at 10MHz, 100MHz, is 122kΩ, 37kΩ, respectively. Similarly these values verify the feature of this port; the high impedance output. Figure 4.33 shows the frequency responses of the impedance at terminal W. The resistance value at terminal W between 1Hz-10kHz is 565Ω, between 10kHz-1MHz is 1.5kΩ at 10MHz, 100MHz, is 26kΩ, 130kΩ, respectively. These values verify the feature of this port; the low impedance output. It is obvious from the figure the best working for this terminal is between 10MHz and 100MHz. The features of proposed CMOS ICFOA+ circuits can be compared as shown in Table 4.4.

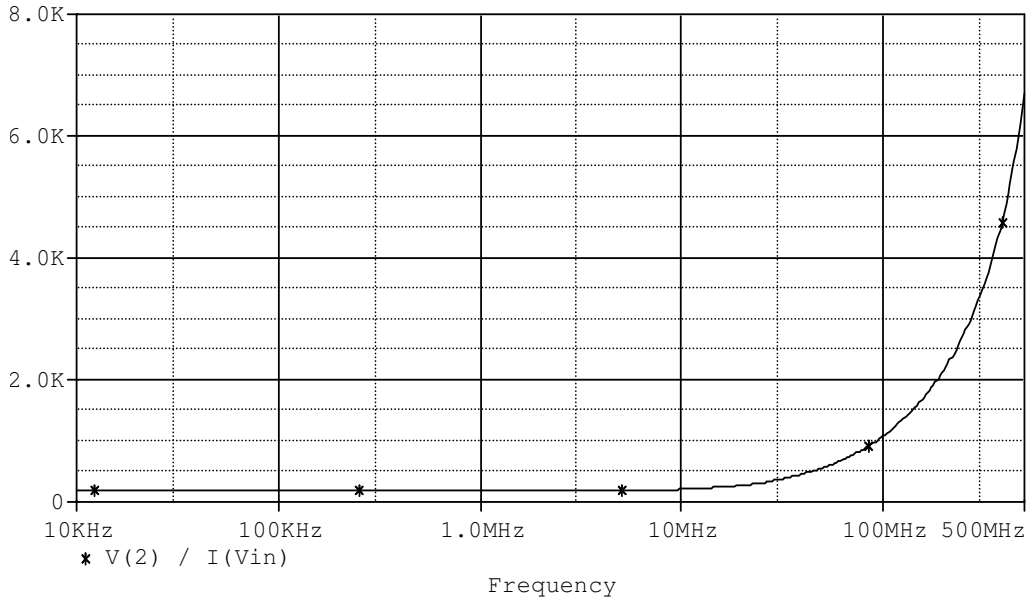

Figure 4.30 Impedance when looking at terminal X.

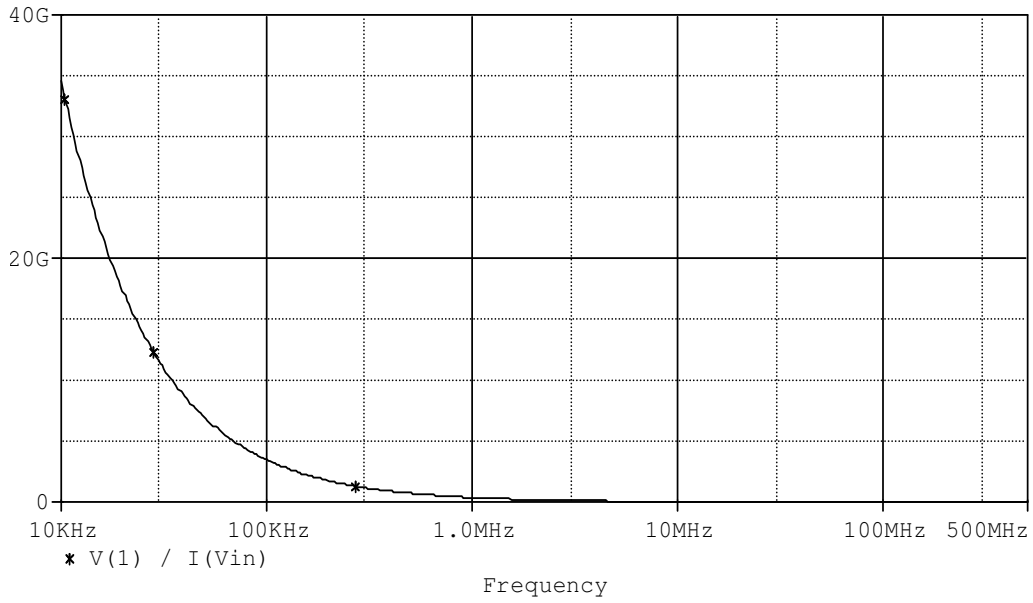

Figure 4.31 Impedance when looking at terminal Y.

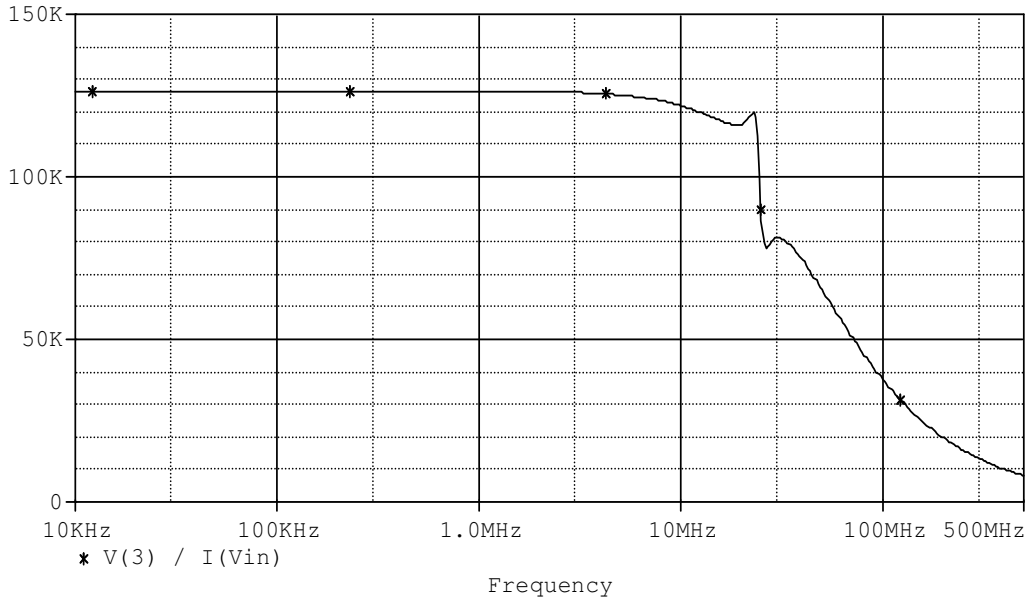

Figure 4.32 Impedance when looking at terminal Z.

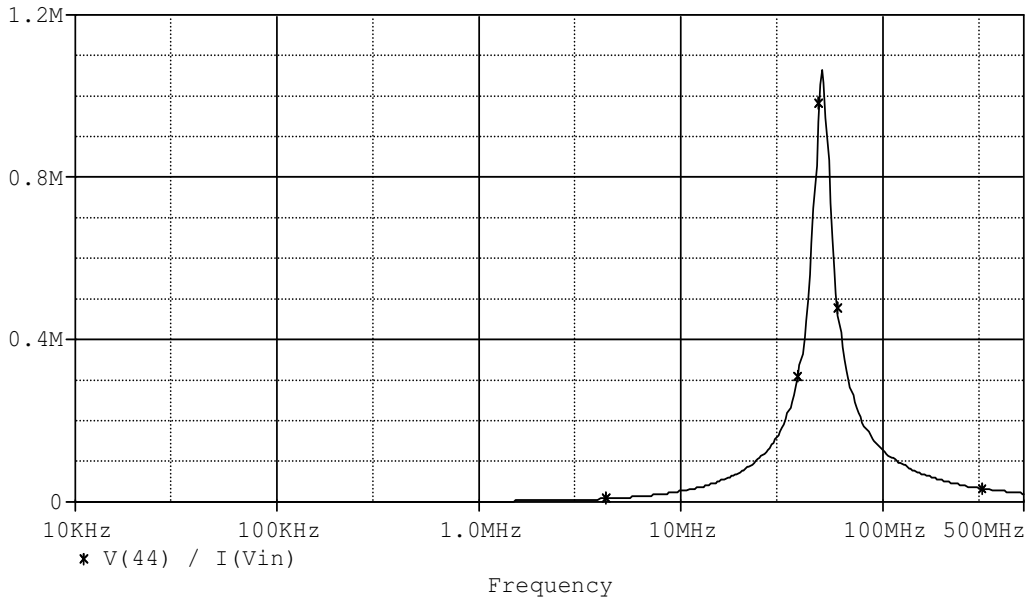

Figure 4.33 Impedance when looking at terminal W.

Table 4.4. Features of CMOS ICFOA+ circuits

	The first ICFOA+	The second ICFOA+	The third ICFOA+
Slew rate	19.61 V/μs	13.59 V/μs	15.07 V/μs
Bandwidth V_X-V_Y	322MHz	323MHz	570MHz
Bandwidth I_Z-I_X	198MHz	199MHz	>1GHz
Bandwidth V_W-V_Z	>1GHz	13.5MHz	13.5MHz
R_X at f=10kHz	63Ω	63Ω	169Ω
R_Y at f=10kHz	228MΩ	228MΩ	34.5GΩ
R_Z at f=10kHz	209.48MΩ	645MΩ	126kΩ
R_W at f=10kHz	179.7Ω	1.5kΩ	565Ω

4.1.4 The First CMOS ICFOA– Design

A CMOS realization of ICFOA– is shown in Figure 4.34. It is obtained by cascading the ICCII– in Sobhy & Soliman (2007) with the voltage buffer in Gupta & Senani (2005). The performance of the proposed CMOS realization is simulated using SPICE program with 0.35μm CMOS process parameters. The aspect ratios of the MOS transistor in the circuit are given in Table 4.5. The supply voltages (VDD, VSS) are taken as ±2.5V and bias voltages are VB=±1.21V, and VC=–2.0139V.

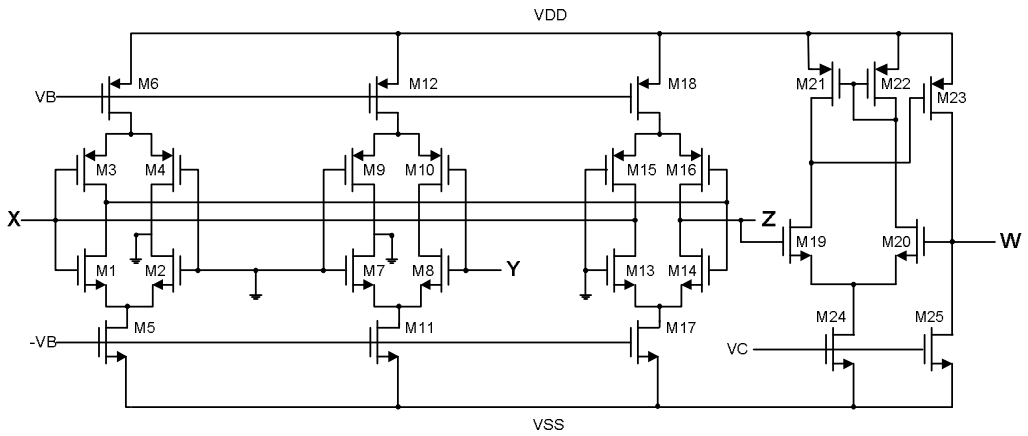

Figure 4.34 The first CMOS ICFOA– design.

Table 4.5 Transistor dimensions of the first CMOS ICFOA–

TRANSISTORS	W(µm)	L(µm)
M1	0.7	2.1
M2	1.05	2.1
M3	3.5	2.1
M4	2.1	2.1
M5	30	1.05
M6	23.5	1.05
M7	2.1	2.1
M8	1.05	2.1
M9	2.1	2.1
M10	2	2.1
M11	27.65	1.05
M12	57.75	1.05
M13-M14	17.5	0.35
M15-M16	35	0.35
M17	17.66	1.05
M18	75.44	1.05
M19	35	0.35
M20-M21	24	0.35
M22	60	1.5
M23	15	1.5
M24-M25	10	1.5

Figure 4.35 shows the DC relation between Y and X terminal voltages. The input voltage is applied on terminal Y and the output voltage is obtained on terminal X with an infinite resistance connected at the X and terminal Z being grounded. Figure 4.36 shows I_X-I_Z DC characteristic of the circuit. A linear current flowing over a wide current range can be seen from this figure. This figure depicts the I_Z=–I_X relation as mentioned before. Figure 4.37 shows the DC relation between the

voltages at W and Z terminals, V_W and V_Z. As seen from the figure these voltages show a linear relation as expected for a wide range of voltage.

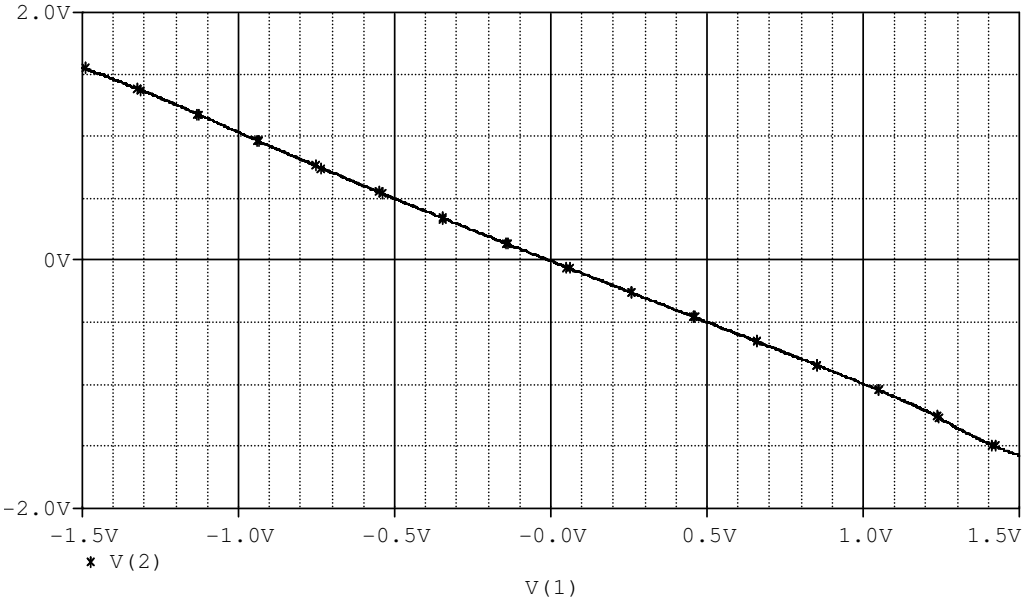

Figure 4.35 DC characteristic between V_X and V_Y.

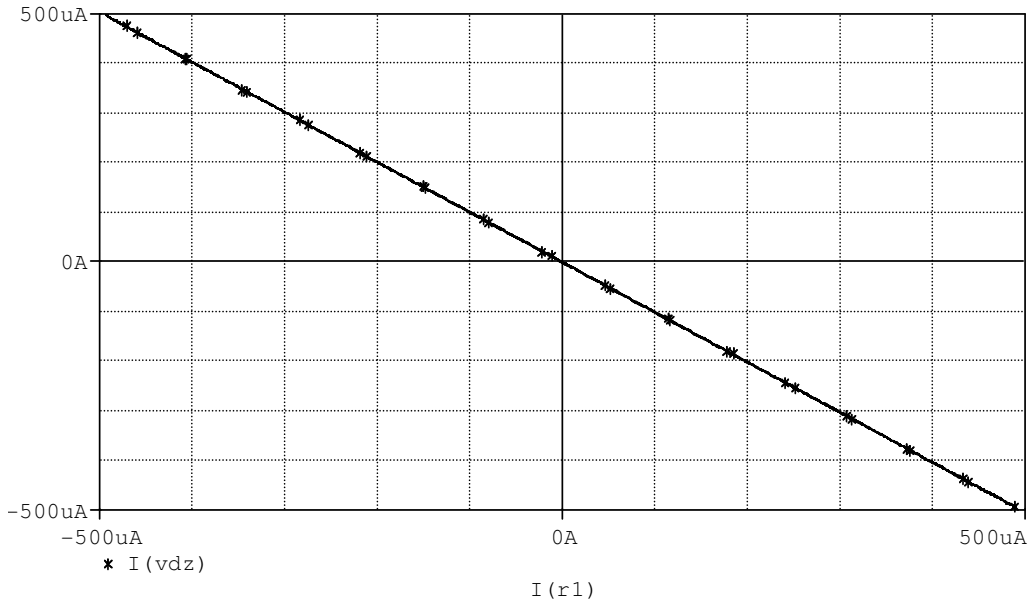

Figure 4.36 DC characteristic between I_Z and I_X.

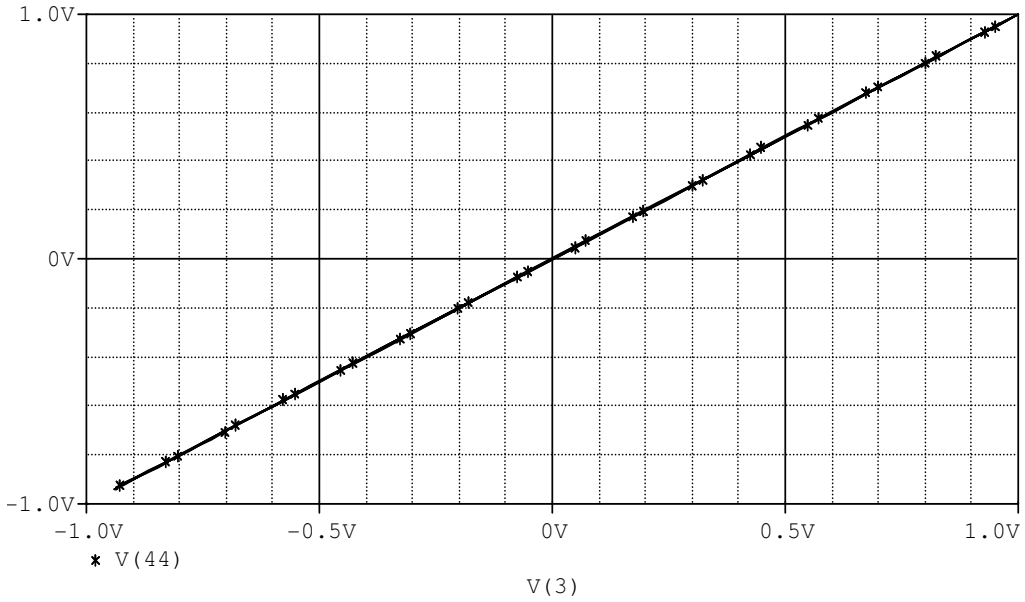

Figure 4.37 DC characteristic between V_W and V_Z.

Figure 4.38 shows the AC characteristic between X and Y voltages. It is seen from this figure that the relation between these voltages given in Equation (2.7) is verified up to 500MHz. In the same way Figure 4.39 shows the I_X-I_Z AC characteristic. It illustrates that the relation between I_X-I_Z up to 100MHz as it is expected. Figure 4.40 shows the V_W-V_Z AC characteristic and illustrates the relation between the voltages at Z and W terminals. These figures confirm that the proposed CMOS ICFOA– circuit works properly.

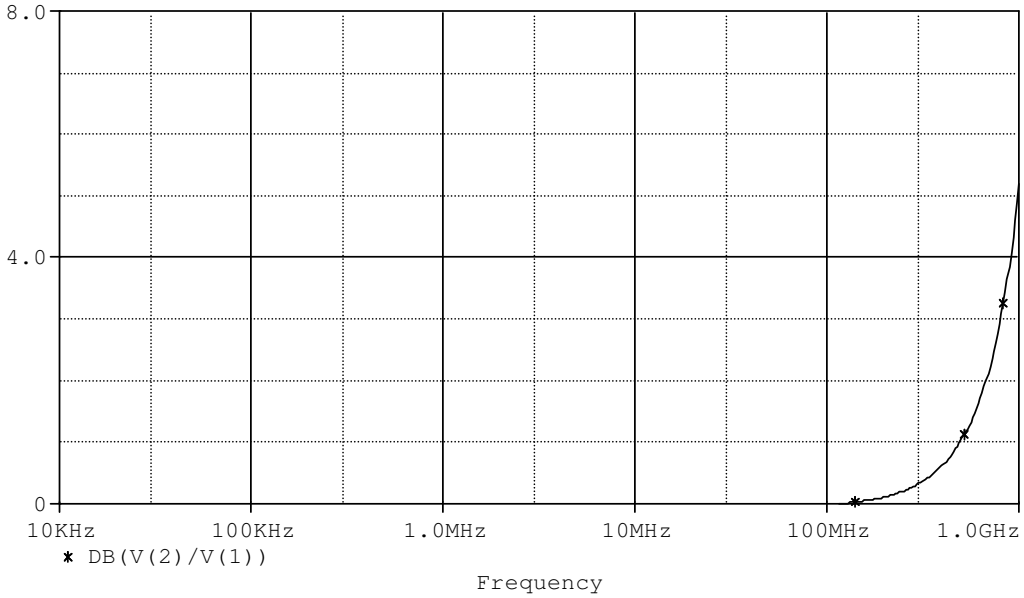

Figure 4.38 AC characteristic between V_X and V_Y.

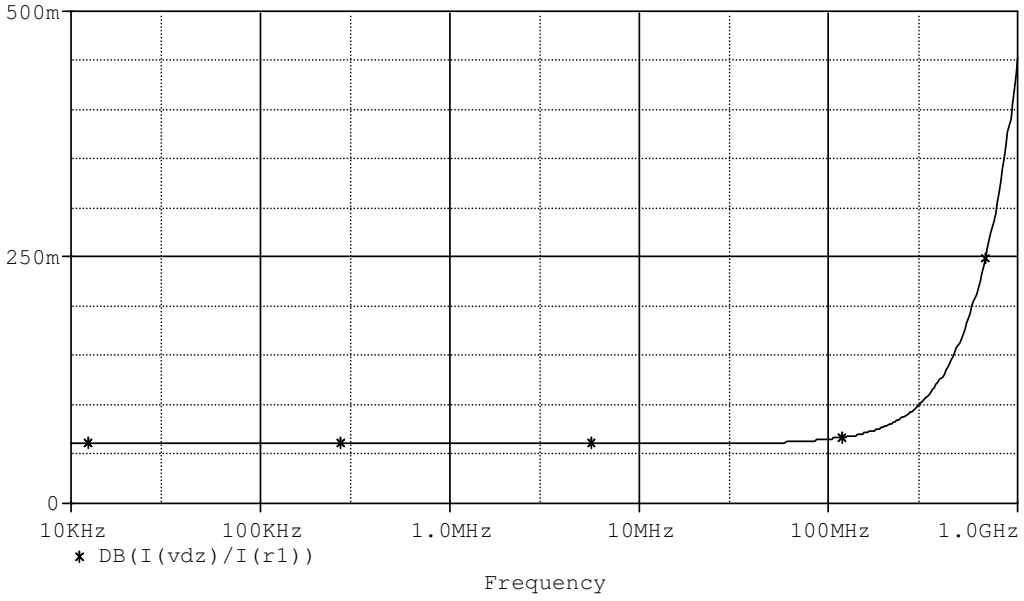

Figure 4.39 AC characteristic between I_Z and I_X.

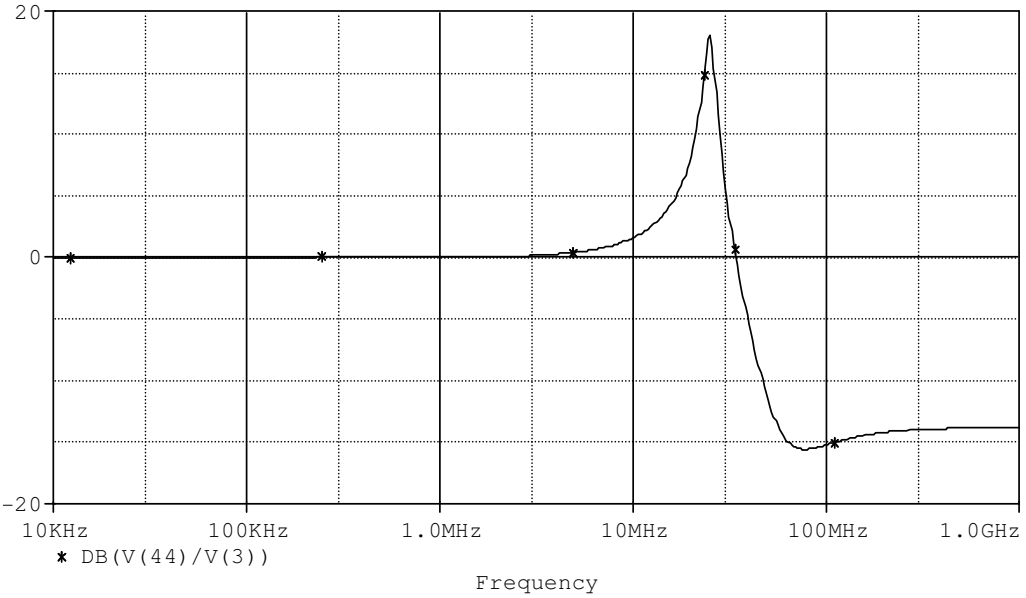

Figure 4.40 AC characteristic between V_W and V_Z.

Figure 4.41 shows the frequency responses of the impedance at terminal X. The resistance value at terminal X between 1Hz-100Hz and 10kHz-100kHz is 8.8kΩ, 25.198kΩ and at 1kHz, 1MHz, 10MHz and 100MHz is 19.647kΩ, 23.968kΩ, 9.94kΩ and 7.36kΩ, respectively. These values show that the resistance value is small for low frequencies as expected. Figure 4.42 shows the frequency responses of the impedance at terminal Y. The resistance value at terminal Y at 1Hz, 10Hz, 100Hz, 1kHz, 10kHz, 100kHz, 1MHz, 10MHz, 100MHz is 7.045TΩ, 690GΩ, 70.451GΩ, 7.0451GΩ, 704.513MΩ, 70.452MΩ, 7.0516MΩ, 712.889kΩ, 71.719kΩ, respectively. These values verify the feature of this port; its input current approaches to zero. Figure 4.43 shows the frequency responses of the impedance at terminal Z. The resistance value at terminal Z between 1Hz-100Hz is 162.556MΩ, at 1kHz, 10kHz, 100kHz, 1MHz, 10MHz, 100MHz is 157.534MΩ, 146.864MΩ, 46.499MΩ, 4.876MΩ, 496.462kΩ, 45.837kΩ, respectively. Similarly these values verify the feature of this port; the high impedance output. Figure 4.44 shows the frequency responses of the impedance at terminal W. The resistance value at terminal W between 1Hz-10kHz is 66.674MΩ, at 100kHz, 1MHz, 10MHz, 100MHz, is 57.986MΩ, 11.522MΩ, 1.1642MΩ, 108.937kΩ, respectively. These values verify the feature of this port; the low impedance output.

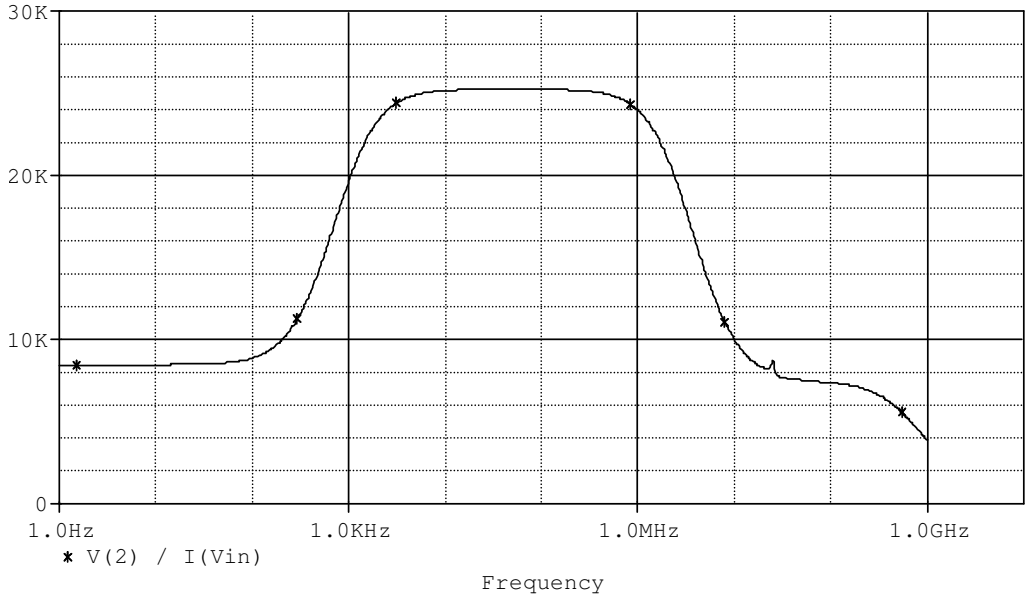

Figure 4.41 Impedance when looking at terminal X.

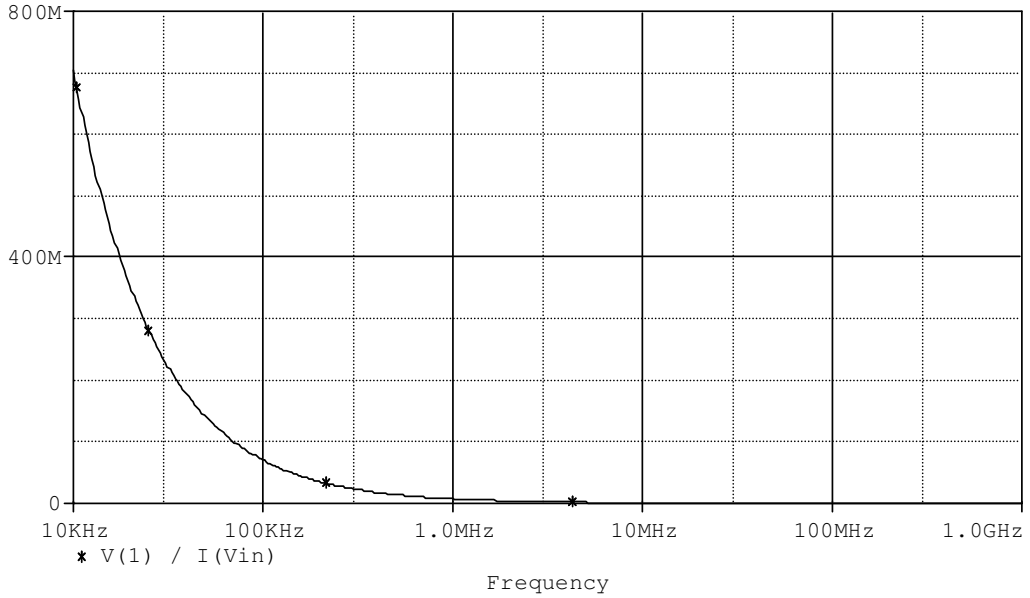

Figure 4.42 Impedance when looking at terminal Y.

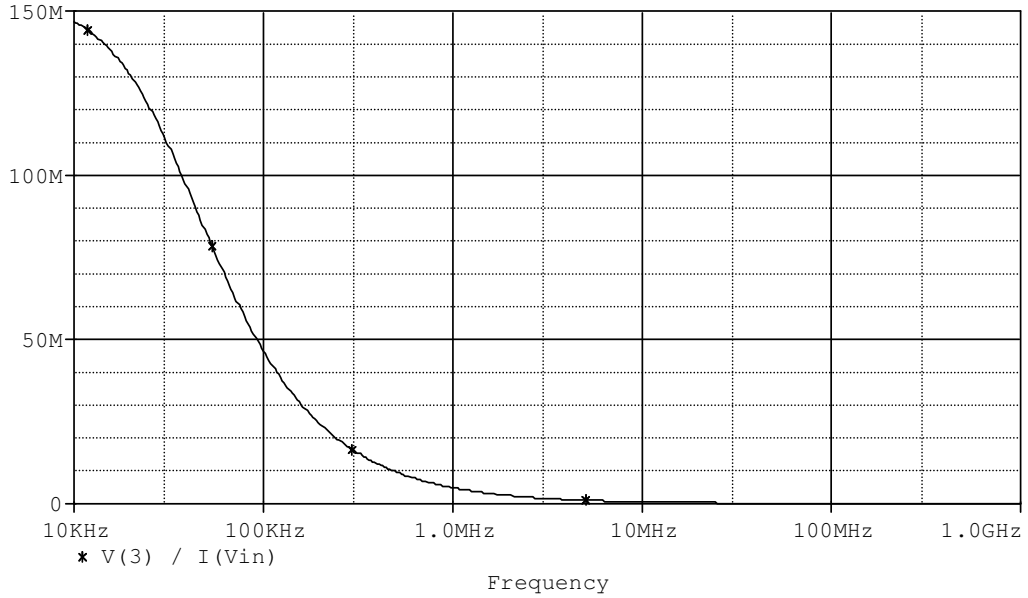

Figure 4.43 Impedance when looking at terminal Z.

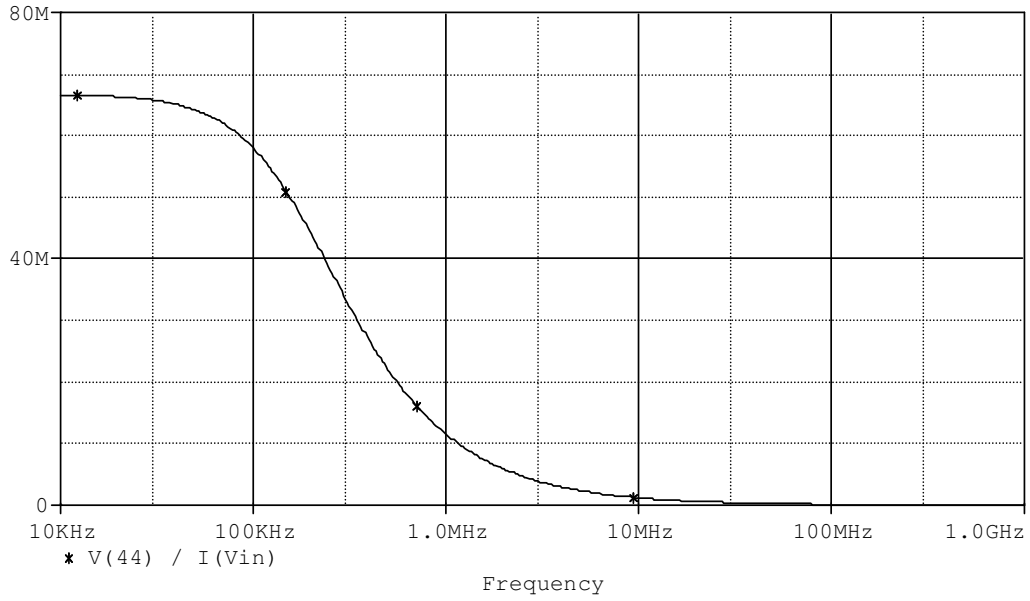

Figure 4.44 Impedance when looking at terminal W.

4.1.5 The Second CMOS ICFOA– Design

Another CMOS realization of ICFOA– obtained by cascading the DVCC based ICCII– in Ibrahim, Minaei & Kuntman (2006), (with grounded Y_1 terminal) and the buffer in Gupta & Senani (2005). The performance of the proposed CMOS

realization is simulated using SPICE program with 0.35µm and 0.5 µm CMOS process parameters. The aspect ratios of the MOS transistor in the circuit are given in Table 4.6. The supply voltages (VDD, VSS) are taken as ±2.5V, bias voltage is VB=–1.32V and VC=–2.0139V.

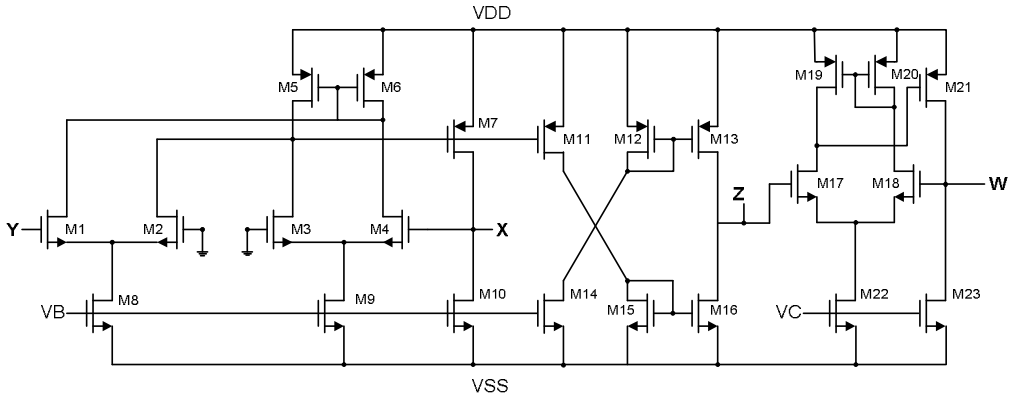

Figure 4.45 The second ICFOA– design.

Table 4.6 Transistor dimensions of the second CMOS ICFOA–

TRANSISTORS	W(µm)	L(µm)
M1	0.66	0.5
M2	1.1	0.5
M3-M4	0.67	0.5
M5	21.1	0.5
M6	13.35	0.5
M7	21.1	0.5
M8	12.7	2
M9	13.2	2
M10	225	2.5
M11	13.3	0.5
M12	14.9	0.5
M13	9.33	0.5
M14	49.5	0.5
M15	38.6	0.5
M16	75.6	0.5
M17	35	0.35
M18-M19	24	0.35
M20	60	1.5
M21	15	1.5
M22-M23	10	1.5

Figure 4.46 shows the DC relation between Y and X terminal voltages. The input voltage is applied on terminal Y and the output voltage is obtained on terminal X with an infinite resistance connected at the X and terminal Z being grounded. Figure 4.47 shows I_X-I_Z DC characteristic of the circuit. A linear current flowing over a wide current range can be seen from this figure. This figure depicts the I_Z=–I_X relation as mentioned before. Figure 4.48 shows the DC relation between the voltages at W and Z terminals, V_W and V_Z. As seen from the figure these voltages show a linear relation as expected for a wide range of voltage.

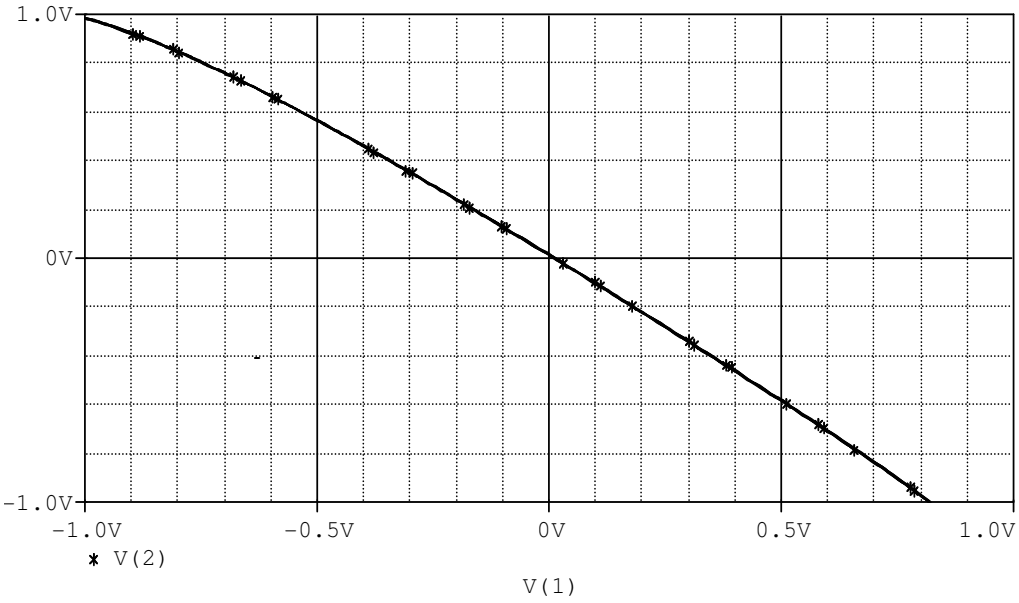

Figure 4.46 DC characteristic between V_X and V_Y.

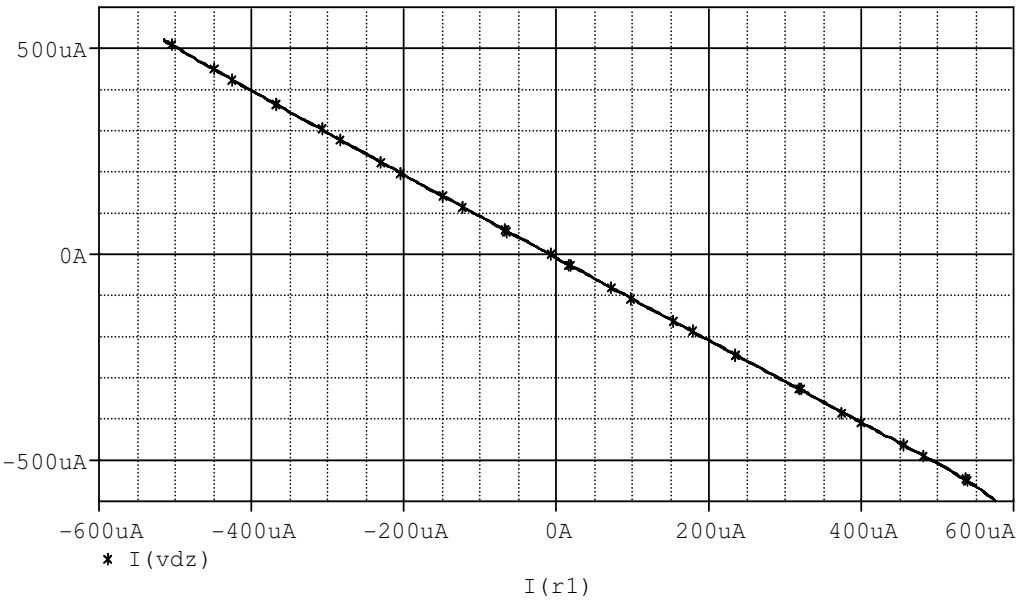

Figure 4.47 DC characteristic between I_Z and I_X.

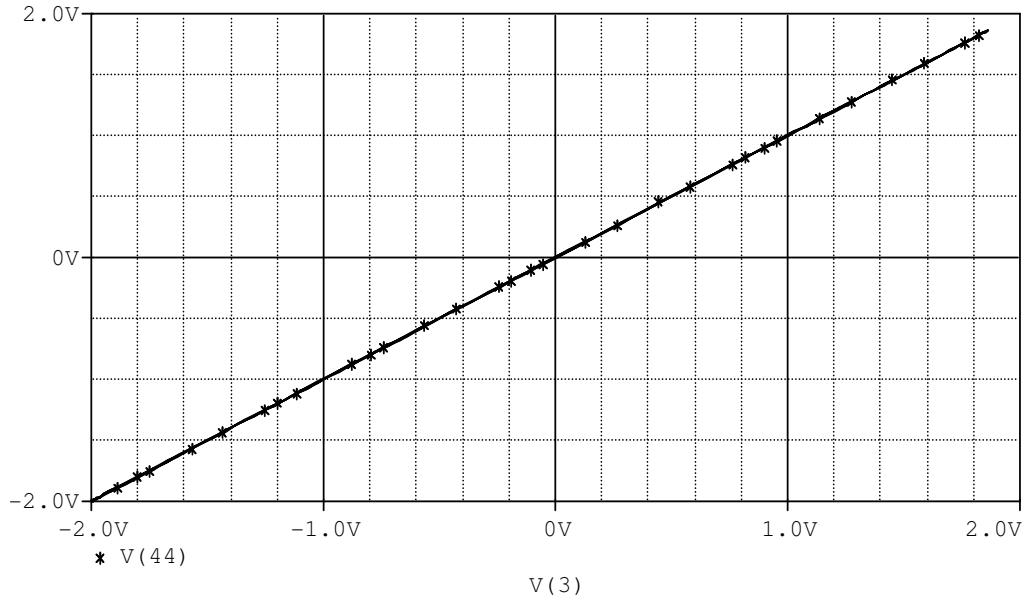

Figure 4.48 DC characteristic between V_W and V_Z.

Figure 4.49 shows the AC characteristic between X and Y voltages. It is seen from this figure that the relation between these voltages given in Equation (2.7) is verified up to 50MHz. In the same way Figure 4.50 shows the I_X-I_Z AC characteristic. It illustrates that the relation between I_X-I_Z up to 100MHz as it is expected. Figure 4.51 shows the V_W-V_Z AC characteristic and illustrates the relation

between the voltages at Z and W terminals. These figures confirm that the proposed CMOS ICFOA– circuit works properly.

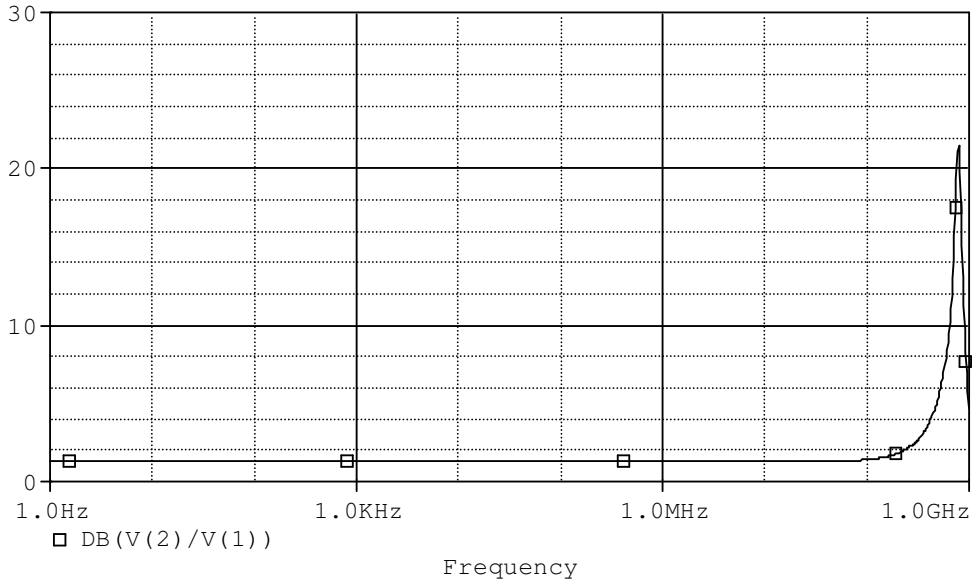

Figure 4.49 AC characteristic between V_X and V_Y.

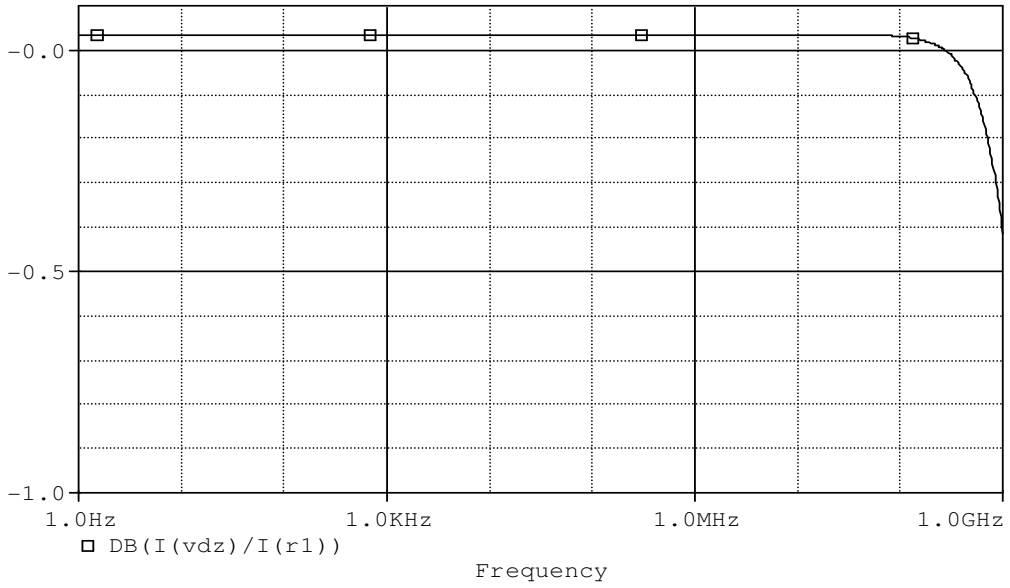

Figure 4.50 AC characteristic between I_Z and I_X.

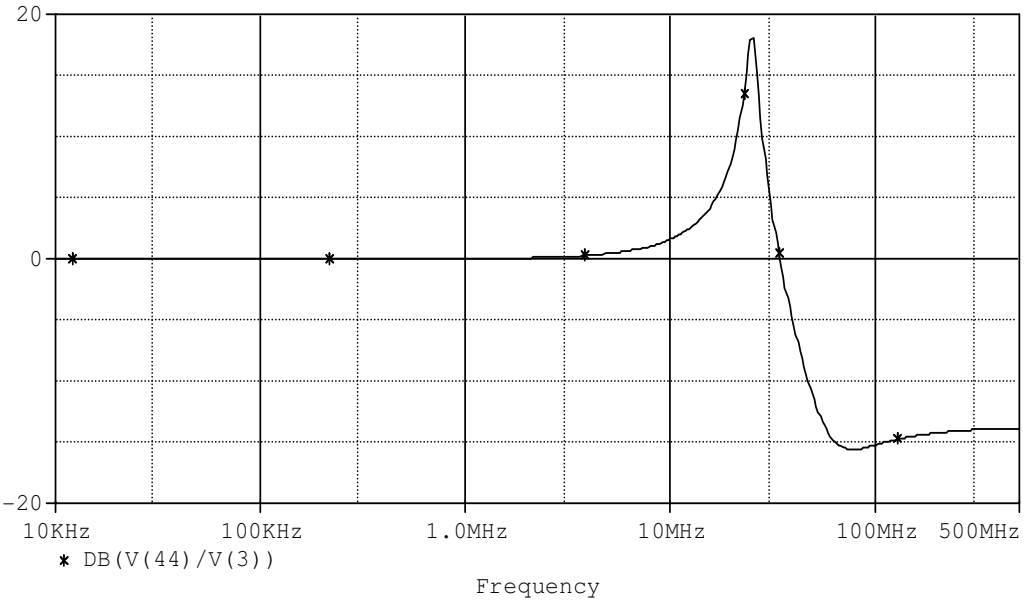

Figure 4.51 AC characteristic between V_W and V_Z.

Figure 4.52 shows the frequency responses of the impedance at terminal X. The resistance value at terminal X between 1Hz-10kHz is 108Ω, at 100kHz, 1MHz, 10MHz and 100MHz is 95Ω, 94Ω, 111Ω, 620Ω, respectively. These values show that the resistance value is small for low frequencies as expected. Figure 4.53 shows the frequency responses of the impedance at terminal Y. The resistance value at terminal Y at 1Hz, 10Hz, 100Hz, 1kHz, 10kHz, 100kHz, 1MHz, 10MHz, 100MHz is 282TΩ, 28TΩ, 2.8TΩ, 282GΩ, 28GΩ, 2.8GΩ, 282MΩ, 28.2MΩ, 2.8MΩ, respectively. These values verify the feature of this port; its input current is equal to zero. Figure 4.54 shows the frequency responses of the impedance at terminal Z. The resistance value at terminal Z between 1Hz-10MHz is 77kΩ, at 100MHz, is 33kΩ. Similarly these values verify the feature of this port; the high impedance output. Figure 4.55 shows the frequency responses of the impedance at terminal W. The resistance value at terminal W between 1Hz-10kHz is 66.6MΩ, at 100kHz, 1MHz, 10MHz, 100MHz, is 58MΩ, 11.5MΩ, 1MΩ, 108kΩ, respectively.

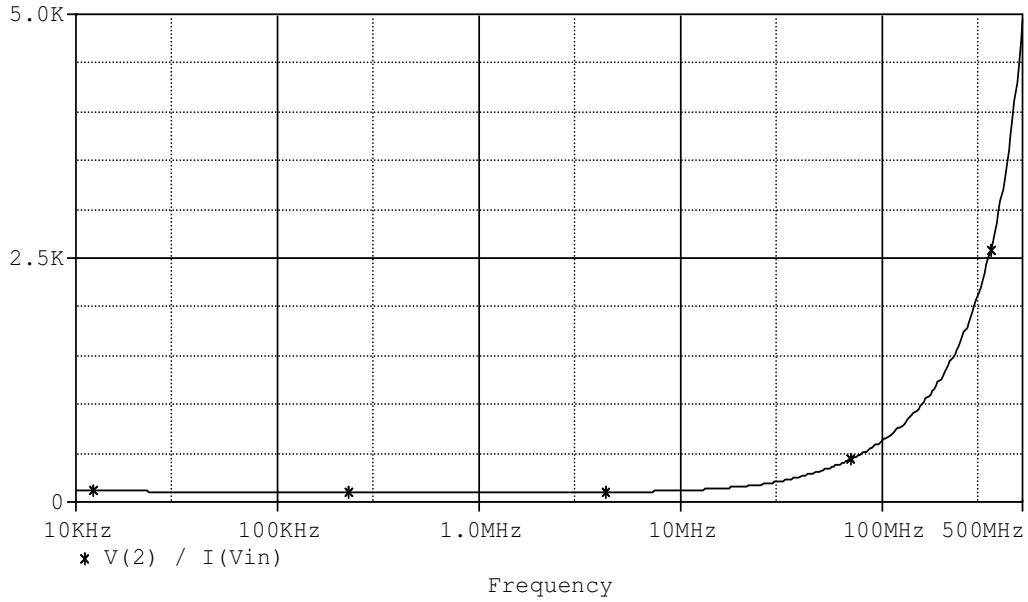

Figure 4.52 Impedance when looking at terminal X.

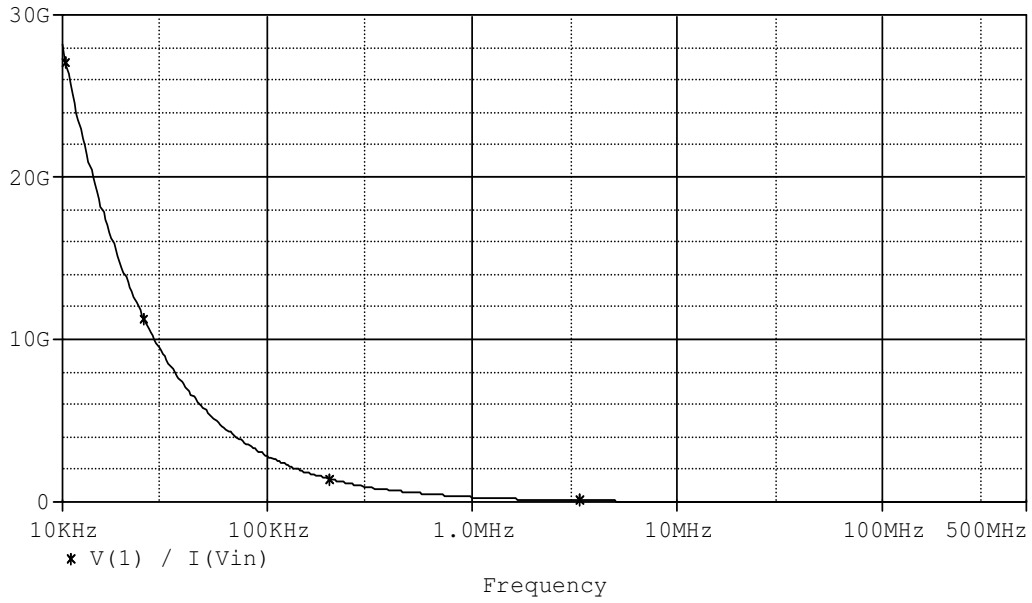

Figure 4.53 Impedance when looking at terminal Y.

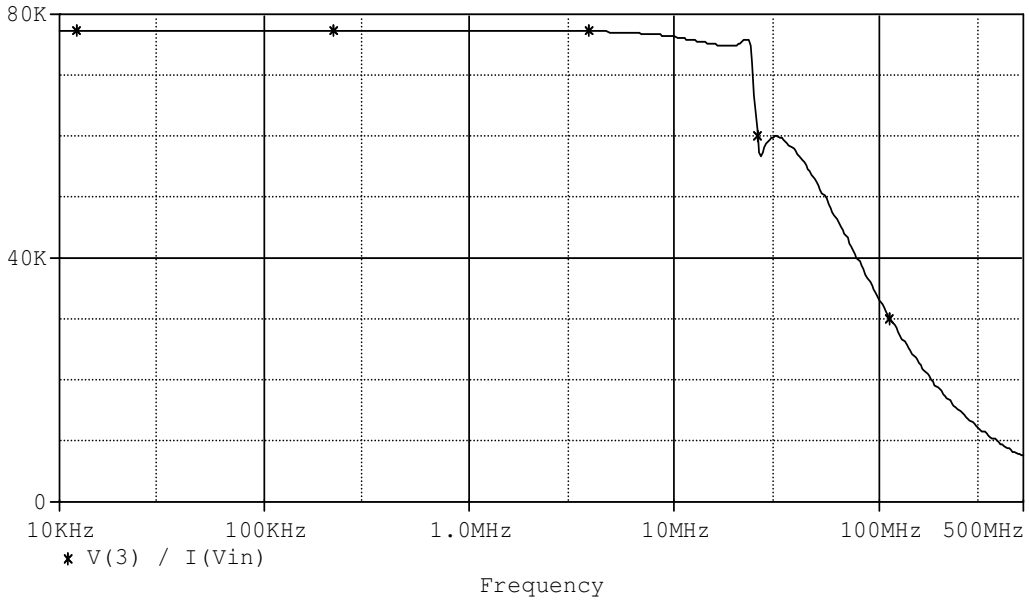

Figure 4.54 Impedance when looking at terminal Z.

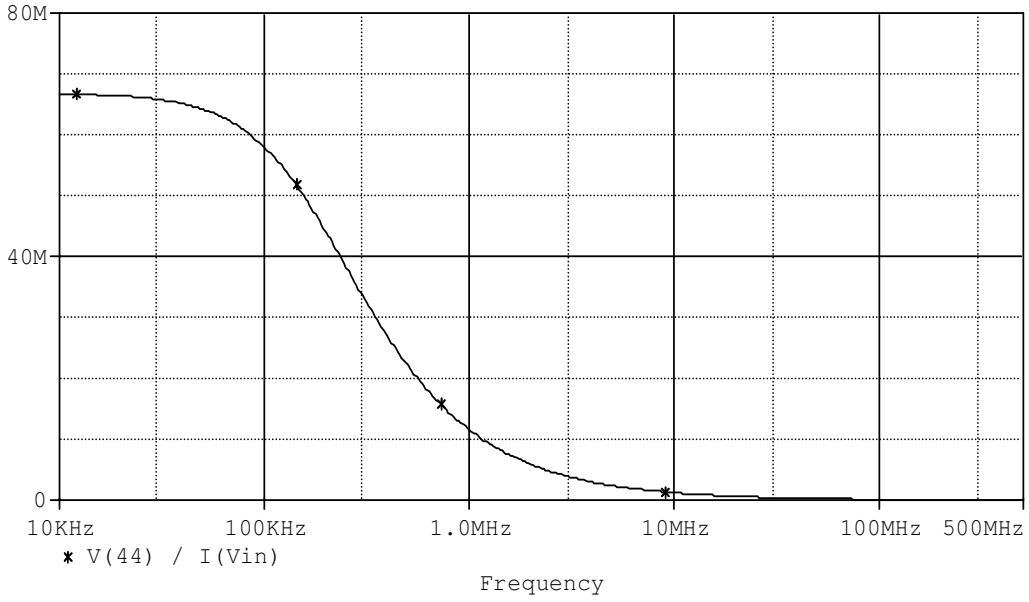

Figure 4.55 Impedance when looking at terminal W.

4.1.6 The Third CMOS ICFOA– Design

Another CMOS realization of ICFOA– obtained by cascading the ICCII– in Awad & Soliman (1999), and the buffer in Gupta & Senani (2005). The performance of the proposed CMOS realization is simulated using SPICE program with 0.35µm

and 1.2µm CMOS process parameters. The aspect ratios of the MOS transistor in the circuit are given in Table 4.7. The supply voltages (VDD, VSS) are taken as ±2.5V and bias voltages are ±VB= ±3.5V, ±VC= ±0.6V, VBB=–2.0139V.

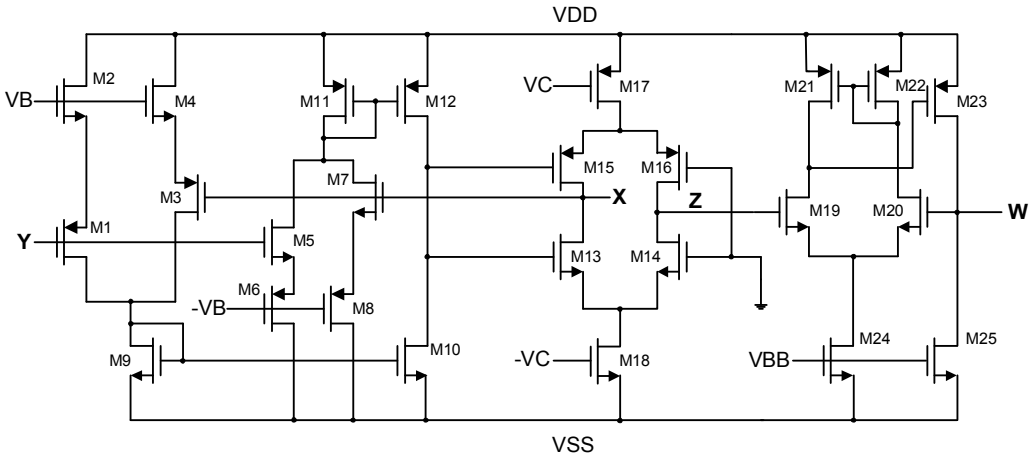

Figure 4.56 The third CMOS ICFOA– design.

Table 4.7 Transistor dimensions of the third CMOS ICFOA–

TRANSISTORS	W(µm)	L(µm)
M1	200	2.8
M2	130	3.6
M3	140	2.8
M4	93	3
M5	130	3.6
M6-M8	120	3.6
M9-M10	30	3.6
M11-M12	90	1.2
M13-M14	40	1.2
M15-M16	120	1.2
M17	200	3.6
M18	70	3.6
M19	35	0.35
M20-M21	24	0.35
M22	60	1.5
M23	15	1.5
M24-M25	10	1.5

Figure 4.57 shows the DC relation between Y and X terminal voltages. The input voltage is applied on terminal Y and the output voltage is obtained on terminal X with an infinite resistance connected at the X and terminal Z being grounded. Figure

4.58 shows I_X-I_Z DC characteristic of the circuit. A linear current flowing over a wide current range can be seen from this figure. This figure depicts the I_Z=–I_X relation. Figure 4.59 shows the DC relation between the voltages at W and Z terminals, V_W and V_Z. As seen from the figure these voltages show a linear relation as expected for a wide range of voltage.

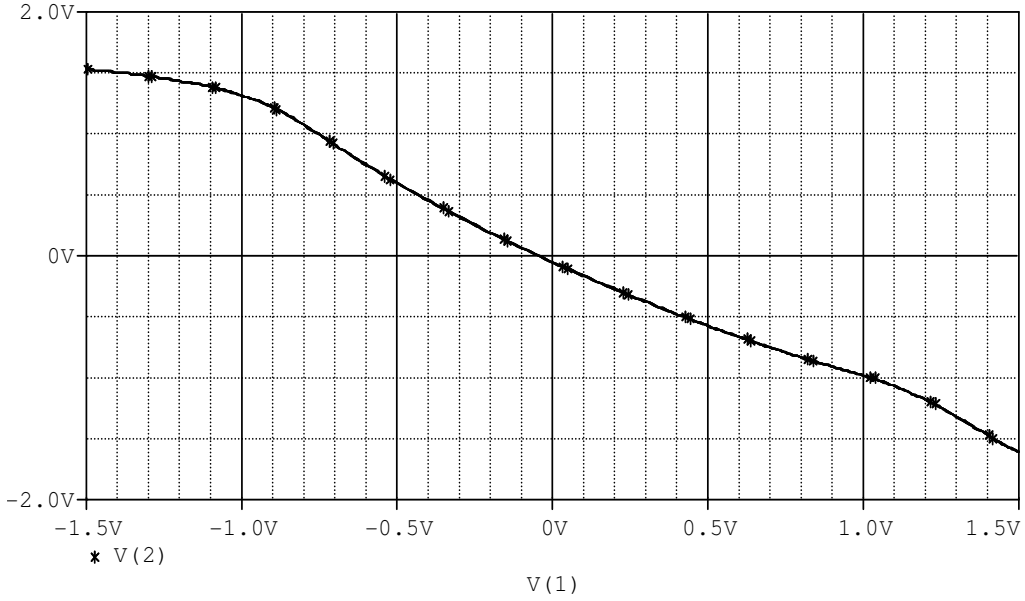

Figure 4.57 DC characteristic between V_X and V_Y.

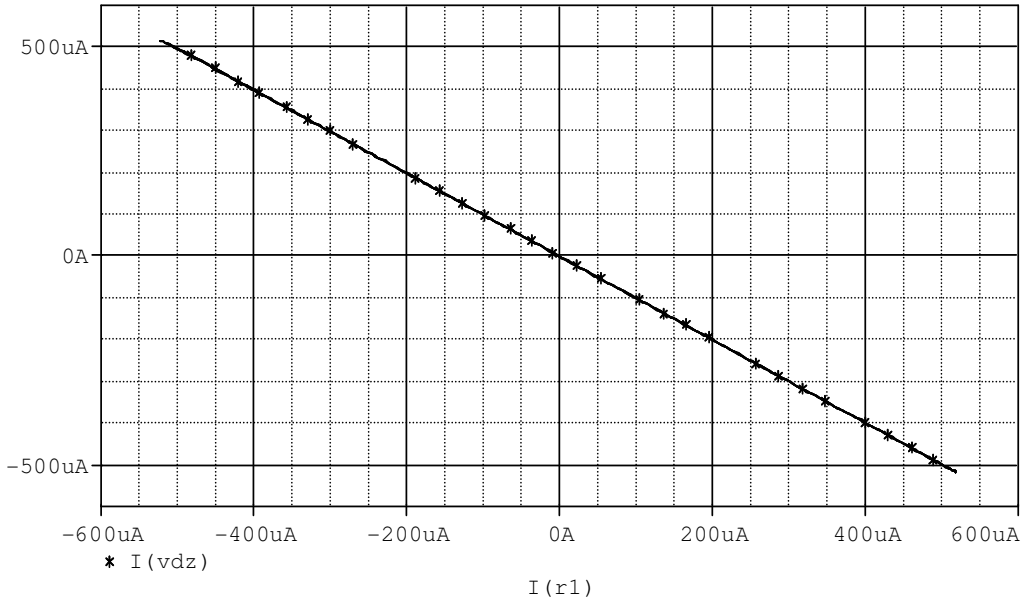

Figure 4.58 DC characteristic between I_Z and I_X.

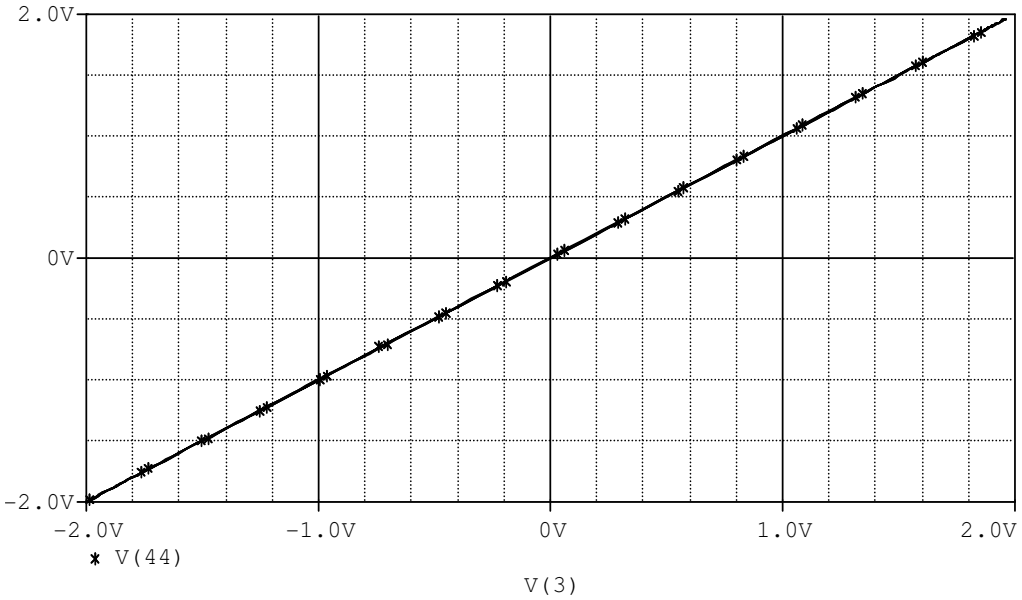

Figure 4.59 DC characteristic between V_W and V_Z.

Figure 4.60 shows the AC characteristic between X and Y voltages. It is seen from this figure that the relation between these voltages given in Equation (2.7) is verified up to 50MHz. In the same way Figure 4.61 shows the I_X-I_Z AC characteristic. It illustrates that the relation between I_X-I_Z up to 100MHz as it is expected. Figure 4.62 shows the V_W-V_Z AC characteristic and illustrates the relation between the voltages at Z and W terminals. These figures confirm that the CMOS ICFOA– works properly.

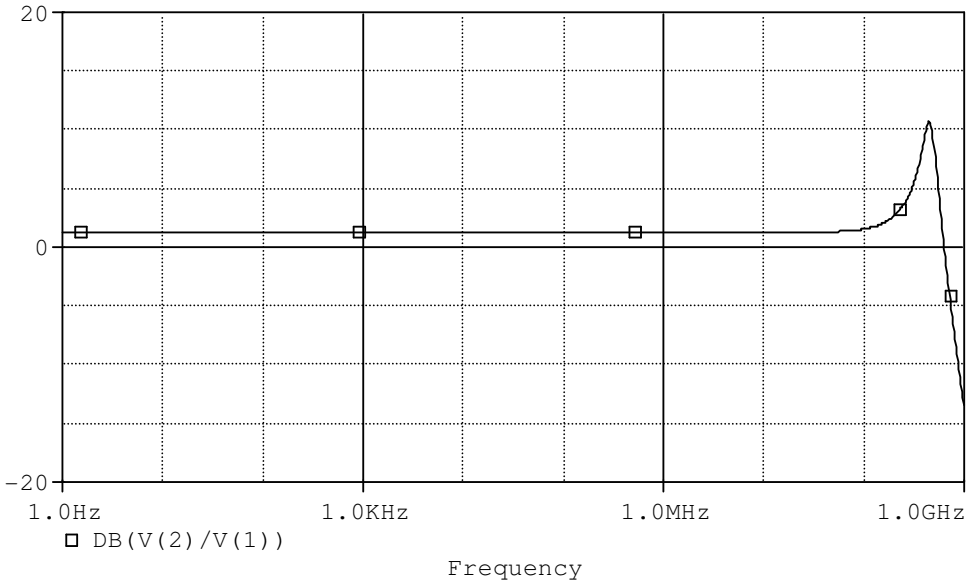

Figure 4.60 AC characteristic between V_X and V_Y.

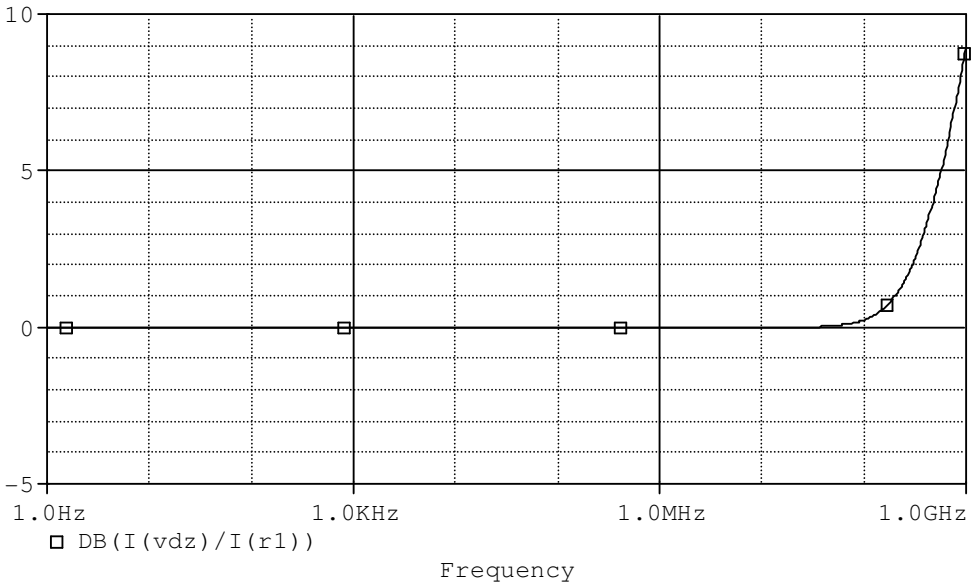

Figure 4.61 AC characteristic between I_Z and I_X.

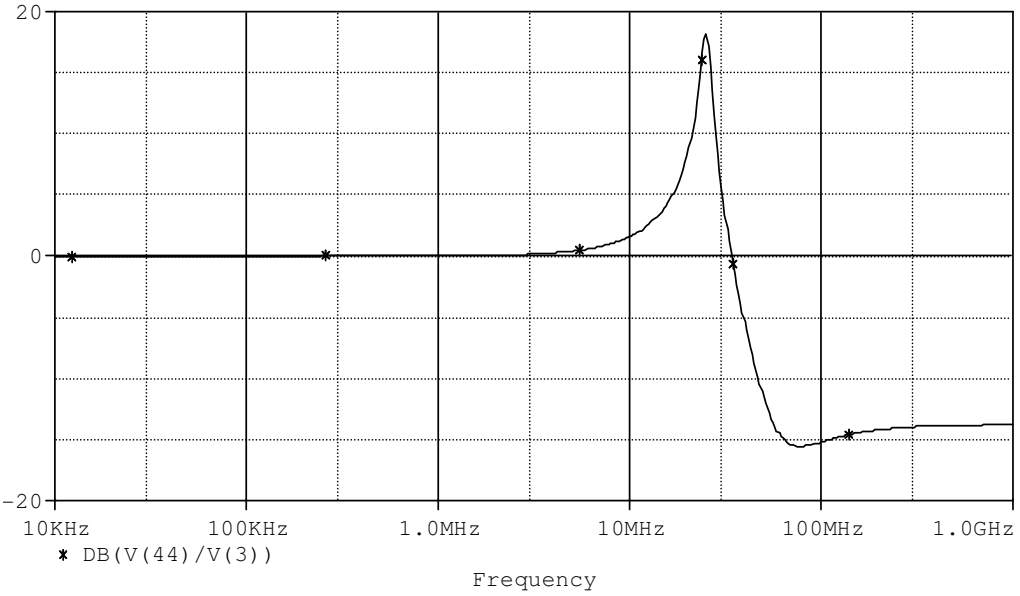

Figure 4.62 AC characteristic between V_W and V_Z.

Figure 4.63 shows the frequency responses of the impedance at terminal X. The resistance value at terminal X between 1Hz-10MHz is 330Ω, at 100MHz is 236Ω. These values show that the resistance value is small for low frequencies as expected. Figure 4.64 shows the frequency responses of the impedance at terminal Y. The resistance value at terminal Y at 1Hz, 10Hz, 100Hz, 1kHz, 10kHz, 100kHz, 1MHz, 10MHz, 100MHz is 336.6GΩ, 33.6GΩ, 3.36Ω, 336.6MΩ, 33.6MΩ, 3.36MΩ, 336.56kΩ, 33.56kΩ, 3.35kΩ, respectively. These values verify the feature of this port; its input current is equal to zero. Figure 4.65 shows the frequency responses of the impedance at terminal Z. The resistance value at terminal Z between 1Hz-100kHz is 2.9 MΩ, at 1MHz, 10MHz, 100MHz, is 2.46MΩ, 452kΩ, and 42.5kΩ, respectively. Similarly these values verify the feature of this port; the high impedance output. Figure 4.66 shows the frequency responses of the impedance at terminal W. The resistance value at terminal W between 1Hz-10kHz is 66.6MΩ, at 100kHz, 1MHz, 10MHz, 100MHz, is 58MΩ, 11.521MΩ, 1.16MΩ, 110.8kΩ, respectively. The features of proposed CMOS ICFOA– circuits can be compared as shown in Table 4.8.

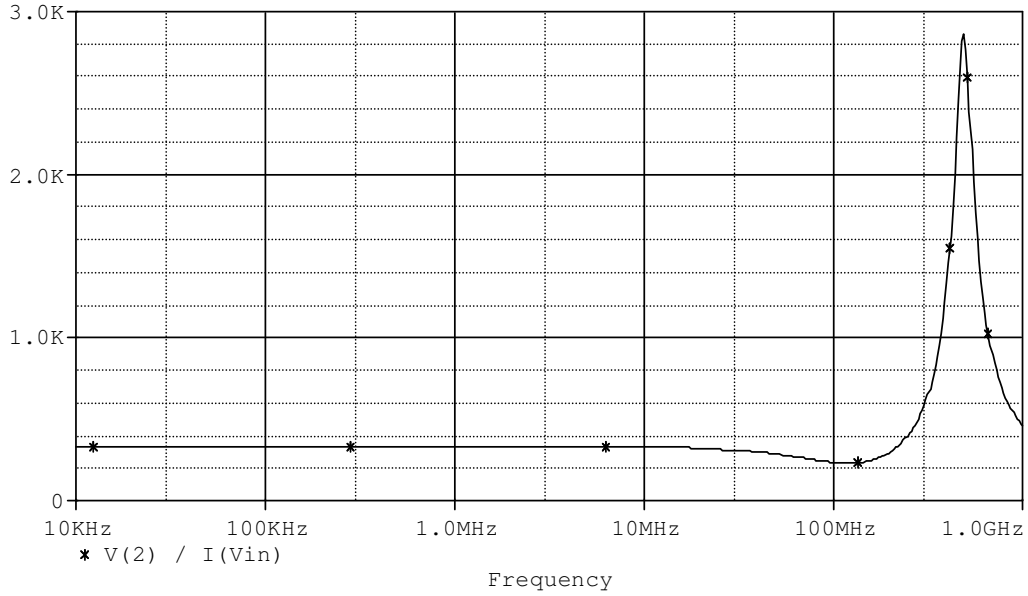

Figure 4.63 Impedance when looking at terminal X.

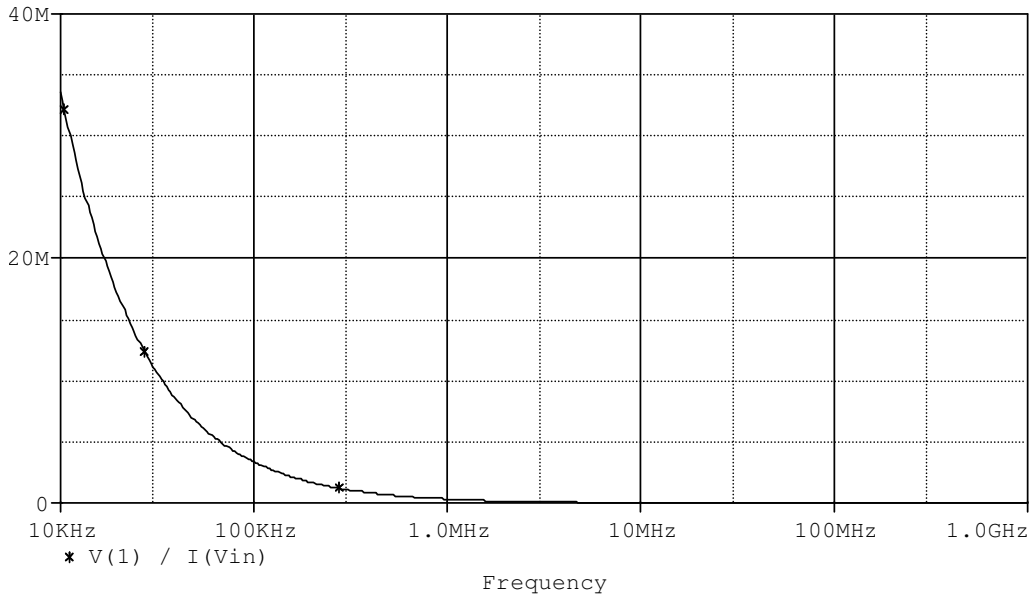

Figure 4.64 Impedance when looking at terminal Y.

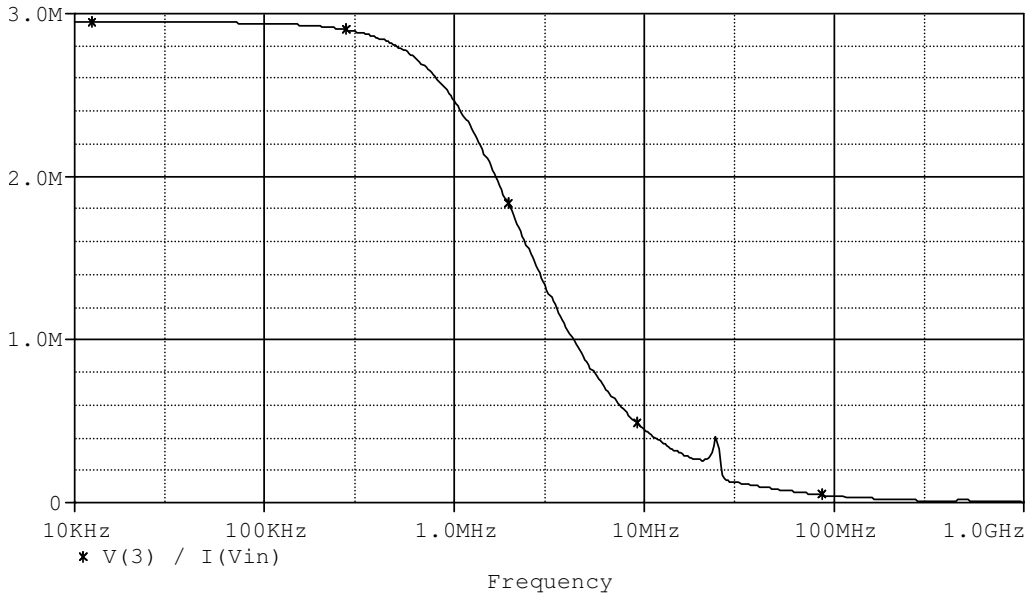

Figure 4.65 Impedance when looking at terminal Z.

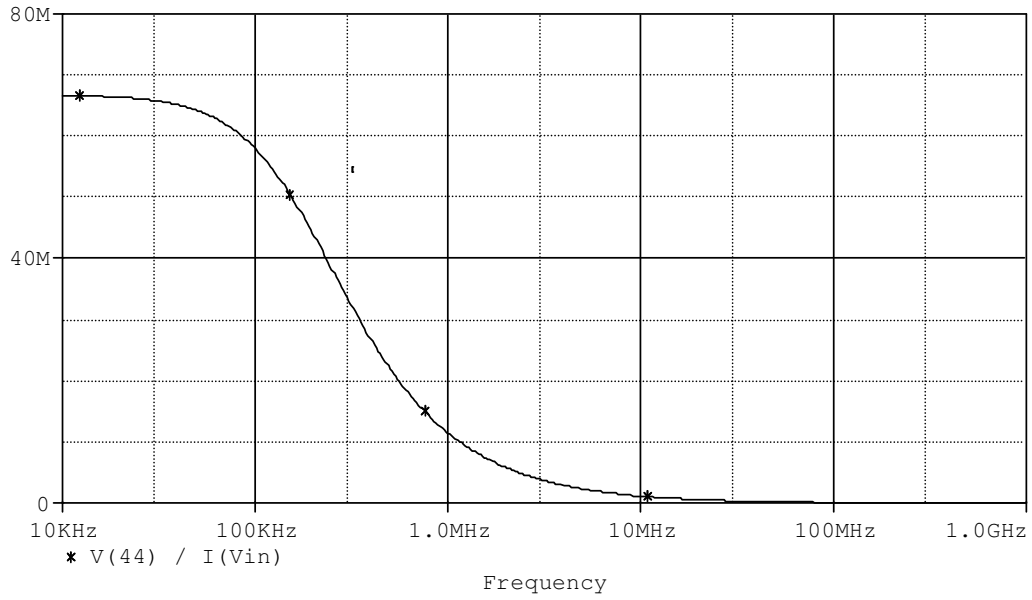

Figure 4.66 Impedance when looking at terminal W.

Table 4.8. Features of CMOS ICFOA– circuits

	The first ICFOA–	The second ICFOA–	The third ICFOA–
Slew rate	15.23 V/µs	16.58 V/µs	17.8 V/µs
Bandwidth V_X-V_Y	804MHz	347.5MHz	220MHz
Bandwidth I_Z-I_X	>1GHz	>1GHz	386MHz
Bandwidth V_W-V_Z	13.43MHz	13.43MHz	13.49MHz
R_X at f=10kHz	25.198kΩ	108Ω	330Ω
R_Y at f=10kHz	704.513MΩ	28GΩ	33.6GΩ
R_Z at f=10kHz	146.864MΩ	77kΩ	2.9MΩ
R_W at f=10kHz	66.674Ω	66.6MΩ	66.6MΩ

4.2 ICFOA Based Biquadratic Filters

Analog filters are important building blocks which are used in signal processing systems in electronics. Analog filters are used to pass the required frequency components and to reject other frequency components. The second order active filters are mostly implemented by using voltage mode active elements in the literature. But due to the limited bandwidth of voltage mode active elements, designing analog filters at high frequencies is not easy.

Proposed general configuration for the ICFOA filters is shown in Figure 4.67. Routine analysis yields the transfer function as:

$$\frac{V_{out}}{V_{in}} = \frac{Y_1(Y_3 - Y_5 - Y_6)}{(Y_1 + Y_2 + Y_3)(Y_3 + Y_4 + Y_6) - Y_3(Y_3 - Y_5 - Y_6)} \tag{4.1}$$

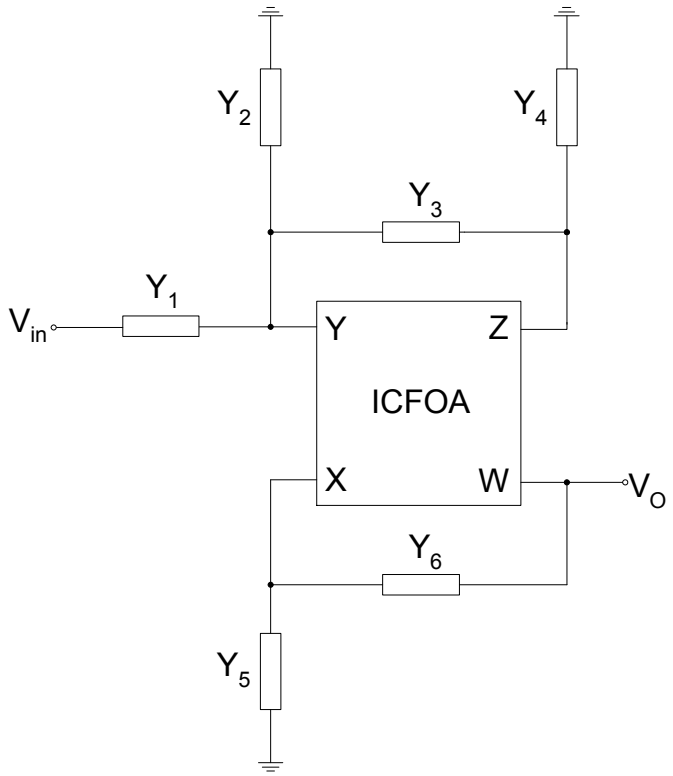

Figure 4.67 Filter configuration.

Choosing appropriate admittance combination in Equation (4.1), five different types of filters, low-pass, high-pass, band-pass, all-pass and notch, can be obtained. The admittance combinations and the types of filters which obtained by this combinations can be given as in Table 4.9. Natural frequency, quality factor and the gain of the filters can be given as in Table 4.10. For all-pass and notch filters the following conditions must be achieved respectively.

$$C_5G_5 = 2(C_3G_5 + C_5G_3) \tag{4.2}$$

$$C_5G_5 = (C_3G_5 + C_5G_3) \tag{4.3}$$

Table 4.9 Second-order filters obtained from Equation (4.1)

Filter	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6
Low-pass	G_1	sC_2	0	sC_4	0	G_6
High-pass	sC_1	G_2	0	G_4	0	sC_6
Band-pass	sC_1	G_2	0	sC_4	0	G_6
All-pass	∞	0	sC_3+G_3	0	$1\Big/\left(\frac{1}{G_5}+\frac{1}{sC_5}\right)$	0
Notch	∞	0	sC_3+G_3	0	$1\Big/\left(\frac{1}{G_5}+\frac{1}{sC_5}\right)$	0

Table 4.10 Natural frequency, quality factor and gain of the proposed filters obtained from Figure 4.67

Filter	Natural frequency	Quality factor	Gain
Low-pass	$\sqrt{\frac{G_1G_6}{C_2C_4}}$	$\frac{\sqrt{G_1G_6C_2C_4}}{C_4G_1+C_2G_6}$	1
High-pass	$\sqrt{\frac{G_2G_4}{C_1C_6}}$	$\frac{\sqrt{G_2G_4C_1C_6}}{C_1G_4+C_6G_2}$	1
Band-pass	$\sqrt{\frac{G_2G_6}{C_1C_4}}$	$\frac{\sqrt{G_2G_6C_1C_4}}{C_1G_6+C_4G_2}$	$\frac{C_1G_6}{C_1G_6+C_4G_2}$
All-pass	$\sqrt{\frac{G_3G_5}{C_3C_5}}$	$2\sqrt{\frac{G_3C_3}{C_5G_5}}$	1
Notch	$\sqrt{\frac{G_3G_5}{C_3C_5}}$	$\sqrt{\frac{G_3C_3}{C_5G_5}}$	1

To verify the theoretical study, the presented filters were simulated by using PSPICE program. Supply voltages were taken as ±2.5V. Simulation results using ideal and CMOS ICCII are shown in Figures 4.68-4.72. All resistor and capacitor values were taken as 10kΩ and 10pF. These component values result in natural frequency of 1.59MHz. The PSPICE simulations were performed using a CMOS realization of ICFOA which proposed in this thesis which is shown in Figure 4.1, with the same transistor aspect ratios and process parameters as in Table 4.1.

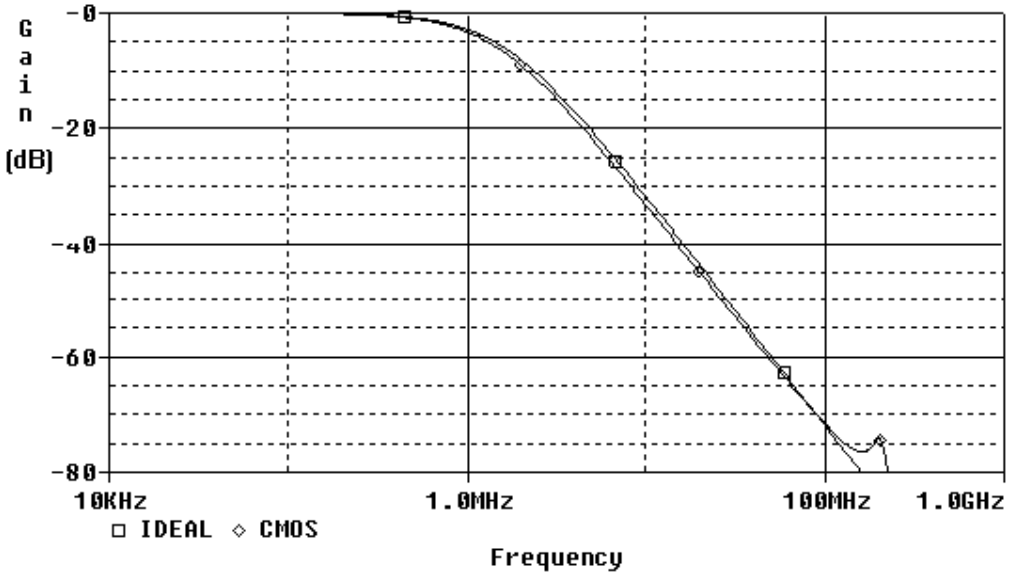

Figure 4.68 PSPICE simulation results of the low-pass filter.

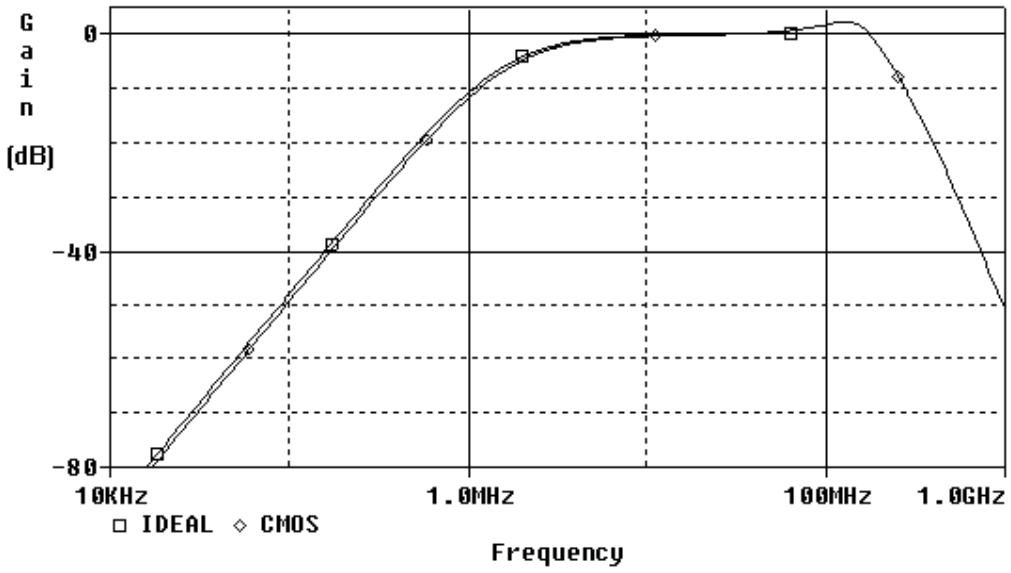

Figure 4.69 PSPICE simulation results of the high-pass filter.

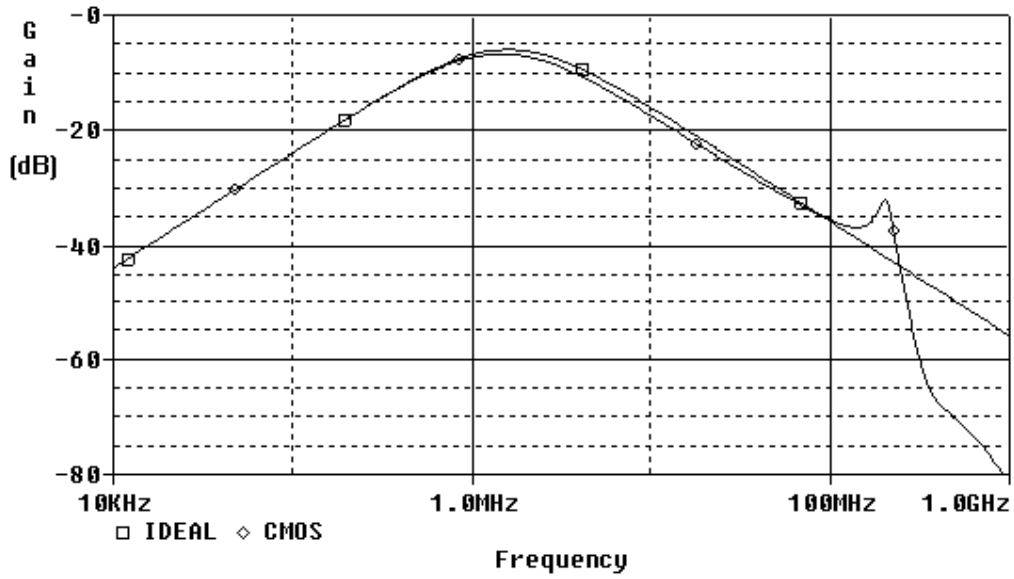

Figure 4.70 PSPICE simulation results of the band-pass filter.

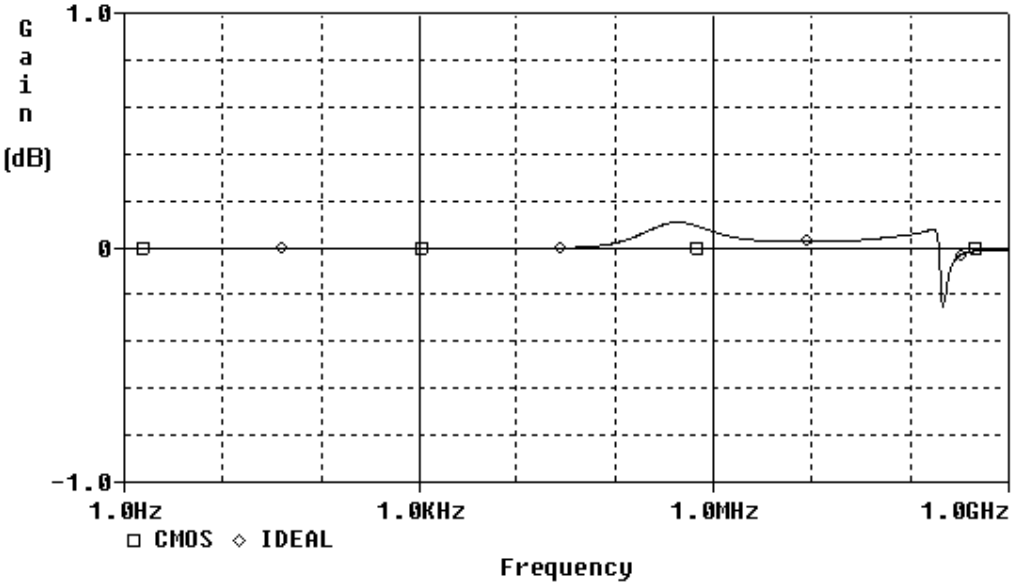

Figure 4.71 PSPICE simulation results of the all-pass filter.

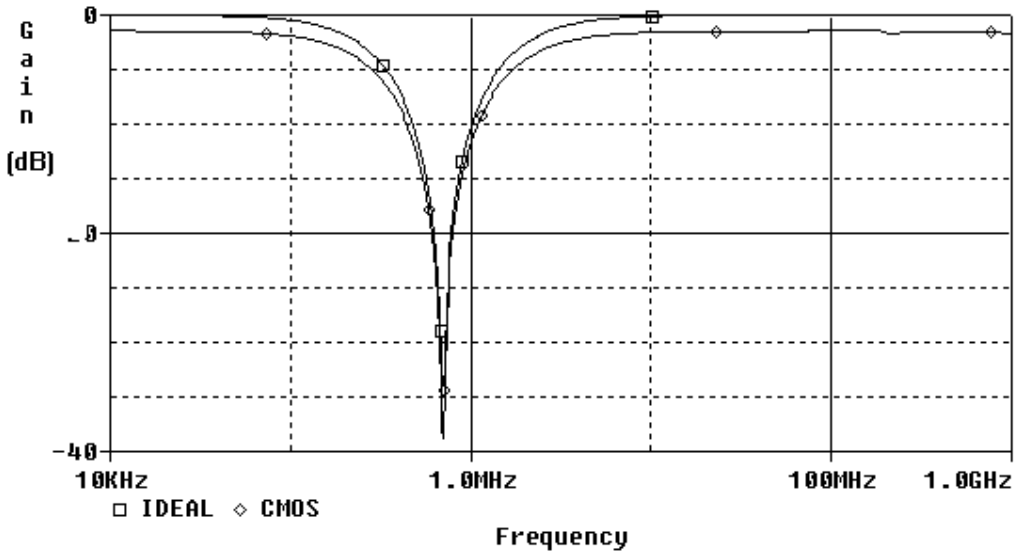

Figure 4.72 PSPICE simulation results of the circuit notch filter.

CHAPTER FIVE
CONCLUSION

In this thesis, analog circuit design using ICCII and ICFOA active elements is considered. These active elements are current mode building blocks. ICCII has high impedance output and mostly has found applications in the field of current mode analog circuit design than voltage mode circuits. Due to its high impedance output, it is not suitable for cascade connection in voltage mode circuit as with CCII. In order to overcome this problem another output terminal having low impedance is added as it is done for CFOA. The CMOS realization of ICFOA is obtained using a CMOS realization of ICCII as a core followed by a CMOS voltage buffer. Due to its low impedance output, it is suitable for voltage mode circuits.

Since its input terminals are at opposite potentials, ICCII is more suitable for synthesis of all-pass and notch filters than CCII. In this thesis, ICCII based first order all-pass filter and ICCII based quadrature oscillator are presented. These circuits are simulated using PSPICE program and in the simulations a CMOS realization of ICCII is used. Also, ICCII based first order all-pass filter and ICCII based quadrature oscillator are tested experimentally using the AD844 implementation of the ICCII element.

Furthermore, totally six ICFOA CMOS realizations, three for ICFOA+ and three for ICFOA–, are presented in this thesis. The presented CMOS realizations are simulated using PSPICE program with suitable supply voltages and aspect ratios of transistors. ICFOA based biquadratic filter topology is presented as an application example. The filter circuits, which are obtained from this topology, are simulated using PSPICE program. In the simulations, the CMOS realization of ICFOA+ is used.

As future works, some attempts can be done to improve the performance of these CMOS realizations and to introduce other CMOS realizations of ICFOA. Also Bipolar and BiCMOS realizations of ICFOA can be presented and the performance

of these technologies can be compared. Many new ICFOA based analog signal processing applications can be given. ICCII and ICFOA can be used as an active element in chaotic signal generator circuit instead of op-amp. Also, analog design of fuzzy controllers and neural networks can be considered.

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