DOKUZ EYLÜL UNIVERSITY
GRADUATE SCHOOL OF NATURAL AND APPLIED SCIENCES

THE DESIGN OF A TEST METHOD TO IDENTIFY RELIABILITY PROBLEMS OF CONSUMER ELECTRONIC PRODUCT DURING EARLY PHASES OF DEVELOPMENT

by
Ali Tarkan TEKCAN

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İZMİR

THE DESIGN OF A TEST METHOD TO IDENTIFY RELIABILITY PROBLEMS OF CONSUMER ELECTRONIC PRODUCT DURING EARLY PHASES OF DEVELOPMENT

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We have read the thesis entitled **"THE DESIGN OF A TEST METHOD TO IDENTIFY RELIABILITY PROBLEMS OF CONSUMER ELECTRONIC PRODUCT DURING EARLY PHASES OF DEVELOPMENT"** completed by **ALİ TARKAN TEKCAN** under supervision of **PROF. DR. MUSTAFA GÜNDÜZALP** and we certify that in our opinion it is fully adequate, in scope and in quality, as a thesis for the degree of Doctor of Philosophy.

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THE DESIGN OF A TEST METHOD TO IDENTIFY RELIABILITY PROBLEMS OF CONSUMER ELECTRONIC PRODUCT DURING EARLY PHASES OF DEVELOPMENT

ABSTRACT

The rapid advances in technology, the increase on the number of manufacturers and high consumer expectations make today's consumer electronics market highly competitive. Under these competitive market conditions, companies try to keep and increase their quality and reliability level of their products. Design to manufacturing time is becoming shorter and shorter. The classical approach for reliability testing cannot maintain desired reliability levels for products due to rapid changes on design such as cost down works, alternative components and additional new features and also such methods cannot respond with enough speed. A new approach for reliability must be developed in order to get trouble-free and robust products, which satisfy customer needs for a long time and this approach must show how reliable the new product is against the old one. A novel parameter, called maturity level (ML) or failure risk factor (FRF), which is given by 1-ML, is demonstrated to incorporate such factors and it is combined with traditional reliability prediction methods. Specifically, the new approach takes into account the qualitative reliability tests, which include hardware and software tests, performed during the research and development (R&D) stage and combines them with the other reliability prediction methods by using basic approaches.

As a result, the new approach gives more accurate predictions compared with traditional prediction methods. Therefore, reliability analysts can determine the reliability and return rate of their products more accurately with this prediction model.

Keywords: Consumer electronics, reliability, estimation, artificial neural networks, maturity level, product robustness, field failures, product level testing, board level testing, design quality

TÜKETİCİ ELEKTRONİĞİNDE TASARIM ERKEN DÖNEMLERİNDE GÜVENİLİRLİK PROBLEMLERİNİN BELİRLENMESİ AMACIYLA TEST METOTLARININ TASARLANMASI

ÖZ

Günümüzde tüketici elektroniği pazarı, hızla gelişen teknoloji, artan üretici sayısı ve yüksek müşteri beklentileri sebebiyle aşırı rekabetçi hale gelmiştir. Bu rekabetçi pazar koşulları altında şirketler ürünlerinin kalitesini ve güvenilirlik seviyesini korumaya ve geliştirmeye çalışmaktadırlar. Ürünlerin tasarımda üretime geçiş zamanları oldukça kısalmıştır. Maliyet düşürme çalışmaları, alternatif malzemeler, yeni ek özellikler gibi hızlı tasarım değişiklikleri sebebiyle güvenilirlik testlerinde kullanılan klasik yaklaşım, ürünler için istenilen güvenilirlik seviyesini sağlayamaz ve ihtiyaçlara yeterli hızda cevap veremez hale gelmiştir. Müşterinin ihtiyaçlarını uzun süre karşılayabilen hatalarından arındırılmış ve sağlam ürünler geliştirmek ve yeni ürünlerin güvenilirliklerini eski ürünler ile karşılaştırabilmek amacıyla güvenilirlik için yeni bir metot geliştirme ihtiyacı oluşmuştur. Bu faktörleri birleştiren, Olgunluk Seviyesi veya Hata Risk Faktörü isimli, yeni bir parametre geliştirilmiştir ve sonrasında bu parametre klasik güvenilirlik tahmin metotlarıyla birleştirilmiştir. Özellikle yeni yaklaşım AR-GE aşamasında yapılan, donanım ve yazılım testlerinden oluşan, nitel güvenilirlik testlerini ele almaktadır ve basit matematiksel yaklaşımlar ile diğer güvenilirlik tahmin metotları ile birleştirilmişlerdir.

Sonuç olarak, yeni yaklaşımın klasik tahmin metotlarına göre daha kesin tahmin sonuçları vermesi beklenmektedir. Bu tahmin modeliyle güvenilirlik analistleri, ürünlerinin güvenilirliklerini ve geri dönüş oranlarını hakkında daha kesin tahminlerde bulunabileceklerdir.

Anahtar sözcükler: Tüketici elektroniği, güvenilirlilik, tahmin, yapay sinir ağları, olgunluk seviyesi, ürün sağlamlığı, sahada karşılaşılan hatalar, ürün seviyesinde test, kart seviyesinde test, tasarım kalitesi

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CHAPTER ONE
INTRODUCTION

Reliability is a time related function that expresses the probability of performing functions without failure in specified environments for desired time period.

"Reliability is the best quantitative measure of the integrity of a designed part, component, product, or system. Reliability is the probability that parts, components, products, or systems will perform their designed-for functions without failure in specified environments for desired periods at a given confidence level (Kececioglu, 2002)."

"Reliability engineering provides the theoretical and practical tools whereby the probability and capability of parts, components, equipment, products, and systems to perform their required functions for desired periods of time without failure, in specified environments and with a desired confidence, can be specified, predicted, designed in, tested, demonstrated, packaged, transported, stored, installed, and started up, and their performance monitored and fed back to all concerned organizations (Kececioglu, 2002)."

Companies need to control the reliability of their products to ensure the balance between design cost and service cost. If a product is designed to have a very high reliability, to get a very low service cost, then the design cost will increase dramatically. On the other side, if a product is supposed to be designed with a very low design cost, then, the reliability of the product could be very low. This low reliability could result a very high service cost. Therefore, the optimal point between design cost and service cost should be adjusted carefully. This clarification can only be done with a strict reliability test program and an accurate reliability prediction method.

This process is composed by a series of reliability tests, procedures and lastly, calculations and analysis. All kind of reliability problems found by production

quality, outgoing quality, third party customers and end users are well noted, and test procedures can be scrutinized. Also, market returns data is taken as a feedback to recheck our calculation and corrective data for test procedures.

There are many available methods and standards in the literature to predict reliability (Eames, 1978; Zhengguo, Yindong, & Donghua, 2009; Pecht & Kang, 1988; Roca, 1988; Pecht & Nash, 1994; Roca, 1988; Ormon, Cassady, & Greenwood, 2002; Jones & Hayes, 1999; Jones & Hayes, 2001; Goel & Graves, 2006). Stress based standards are the ones which are generally used (Harms, 2010; Harb & Balog, 2012; Vannoy, 1990; Mroczkowski & Maynard, 1991; Chan & Calleja, 2011; Fong & Li, 2012). Furthermore, most of the companies perform accelerated life tests (ReliaSoft Corporation, 2012) and analyze their test data with statistical distributions (Ruan, et al., 2012; Yuan, Liu, & Kuo, 2012; Yu & Chang, 2012; Zhang, et al., 2012; Benavides, 2011; Fan & Wang, 2011; Han & Naredran, 2011; Yang, 2010). However, predicted reliability and return rate value by using stress based standards or applying accelerated life tests are frequently different from the real reliability and return rate value (Jones & Hayes, 1999). One reason for this is that companies cannot afford enough number of samples/prototypes available for testing and this situation forces them to plan accelerated life tests with small sample size (Ma & Meeker, 2010). In addition, based on past experiences, the main reason is that the stress factors mentioned in the standards and used in accelerated life tests are not the sole failure contributors faced in the field during the life period of the product. The main stress factors mentioned in stress based standards are temperature, voltage and power dissipation (Defense, U.D.o., 1995). In addition, the main stress factors used in accelerated life tests are temperature, relative humidity, voltage and vibration (Yang, 2005). However, those stress factors are not the only failure reasons of the products in the field. For example, electro static discharge (ESD), inrush current, voltage dips-interruptions-variations, lightning, loose plugs etc., can cause failures in the field (Imam, Divan, Harley, & Habetler, 2007; Divan, Bendre, & Joha, 2006; Steurer & Frohlich, 2002; Porter, 1965). The traditional methods do not consider these non-life related failure factors. Therefore, there should be a parameter which can express these failure mechanisms and this new parameter

should be combined with traditional prediction methods to predict the failure rate and reliability of the product more accurately.

In this thesis, the determination of reliability by failure rate estimation with a new parameter, i.e., maturity level (ML) and failure risk factor (FRF), which is expressed by 1-ML, in R&D phase, is introduced. This new parameter is obtained by applying a set of electrical, environmental and mechanical tests in R&D phase before mass production. This set of tests is created to simulate different stress factors and failure mechanisms faced in the field. These tests can also be the approval and validation tests both at the board and product level. In this thesis, for the first time, qualitative, non-life related failure factors are combined with life related failure factors. With the proposed method, engineers can determine the reliability of their designs more accurately.

The fundamental procedure, about assigning score points for the tests, is as the following. A scoring point is given to every test according to the severity of the test. The severity of the test can be decided by analyzing similar projects' field returns. A test which gives more information about failures will have higher scoring points. At the end, the total point of the tests is obtained. On the other hand, a losing point is given to every failure which is found during testing according to its severity. The severity of the failure can also be decided by analyzing similar projects' field returns. After all tests are performed, total losing points will be calculated. The new parameter mentioned above is defined as the ratio of losing points to total test points. Finally, a new parameter which can express different stress factors and failure mechanisms faced in the field is obtained. This new parameter is combined with failure rate calculations from traditional methods by using field return rate indicator (FRRI). Figure 1.1 shows the FRRI progress. Therefore, failure rate and return rate predictions are modified.

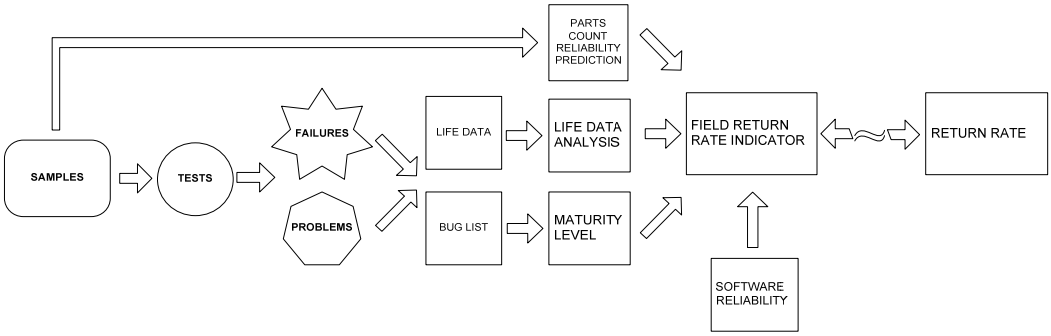

Figure 1.1 Field return rate indicator

In addition, two mathematical FRRI models of combination of this new parameter with stress based failure rate prediction and failure rate calculated by applying accelerated life tests are given with a real life case study. The results of these two methods and the comparison of the results with the real data are also given.

CHAPTER TWO
MATURITY LEVEL

In this chapter, firstly in Section 2.1, maturity level and failure risk factors are defined. Then, pass/fail tests are described in Section 2.2, early life period tests are given in Section 2.3 and design verification tests are introduced in Section 2.4. Total scoring points and total losing points are defined in Section 2.5 and finally, in Section 2.6, a real life case study to calculate maturity level and failure risk factor is given.

2.1 Determination of the New Parameters

To determine the mentioned new parameters, i.e., "Failure Risk Factor (FRF)" and "Maturity Level (ML)", a set of tests which can simulate the different failure modes faced in the field should be created according to type, specification, usage conditions, etc., of the product. In addition, tests and the failures found during testing should have numerical values according to their severities, to determine the risk of failure at the end of testing. These numerical values can be decided by analyzing field returns of similar products.

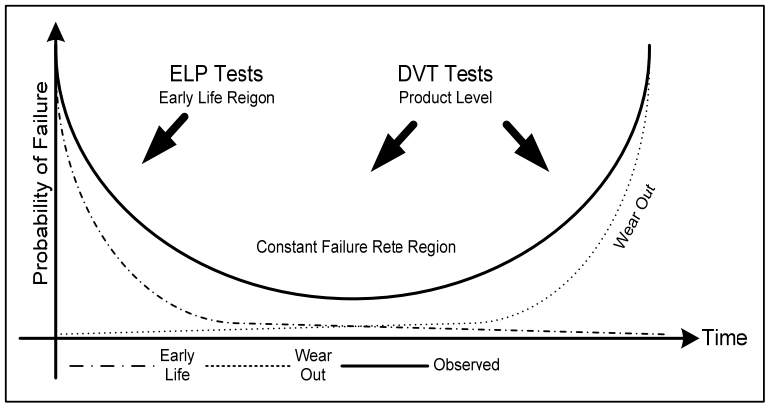

Figure 2.1 Bath tub curve and our test procedure

Figure 2.1 demonstrates where early life period (ELP) and design quality assurance (DQA) tests simulate or stimulate. The overall aim is to decrease the early life region, extend and decrease the level of constant failure rate region.

The calculation method of the new parameter for a LCD TFT TV set is given as a real case study. The test set consists of electrical, environmental and mechanical tests and these tests can further be grouped as pass/fail tests, early life period tests and design verification tests (Tekcan & Kirisken, 2010). All tests have "*scoring points*" and these points are given according to the severities of the tests. The severity of the tests can be decided by analyzing production line failures, field returns from similar projects etc. If a test is thought to be more effective, then this test will have higher scoring points. In addition to this, the failures found during testing are grouped according to their severities, as "showstopper," "high," "medium," and "low". Also, failure severities have "losing points" (Tekcan & Kirisken, 2010). These points are also decided by analyzing field returns of similar projects (De Visser, Yuan, & Nagappan, 2006).

FRF is the ratio of total losing points to the total scoring points. It is between 0 and 1and can be represented as the reverse of the Maturity Level as the following,

$$FRF = 1 - \text{Maturity Level (ML)} \quad (2.1)$$

2.2 Pass / Fail Tests

Pass/Fail tests are also referred to as "reliability approval tests". The main aim is to find major design failures. These tests are performed on a product level, and usually with a small sample size. The list of Pass/Fail tests for a LCD TFT TV set is given in Table 2.1.

Table 2.1 List of pass/fail tests

Test Category	Test Name	Scoring
Electrical	Voltage Current Stress Test	100
	Temperature Stress Test	100
	Open/Short Circuit Test	100
	ESD Test	100
	Surge Test	25
	Lightning Test	50

Table 2.1 Continued

Test Category	Test Name	Scoring
	Voltage Dips, Interruption and Variation	50
	Power On/Off Test	50
	Inrush Test	75
Environmental	Heat-Run Test	100
	High Temperature Test	50
	Low Temperature Test	50
	High Humidity Life Test	50
Mechanical	Vibration Test	25
	Wall Holder Strength Test	25
	Drop Test	50
	Total	**1000**

As it can be seen from Table 2.1, voltage current stress test, temperature stress test, open/short circuit test, ESD test and heat-run test have 100 points because they are very effective tests on finding failures for LCD TV sets.

2.3 Early Life Period Tests

Early life period (ELP) tests are performed with minimum 20 samples, on a board level. These tests are performed to determine component quality problems, assembly problems, solder-joint problems and failures occurred in early life period which are also known as infant mortality failures. The list of Early Life Period tests for a LCD TFT TV set is given in Table 2.2.

Table 2.2 List of early life period tests

Test Category	Test Name	Scoring Points
Environmental	Thermal Cycling Test	75
	High Temperature High Humidity	50
	Thermal Shock Test	50
Mechanical	Random Vibration Test	50
	Total	**225**

The most important stress factor for board level tests is thermal cycling. Because of this, thermal cycling test is given 75 scoring points.

2.4 Design Verification Tests

Design verification tests (DVTs) are not the same as approval tests. These tests give feedback to designers about the weakest points of the design. DVT is performed with large sample sizes on a product level and test period is longer than pass/fail tests. The main purpose of DVTs is to determine minor design problems. Combined stress factors are used to accelerate failure mechanism. The list of DVTs for a LCD TFT TV set is given in Table 2.3

Table 2.3 List of design verification tests

Test Category	**Test Name**	**Scoring Points**
Electrical	Powered / Unpowered Temperature Cycling Test	100
	ESD Step Stress to Failure Test	50
Environmental	Combined High Temperature High Humidity Test	50
	Thermal Shock Test	75
	Temperature Step Stress to Failure Test	50
	Operational High / Low Temperature Humidity Test	50
	High Humidity Storage Test	25
	Temperature Cycle Test	50
Mechanical	Constructional Inspection Test	50
	Unpackaged Shock Test	50
	Random Vibration Step Stress to Failure Test	25
	Total	**575**

Powered/unpowered temperature cycling test is a very effective test on finding failures as it includes 4 different types of failure factors; low temperature, high temperature, thermal cycling and power on/off cycles. Therefore, this test is given 100 scoring points. High humidity storage test and random vibration step stress to failure test are not so effective tests. Because of this, they are given 25 scoring points.

2.5 Total Scoring Points and Total Losing Points

After the scoring points of the tests are decided, total scoring points are obtained. It is given in table 4. In our application, for an LCD TV set, the total scoring point is 1800 points. The biggest part of the scoring points is the pass/fail tests and the smallest part of the scoring points is the early life period tests.

Table 2.4 Total scoring points

Test Type	**Scoring Points**
Pass / Fail Tests	1000
Early Life Period Tests	225
Design Verification Tests	575
Total Scoring Points (TSP)	**1800**

Then, the losing points of the failure severities are determined as shown in table 5. In our application, a showstopper failure has 120 losing points, a high failure has 45 losing points, a medium failure has 24 losing points and a low failure has 9 losing points.

Table 2.5 Losing points of failure severities

Failure Severity	**Losing Points**
Showstopper (S)	120
High (H)	45
Medium (M)	24
Low (L)	9

When the severity of the observed failures during testing is decided, total losing points of the project can be calculated from equation 2.2 as the following,

$$TLP = (A \times S) + (B \times H) + (C \times M) + (D \times L) \quad (2.2)$$

Where the symbols indicate the following,

TLP: Total Losing Points
A: Number of "Showstopper" Failures
S: Losing Point of Showstopper Failures
B: Number of "High" Failures
H: Losing Point of High Failures
C: Number of "Medium" Failures
M: Losing Point of Medium Failures
D: Number of "Low" Failures
L: Losing Point of Low Failures

By using equation 2.3 a new parameter, "Failure Risk Factor (FRF)", is calculated as the following,

$$FRF = TLP / TSP \quad (2.3)$$

$$ML = 1 - FRF \quad (2.4)$$

Where the symbols indicate the following,

ML: Maturity Level
FRF: Failure Risk Factor
TLP: Total Losing Points
TSP: Total Scoring Points

2.6 Case Study on Maturity Level Calculation

To calculate the maturity level of this project, 20 samples and 20 PW boards are taken and the following tests are performed. The numbers of test units and test duration are also given in the Table 2.6.

Table 2.6 Maturity level test set and test results

Test Name	**Number of Samples**	**Test Duration (Days)**	**Test Result**	**Test Points**
Temperature Stress Test	2	1	Bug No 11	100
Voltage Current Stress Test	3	3	No Failure	100
Open/Short Circuit Test	2	3	No Failure	75
ESD Test	2	1	Bug No 12	100
Momentary Power Out Test	2	18	Bug No 10	50
Surge Test	1	1	No Failure	25

Table 2.6 Continued

Test Name	Number of Samples	Test Duration (Days)	Test Result	Test Points
Voltage Dips, Short Interruption and Variation Test	1	1	No Failure	25
Inrush Test	1	1	No Failure	50
Lightning Surge Test	1	1	No Failure	50
Loose Plug Test	3	1	No Failure	50
Heat-Run Test	3	14	Bug No 2,3,4,7,9	100
High Temperature Test	1	1	Bug No 5	50
Low Temperature Test	2	1	Bug No 1,6,8	50
Temperature Cycle Test	3	5	No Failure	100
High Humidity Life Test	2	5	No Failure	25
Vibration Test	1	1	No Failure	25
Wall Holder Strength Test	1	14	No Failure	25
Drop Test	1	1	No Failure	25
Unpackaged Shock Test (Fragility Test)	1	1	No Failure	25
Random Vibration Step Stress to Failure	1	1	No Failure	50
Powered / Unpowered Temp Cycling	4	12	No Failure	75
Combined High Temperature &Humidity Test	2	4	No Failure	50
Thermal Shock Test	3	9	No Failure	50
Temperature Step Stress to Failure	2	3	No Failure	25
Operational High / Low Temp Humidity Test	3	6	No Failure	50
High Humidity (Environmental Storage Test)	4	2	No Failure	25
Constructional Inspection Test	1	1	No Failure	25
Thermal Cycling Test ELP	5	10	No Failure	50
Random Vibration Test ELP	1	1	No Failure	25
High Humidity Test ELP	2	5	No Failure	50
Thermal Shock Test ELP	10	9	No Failure	50
Power On/Off Test ELP	2	18	No Failure	25

As it can be seen from Table 2.6, most of the failures are found during the tests with high scoring points. The total test time is shortened by using different samples for different tests at the same time. The maturity level calculation data set is given in Table 2.7.

Table 2.7 Maturity level calculation – data set

Bug ID	Title	State	Severity	Points Lost
1	Low Temp NOK Backlight is not enough, picture comes late	Closed	1-showstopper	0
2	U24 Audio IC, because of auto assemble solder problems, there is no sound	Open	2-medium	24
3	Picture freeze in heat room	Closed	1-showstopper	0
4	"Info Banner" remark does not disappear in heat	Closed	1-showstopper	0
5	Stby problem in high temperature test	Closed	1-showstopper	0
6	IC806 was defected at Low Temperature Test	Open	1-showstopper	120
7	TV switches to stb mode at 40°C heat room	Closed	1-showstopper	0
8	TV freezes at Low temperature test and no signal	Closed	1-showstopper	0
9	TV switches to "no signal" mode after working for a while	Closed	1-showstopper	0
10	After St-by off-on, TV freezes and after resetting , it does not work again	Closed	1-showstopper	0
11	Components U32 U24 are NOK at Temperature Stress Test	Closed	1-showstopper	0
12	ESD Test is NOK	Closed	1-showstopper	0
		Total Point	**Loss Point**	**% Maturity**
		1600	144	91

Table 2.7 shows that there are 2 open failures which are not solved before mass production. One of them is decided to be a showstopper failure and the second one is considered as a high failure. If the failure is solved by the design group, the state of the failure is set as "Closed". Closed failures do not cause any lost points. By using equation 3, maturity level is calculated as 91%.

According to the test results shown in table 6 and 7, FRF is calculated as FRF=1-ML = 0.09. This means that, this LCD TV project has a 9% of failure risk probability due to non-life related, qualitative, stress factors in the field.

Next, in Chapter Three, reliability approval tests will be discussed and test specifications for each test will be given.

CHAPTER THREE
RELIABILITY APPROVAL TESTS

In this chapter, the reliability approval tests for a consumer electronics product are introduced. For each test, the aim of test, type, test condition, test duration, test equipment, test method and decision criteria are given.

3.1 Heat Run Test

Heat Run test is a kind of environmental test to determine withstands capacity of products at the maximum rated environment temperature and all adjustments are set to maximum rated (e.g. volume, backlight, etc.).

On the instruction brochures of the consumer electronics products, environmental maximum conditions stated that 0ºC to 40 ºC and the mains voltage can be varied between 176V AC to 264V AC (for Europe) for indoor appliances. Products are tested at maximum high temperature level that guaranteed under voltage variation specified.

Test area environment is set to 40±2ºC and 45%±10 relative humidity. Overall test duration is 3 weeks and EUT supply voltage is set to 176V AC (80% Vs), 220V AC (100% Vs) and 264V AC (120% Vs) each voltage level 1 week. Climatic Chamber, Pattern Generator and Variable AC Power Source are used during test. (Intel, 2003; Vetter, 1973; Neuburger, Aleksov, Schlesser, Kohn, & and Sitar, 2007; Defense, U.D.o., 2008; Defense, U.D.o., 1996; IEC, 2007)

After test Criteria I (or performance Criteria A) is applied, which states that during the test no function loss will be observed (even temporary). After the test, product should work properly with no function loss and copper wires should not get dark or burn and there should be no broken components on the PCB. There shouldn't be any burnt (turned to black) part on bottom part of the PCB. Also during the test no function loss will be observed. Scoring is 100 (out of 100) for this test.

3.2 High Temperature Test

High Temperature test is a kind of environmental test to see the functionality of the product at the maximum operating temperature. Observing and determining infant mortality events before starting the other corresponding tests to avoid uncertainties on each due to process and assembly errors and measuring overall case or cabin temperatures to be sure that product is under its specifications. 9 Samples put into Heat Room or appropriate Climatic Chamber, which is set to 40±2ºC 45%±10 relative humidity (or no humidity control for heat room). Different line voltages applied on each 3 products. After 24 Hours working one of the samples from each voltage group is taken and checks all functions and combinations by using Thermal (Infrared) Camera, Thermocouples with Data logger, Luminance Meter etc. and only check basic functions for remaining. (Intel, 2003; Vetter, 1973)

Total test duration is 24 Hours and EUT supply voltage is set to 176V AC (80% Vs), 220V AC (100% Vs) and 264V AC (120% Vs) for at least 3 samples at each voltage. Heat Room (or Climatic Chamber), pattern generator, variable AC power source, thermal (Infrared) camera, thermocouples with data logger and luminance meter are used during test. (Defense, U.D.o., 2008; Defense, U.D.o., 1996; JEDEC, 2009; JEDEC, 2010; IEC, 2007)

After test Criteria I (or performance Criteria A) is applied, which states that during the test no function loss will be observed (even temporary). After the test, product should work properly with no function loss and copper wires should not get dark or burn and there should be no broken components on the PCB. There shouldn’t be any burnt (turned to black) part on bottom part of the PCB. Also during the test no function loss will be observed. All measured values must be under specifications. Scoring is 50 (out of 100) for this test.

3.3 Low Temperature Test

Low temperature test is a kind of environmental test to determine the suitability of the Audio/Video equipment, under non heat dissipating and heat dissipating conditions, for use under conditions of low temperature.

Equipment under test (EUT) will be put into -15ºC Walk-IN chamber. After 4 Hours non-operating period EUT starts operating for 2 hours in low temperature. Total test duration for this test is 6 Hours and walk-in chamber and pattern generator are used.

After test Criteria II (or performance Criteria B) is applied, which states that no abnormality on operation, EUT must be visually inspected and electrically and mechanically checked. There must not be any permanent electrical and performance problem. Temporary functionality losses constitute no problem for the test criteria, furthermore, some geometrical shifts on the screen or some degradation because of specifications are allowed. Scoring is 50 (out of 100) for this test. (Intel, 2003; Defense, U.D.o., 2008; Neuburger, Aleksov, Schlesser, Kohn, & and Sitar, 2007; Defense, U.D.o., 1996; JEDEC, 2009; JEDEC, 2010; IEC, 2007)

3.4 Temperature Cycle Test

Temperature cycle test is a kind of environmental test to define withstand capacity of EUT under temperature change which can occur in real environment where EUT works with high stress levels. EUT will be put into test cycle that makes transitions between -20ºC and 60 ºC with 30 minutes dwell times and 5 minute transition time. Figure 3.1 shows the test condition. Cycling temperature between -20ºC and 60 ºC and no humidity control during 200 Cycles (~9 Days). (Defense, U.D.o., 1996; IEC, 2005; IEC, 2009)

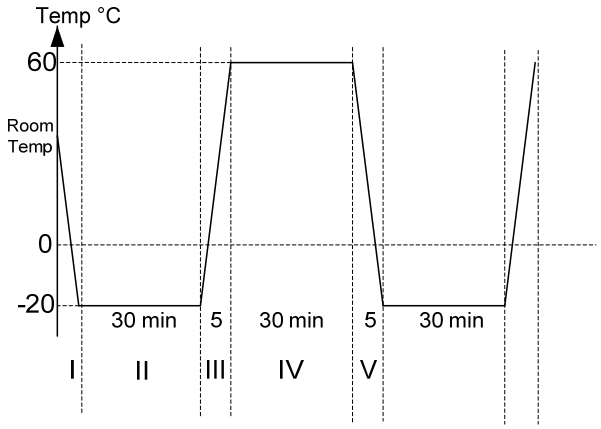

Figure 3.1 Temperature cycle pattern

After test Criteria I (or performance Criteria A) is applied, which states that during the test no function loss will be observed (even temporary). After the test, product should work properly with no function loss and copper wires should not get dark or burn and there should be no broken components on the PCB. There shouldn't be any burnt (turned to black) part on bottom part of the PCB. Also during the test no function loss will be observed. All measured values must be under specifications. Scoring is 50 (out of 100) for this test.

3.5 High Humidity Life Test

High Humidity test is done to determine withstands capacity of products at the high humidity, maximum rated environment temperature and all adjustments are set to maximum rated (e.g. volume, backlight, etc.) and it's a kind of environmental test. EUT will adjusted its maximum settings then put into 40ºC 95% relative humidity environment for 24 Hours. Climatic chamber and pattern generator are used during test. (Defense, U.D.o., 1996; NATO Standardization Agnecy, 2005)

After test Criteria I (or performance Criteria A) is applied, which states that during the test no function loss will be observed (even temporary). After the test, product should work properly with no function loss and copper wires should not get dark or burn and there should be no broken components on the PCB. There shouldn't be any burnt (turned to black) part on bottom part of the PCB. Also during the test

no function loss will be observed. All measured values must be under specifications. Scoring is 25 (out of 100) for this test.

3.6 Temperature Stress Test

Temperature Stress test is a kind of electrical test to determine whether each component working under its specified maximum temperature stated in its datasheet. Overheated components generally indicate overstress such as high power dissipation. These overheated components have shorter life and fails during early life time of EUT. They must be investigated and eliminated by replacing with higher specification components.

TV put into 40ºC environment after thermal equilibrium reached all temperature values are taken by either thermal camera or thermocouple in 40±2ºC RH : 45% ± 10 (or no humidity control for heat room) .

Total test duration for this test is 4 hours to 6 hours. Equipments of this test are; Heat Room (or Climatic Chamber), Pattern Generator, Variable AC Power Source, Thermal (Infrared) Camera, Thermocouples with Data logger, Luminance Meter.

All components' temperatures measured must be under its specification stated on its datasheet with 80% or 90% derating. Scoring is 100 (out of 100) for this test.

3.7 Voltage Current Stress Test

Voltage Current Stress test is a kind of electrical test to measure and compare the current and voltage values of the components used in device with the nominal values and to determine the components exceeding their nominal voltage and current values.

Electrical values such as voltage across, current passing, ripple current, frequency etc. are measured on each component used in 25±2ºC RH: 35% ± 10 (or no humidity control for laboratory condition).

All electrical values measured by electrical measurement devices. Total duration of this test is 1 week and oscilloscope with voltage probes, multimeter and current probe are used. The measured current or voltage value of components shouldn't exceed rated values. Scoring is 100 (out of 100) for this test.

3.8 Open/Short Circuit Test

Open/Short Circuit is a kind of electrical test. The aim is in Open/Short Circuit test while a fault condition occurs such as a short circuit in electrolytic capacitors etc. because of aging, manufacturer must be sure that product causes no fire (for safety) and also still repairable after fault (for reliability).

The components which have to be short circuit risk in future in EUT life are short circuited and which has to be open circuited risk in future in EUT life are opened. Then, all component temperatures are measured and observed against smoke and fire.(IEC, 2001)

Short circuit test is applied to all capacitors (>20V), semiconductors (transistors, diodes), between the windings of transformers' (FBT and SMT) and IC's. Open circuit test is applied to all above including coils and resistors (>1/2Watt); besides transformers' windings never will be opened. During the fault condition test, power consumption and ΔT measurements are performed. Total duration of this test is 1 week and Pattern Generator, Variable AC Power Source, Thermal (Infrared) Camera; Thermocouples with Data logger are used. The EUT works with some criteria and will be failed if;

- Two or more components are burnt,
- One component is burned and spreads the fire to the adjacent components,
- SMT and power supply rectifier are burnt or smoking,
- PCB burns so that it cannot repair,
- ΔT should not be exceeded the IEC/EN60065 Safety standard.

Scoring is 100 (out of 100) for this test.

3.9 ESD Test

ESD test is a kind of electrical test to prevent possible failures of EUT's that can be caused by electrostatic discharge. Human body due to friction charges up to 20kV electrostatic charge. Discharge of this amount on consumer electronic products causes ESD hazards on unit. All reachable parts of product must be immune to ESD in 25±2ºC and RH: 35% ± 10 (or no humidity control for laboratory condition). ESD test has specific test criteria such as; ± 4kV Conducted Discharge, ± 10kV Conducted Discharge, ± 8kV Air Discharge, ± 15kV Air Discharge, ± 5kV Air Discharge to Live Part, ±8 kV Conducted (Touch-Pad Panel), ±15 kV Air (Touch-Pad Panel). Positives and Negatives are applied 20 times for (Accessible metal parts, AV IN, AV OUT, SCART and Tuner Gnd. etc). Total duration of this test is almost 1 Hour and ESD Test Gun, ESD Test Setup are used. (Intel, 2003; IEC, 2008)

After Criteria I, TV have to be checked and it should work after the test without any functional loss. During test temporary function losses are acceptable but they must be self recoverable. Scoring of this test is 100 (out of 100).

3.10 Manual Spark Test

Manual Spark test is a kind of electrical test to define the withstand capability of IC which is located on CRT PCB to anode sparks for several times.

Manual Spark device applies spark on R, G, B, Screen and Focus pins respectively 100 times in 25±2ºC and RH: 35% ± 10 (or no humidity control for laboratory condition). Criteria III (or C) – TV should work after the test without any function loss, no broken or malfunctioned component. Total test duration is 1 hour and Manual Spark Test Device is used.

3.11 Laser Spark Test

Laser Spark test is a kind of electrical test to define the withstand capability of IC which is located on CRT PCB to anode sparks for several times in 25±2ºC and RH: 35% ± 10 (or no humidity control for laboratory condition).

Laser applied on CRT anodes by laser beam in a special room. Total duration is 1 hour and NEC Laser Machine Model: SL480B, Laser Guide Mechanism for 3 Axes are used in Laser Spark test.

After these criteria's, TV should work after the test without any function loss, no broken or malfunctioned component.

3.12 Power Switch On/Off Test

Power Switch is a kind of electrical test to define the mechanical and electrical withstand capability of power switch and product against to switching ON/OFF for several times and measuring.

Especially consumer electronics products on the market face ON and OFF procedures everyday very often. This ON and OFF sequence causes different stresses

on product. This test procedure aims to simulate them in 25±2ºC RH: 35% ± 10 (or no humidity control for laboratory condition).

In Power On/Off switch test; products main on/off switch and they are applied 100.000 times (50.000 ON, 50.000 OFF). Total duration of this test is 18 days and Pneumatic Fingers are used.

After these criteria's, TV should work after the test without any function loss, no broken or malfunctioned component. Scoring of this test is 50 (out of 100).

3.13 Momentary Power out Test

Momentary Power Out test is a kind of electrical test to define the withstand capability of the power circuit against to momentary power out.

Especially consumer electronics products on the market face ON and OFF procedures everyday very often. This ON and OFF sequence causes different stresses on product. This test procedure aims to simulate them in 25±2ºC and RH: 35% ± 10 (or no humidity control for laboratory condition) In Momentary Power Out test; products that have soft switch and they are applied 100.000 times (50.000 ON, 50.000 OFF). Total duration of this test is 18 days and Electronic mains timer is used.

After these criteria's, TV should work after the test without any function loss, no broken or malfunctioned component. Scoring of this test is 50 (out of 100).

3.14 Surge Test

Surge test is a kind of electrical test to take necessary precautions for TVs against surges which are caused by over voltages from switching and lightning transients. Surge test checks device immunity against surge voltages tested. Up to 1kV is applied on (Intel, 2003; IEC, 2005)

Table 3.1 Surge levels for combined surge test

U_{start}	0.5kV	**Ustop**	2kV	∇	0.2kV
$Phase_{start}$	0°	**$Phase_{stop}$**	180°	∇	90°
Positive	5 Pulse	**Negative**	5 Pulse		

Total duration of this test is 1 Hour and Surge Simulator is used.For ±1 Kv device should not set at standby mode and should not be damaged component. For ±2 Kv and above device could be set at standby mode but should not be damaged component. Especially SMPS circuits and associated components should not be failed. Scoring of this test is 25 (out of 100).

3.15 Voltage Dips, Short Interruption and Variation Test

Voltage Dips, Short Interruption and Variation Test is a kind of electrical test to prevent possible failures of device that can be caused by voltage dips, short interruptions and voltage variations. Mains voltage is not well regulated and has not got perfect sine form; this test simulates such dips, interruptions and variations over mains(IEC, 2004)

Table 3.2 Parameters of voltage dips variation test

Unominal:	1 kV
Polarity:	+ / -
Phase:	L + N
Spike Freq:	5 kHz
Burst Duration:	15 ms
Burst Freq:	3 Hz
Test Time:	60 sec
Syncro Freq:	50 Hz
Syncro Angle:	180^0
Phase:	L + N
Spike Freq:	5 kHz

Total test duration is 1 Hour and Surge Simulator is used. The test results shall be classified as respectively: At first; normal performance within the specification limit. Secondly, temporary degradation or loss of function or performance which is self recoverable. Finally; temporary degradation or loss of function or performance which requires operator intervention or system reset. Degradation or loss of function or performance which is not recoverable due to damage of equipment or software or loss of data. Scoring of this test is 50 (out of 100).

3.16 Inrush Test

Inrush test is a kind of electrical test to determine the current on the main power line when the power is on and decide whether that current is suitable for the switch, fuse and the other primer components if available.

When TV is turned on, bulk capacitor consumes very high current in 25±2ºC and RH: 35% ± 10 (or no humidity control for laboratory condition). Inrush current on mains line is measured by either current probe or series current sensing resistor. Total test duration is 1 hour and Current Probe or Current Sense Resistor is used during test. Oscilloscope can be used. Scoring of this test is 75 (out of 100).

3.17 Lightning Surge Test

Lightning Surge test is a kind of electrical test to define the withstand capability of the TV against to high voltage and current resulting from lightning surge. Lightning's dropped over mains line or antenna can damage equipment, this test simulates such conditions in 25±2ºC and RH 35% ± 10 (or no humidity control for laboratory condition). (IEC, 2005)

In the Lightning Surge test; 1, 2, 3, 4, 5, 10, 12kV are applied to TV's power input for two stages. Stage 1 is AC line out and Stage 2 is Surge out. Total test duration is 1 hour and Lightning Surge Simulator.

While actualizing Lightning Surge test, we have to check TV in different voltages; for 1, 2, 3 kV there should be no problem. Additionally; for 4, 5 kV fuse can blow and also for 10, 12 kV there should not be a fire condition. Scoring of this test is 75 (out of 100).

3.18 AC Mains over Voltage Test

AC Mains over Voltage test is a kind of electrical test to observe whether a fire situation occurs at TV or not.

City mains voltage generally has not perfect sine form and not perfectly regulated. In some locations of the earth continuous over voltage is common issue. Test is started at 320V for 1 hour. Then, the test voltage is set to 370V. Finally, test voltage is increased by 10V steps in every 30 minutes. Test condition is given in Figure 3.2.

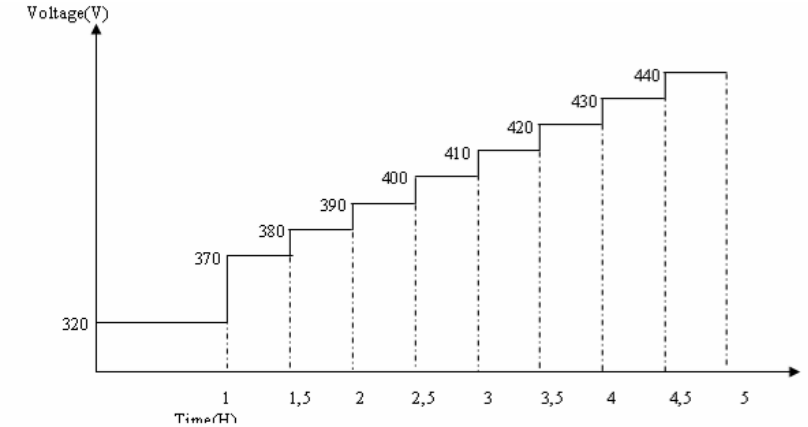

Figure 3.2 AC Mains over voltage test condition

Total test duration is 5 hours. Variable AC Voltage Source and Pattern Generator are used. An important criterion is that component defects and function failures acceptable but any fire situation should not be observed.

3.19 Loose Plug Test

Loose Plug Test is a kind of electrical test to define the performance and withstand capability of the power boards against loose plug switching.

Plugging equipment to mains socket causes arcs/spikes that have very high voltages. This test procedure is testing immunity of such conditions in 25±2ºC and RH: 35% ± 10 (or no humidity control for laboratory condition). Operator try to mount socket to plug improperly to create sparks randomly. Total test duration is 1 hour and Loose Plug Test setup is used. TV should work properly after test without any function loss. Scoring of this test is 50 (out of 100).

3.20 Vibration Test

Vibration test is a kind of mechanical test to determine the possible failures on TV while TV is transported by different types of vehicles and measuring the strength of components while external vibration applied at their resonant frequencies. Product with box will be affected by outside vibrations while transporting, this test mainly simulates such conditions. (Defense, U.D.o., 2008; IEC, 2007)

Test:

1- Packaged
2- Unpackaged

For Z Axis;

- Signal : Sine
- Frequency (≤26") : 5 – 55 Hz.
- Frequency (≥26") : 5 – 100 Hz.
- Sweep Time : 10 min.
- Total Time : 60 min
- Acceleration : 1G

For X – Y Axis;

- Signal : Sine
- Frequency (≤26") : 5 – 55 Hz.
- Frequency (≥26") : 5 – 100 Hz.
- Sweep Time : 10 min.
- Total Time : 30 min
  Each axis
- Acceleration : 1G

Test will be applied on packaged products first and results will be reported than unpackaged TV fixed on shaker test will applied and results will be reported with a

separate report. Product tested must be fastened on head expander. (McConnell, 1995)

Total test duration is 1 hour and Electrodynamics Vibration Machine is used. In Vibration tests; TV should work properly and there mustn't be any crack at the TV cabin, at the solder points of chassis, at the pins of components. In addition, there mustn't be any major problem at the TV packaging and snow boxes. Scoring of this test is 25.

3.21 Wall Holder Strength Test

Wall Holder Strength test is a kind of mechanical test to define the withstand capability of the TFT/LCD and Plasma TVs against to weight stress when they are mounted on the wall such that a force in addition to the weight of the TFT/LCD or Plasma TVs is applied downwards through the center of gravity under environmental conditions specified in -15±2 °C, RH=%45±10 (1 Week) and 40±2 °C, RH=%45±10 (1 Week).

%20 Additional mass symmetrically connected downwards on TV while it mounted. Total test duration is 2 weeks and Specials weights are used.

TV should stay without fall down on wall and there must not be any crack or broken on back cover under conditions stating that a force in addition to the weight of the TFT/LCD or Plasma TVs is applied downwards through the center of gravity under environmental conditions for 2 weeks totally. Scoring of this test is 25 (out of 100).

3.22 Drop Test

Drop test is a kind of mechanical test to see the effects of a possible drop on device or package while delivery and obtain the consignment of the device to the customer without any damage.

Packaged product is dropped at various heights on each corner and surface by free fall drop test machine. Total test duration is 1 hour and Free Fall drop test machine is used.

TV should work properly and there mustn't be any crack at the TV cabin, at the solder points of chassis, at the pins of components. In addition, there mustn't be any major problem at the TV packaging and snow boxes. Scoring of this test is 50 (out of 100).

3.23 Unpackaged Shock (Fragility) Test

Unpackaged Shock (Fragility) test is a kind of mechanical test to determine the effects of mechanical shock pulse applied to TV in 25±2ºC and RH: 35% ± 10 (or no humidity control for laboratory condition). (Defense, U.D.o., 2008)

Test:40G Test 10msec shock pulse up to 23"
30G for 6msec for 23-32"
> 32" 30G, 4.5msec
Z and X axis only, no for panel plane
25 Pulses
No box, only product, fastened to head expander

Total test duration is 1 hour and Free Fall Mechanical Shock or Electrodynamics Vibration Machine can be used.TV should work properly and there mustn't be any crack at the TV cabin, at the solder points of chassis, at the pins of components. Scoring of this test is 100 (out of 100).

3.24 Random Vibration Strength Test

Random Vibration Strength test is a kind of mechanical test to determine the possible failures on TV while TV is transported by different types of vehicles and measuring the strength of components while external vibration applied at their

random frequencies. Random Vibration Strength test should be checked with the given table 3.3 for Packaged and Unpackaged;

Table 3.3 Random vibration test levels

Freq. (Hz.)	**PSD (g2/Hz.)**
12	0.017
42	0.017
54	0.058
72	0.058
200	0.006
Grms	2.400

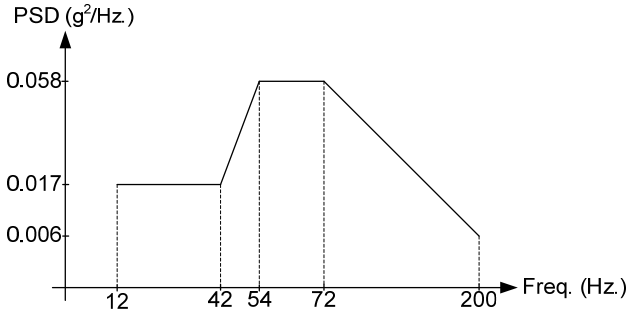

Figure 3.3 Random vibration test condition

The pattern shown, in Figure 3.3, will be applied 20 minutes for both packaged and unpackaged products but reports will be separate. Product tested must be fastened on head expander. Total test duration is 1 hour and Electrodynamics Vibration Machine is used. (Defense, U.D.o., 2008; Intel, 2003)

TV should work properly and there mustn't be any crack at the TV cabin, at the solder points of chassis, at the pins of components. Scoring of this test is 100 (out of 100).

CHAPTER FOUR
DESIGN VERIFICATION TESTS

In this chapter, the design verification tests are introduced. The main purpose of product level testing or design verification testing is to simulate possible and most likely failures by doing long period tests. Test results are not PASS/FAIL tests, but rather any failure found is feedback to design team to be solved. Product level procedure is very similar to Highly Accelerated Stress Screening (HASS) idea. Generally, overall quality is monitored.

DVTs are product level tests and DVTs are performed with 75 samples. In general, 30 days are required to perform all the tests. Table 2.3 shows the tests applied in this stage. Same scoring process is also performed for DVT. High number of samples gives more accurate results during tests.

The probability of seeing more likely failures is increased due to realistic stress levels and high number of samples. Each sample is put into heat run test after the end of other tests. In heat-run test, product simply works at 40°C ambient temperature with full rating of its settings. Life test has no strict time limit; the failures occurred are recorded to calculate Mean Time to Failure (MTTF). In addition to this, problems found are recorded for scoring.

4.1 Powered / Unpowered Temperature Cycling

Powered/Unpowered Temperature cycling test is a kind of environmental test to determine the strength of equipment against extreme temperature change.

This test is done as a highly accelerated test method that Power ON/OFF combined on. The product is going exactly the minimum temperature level because the product power is OFF at low stage. The test has 4 different types of stress factors; low temperature, high temperature, temperature cycling and power on/off cycles which are shown Figure 4.1.

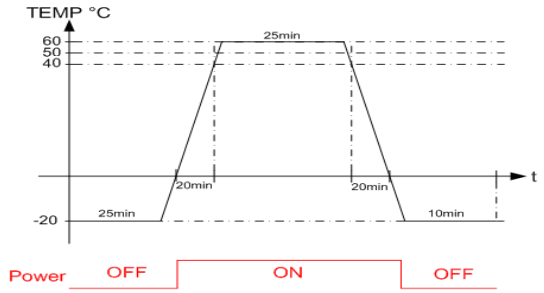

Figure 4.1 Powered unpowered temperature cycling test condition

Total test duration is 75 hours (50 Cycles) and the total number of samples is equal to 5 samples. ESS Climatic Chamber or HALT/HASS Chamber can be used in Powered/Unpowered Temperature Cycling test.

TV should work properly and there mustn't be any crack at the TV cabin, at the solder points of chassis, at the pins of components. Scoring of this test is 50 (out of 100).

4.2 Combined High Temperature & Humidity Test

Combined High Temperature & Humidity test is a kind of environmental test to calculate MTTF of product.

Combined High Temp & Humidity test is a very stressful test which has an acceleration factor of 104. This means that, 1 hour in the test of 80°C - 90%RH environment is equivalent for 104 hours in the field. Samples should put in to 80°C - 90%RH chamber and failure times are recorded. This test will go on until samples defected. Climatic Chamber or Walk-In Chamber can be used and the scoring of this test is 50 (out of 100). (Defense, U.D.o.) (Intel, 2003)

4.3 Thermal Shock Test

Thermal Shock test is a kind of environmental test to determine the thermal resistance against the sudden temperature changes of the Power Boards and Main Boards, in -30 o C during 30 min / +80 o C during 30 min.

Figure 4.2 shows the test condition of thermal shock test. Dwell time is very short in thermal shock test so a rapid chamber is needed to perform this test.

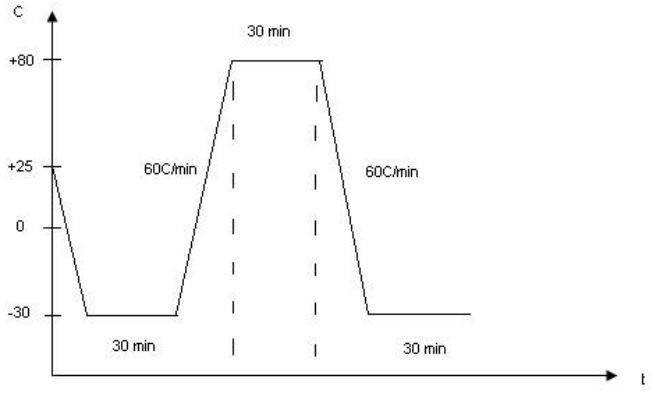

Figure 4.2 Thermal shock test condition

In the Thermal Shock test, temperature should be set at -30ºC during 30 min / +80ºC during 30 min and Ramp Rate should be set at 60ºC/min. Total test duration is 50 hours and Thermal Shock Chamber or ESS Climatic Chamber are used.

TV should work properly and there mustn't be any crack at the TV cabin, at the solder points of chassis, at the pins of components. Scoring of this test is 75 (out of 100).

4.4 Temperature Step Stress to Failure Test

Temperature Step Stress to Failure test is a kind of environmental test to determine the Temperature Strength of the Components used in new design products. Finding weakest points of the design by applying increasing temperature until a defect observed.

Table 4.1 Temperature stress test levels and durations

TEMPERATURE	DURATION
50±2 °C	4 Hours
55±2 °C	4 Hours
60±2 °C	4 Hours
65±2 °C	4 Hours
70±2 °C	4 Hours
75±2 °C	4 Hours
80±2 °C	4 Hours
90±2 °C	4 Hours
100±2 °C	4 Hours
Until product malfunctioned	

Total test duration is 4 hour each step and Climatic Chamber is used. Failure modes and failure components are inspected in details. Results are recorded on bug list. Design team tries to improve strength of failed components. Scoring of this test is 50 (out of 100).

4.5 Operational High / Low Temperature Humidity Test

Operational High/Low Temperature Humidity test is a kind of environmental test to define the withstand capability of the products while they are running against the variable temperature and humidity. Test condition is given in Figure 4.3.

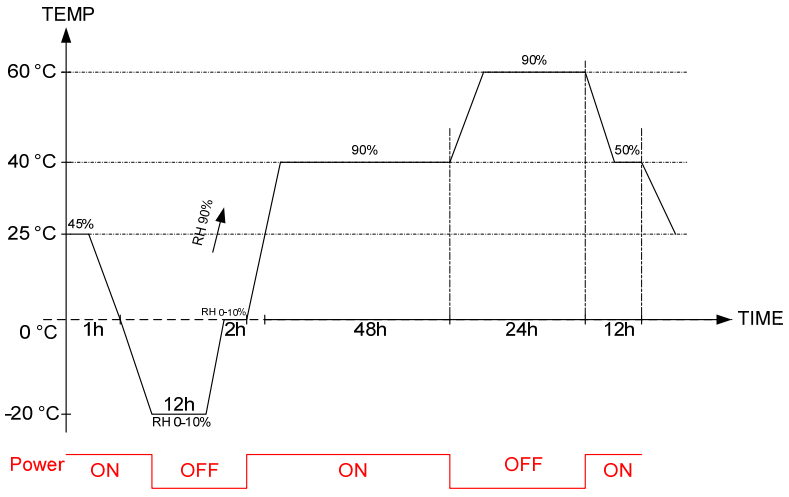

Figure 4.3 Operational high/low temperature humidity test condition

Total test duration is 99 Hours. 3 equipments are used in Operational High/Low Temperature Humidity test and they are; CH2000 Climatic Chamber, Power ON / OFF Setup, AC Power Source.

TV should work properly and there mustn't be any crack at the TV cabin, at the solder points of chassis, at the pins of components. Scoring is 50 (out of 100) for this test.

4.6 High Humidity (Environmental Storage) Test

High Humidity (Environmental Storage) test is a kind of environmental test to see the effects of humidity and temperature while transportation.

High Humidity works in 50°C and -15°C. Storage in box at 50°C, 90% RH 48 hrs. Then 24 hours operating in 40°C %80 RH. Also; storage in box -15°C, 45% 48 hrs. Then 24 hours operating in Room Temp %50 RH. Total test duration is 2 Days and Climatic Chamber is used.

TV should work properly and there mustn't be any crack at the TV cabin, at the solder points of chassis, at the pins of components. In addition, there mustn't be any major problem at the TV packaging and snow boxes. Scoring is 25 (out of 100) for this test.

4.7 Design Structure Inspection Test

Design Structure Inspection test is a kind of inspection test to find out the physical construction faults which can constitute a trouble in the future on PCB. This test will be applied all new coming TV's and Boards.

Running

TV must work properly with full functions for 20 min. Boards must work properly with full loading for 20 min.

Mains

20 min. @ 176V. AC. (80% Vs)

20 min. @ 264V. AC. (120% Vs)

TV must work properly. And power consumptions and current drawn must be in the limits.

Loose Plug Test

Loose Plug test applied for 30 minutes.

Constructional Inspection

TV back covers are removed and the location of boards and cables are checked. Boards are checked for component locations and solder reliability.

SAP BOM Check

Boards must be checked with BOM on the SAP, boards must be assembled according to latest BOM.

Scoring is 50 (out of 100) for this test.

CHAPTER FIVE
BOARD LEVEL TESTS

In this chapter, the board level tests are introduced. The main purpose of board level testing is to find and observe quality problems, assembly problems and failures occurred in early life, e.g., infant mortality failures. The judgment criterion of this test package is not strict PASS /FAIL. Problems found is fed back to design team to discuss. The idea of these tests is very similar to Highly Accelerated Life Test – HALT. The following example explains procedure, judgment and corrective action for 42" Full HD High End TV PSU Card board level random vibration test.

Table 5.1 Random vibration test result of PSU of a 42" LCD TV set

		42" PSU Board
Test		Random Vibration Board Level
Acceleration / Freq.		4 g_{rms} / 10Hz. – 500Hz.
Total Test Duration		30 min.
Failures Found		
1	During test some electrolytic capacitors leaves PCB	
2	Heat Sink brakes small part of PCB	
Judgement		
1	Holes and Pads are not suitable for capacitor pins. They must be smaller. It is a representative problem. It can cause dry solder problems. It must be corrected.	
2	Because of high stress levels and heat sink is too heavy, failure is not representative.	

Table 5.1 shows a 42" PSU Board sample from random vibration test. Due to high stress levels during test, some fails are non-representative errors so they must not be considered. It is generally too hard to define a failure as representative or non-representative for the people dealing with reliability, therefore, the design team must define failures correctly at that stage. Representative failures found are generally critical and must be sold, but some failures, even they are representative, may not be solved.

Table 2.2, in Chapter 2, shows the board level test list. Each test is performed with 15 samples. The level of stress of these tests is very high; therefore each of the board level tests can be a part of Highly Accelerated Life Test (HALT) procedure.

5.1 Thermal Cycling ELP

Thermal Cycling ELP test is a kind of environmental test to determine the Thermal resistance of the Power Boards and Main Boards with respect to the defined testing conditions in -20ºC / +80ºC - 10°C/min. Test condition is given in Figure 5.1.

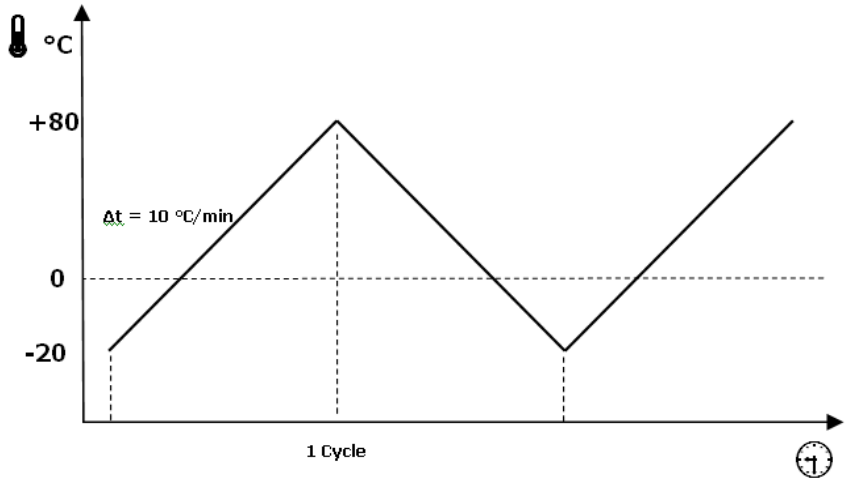

Figure 5.1 Thermal cycling test condition

Thermal Cycling ELP has 24 cycles. Total test duration is 8 hours and Thermal Shock Chamber or ESS Climatic Chamber can be used. All boards must work properly after the test, any damage on components or solder is not accepted. Scoring is 75 (out of 100) for this test.

Related International Standards

MIL-STD-883G Method 503.5 Temperature Shock

IEC 60068-2-30 Damp Heat Cycling

IEC 60068-2-14 Change of Temperature

NATO STANAG 4370, Environmental Testing

5.2 Random Vibration Test ELP

Random Vibration test is a kind of mechanical test to determine the possible failures on boards in early life by measuring the strength of components while

external vibration applied at their random frequencies in 25±2ºC and RH: 35% ± 10 (or no humidity control for laboratory condition).

Figure 5.2 shows the test condition for random vibration test.

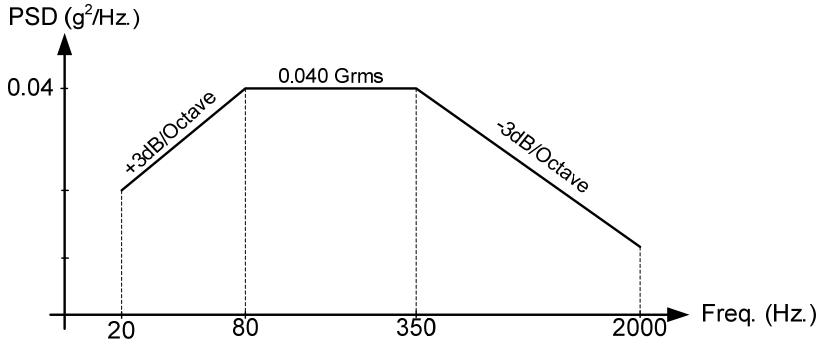

Figure 5.2 Random vibration test condition

This test should apply products according to followings; Min 5 Grms for Main board, each axis 20 minutes, 10 Boards (DVT), 20 Boards (PVT) and Min 1.5 Grms for Power board, each axis 20 minutes, 10 Boards (DVT), 20 Boards (PVT).Total test duration is 2 hours and Vibration Machine is used.

All boards must work properly after the test, any damage on components or solder is not accepted. Scoring is 50 (out of 100) for this test.

Other Company Spec.

IntelBluebookUpto $1G_{rms}$

AUOUpto 1.8 G_{rms}

Related International Standards

MIL-STD-810GMethod 514.6 Vibration

5.3 High Humidity Test ELP

High Humidity test is a kind of environmental test to define the withstand capability of the Boards against to high humidity.

Total test duration is 24 Hours and Climatic Chamber is used. All boards must work properly after the test, any damage on components or solder is not accepted. Scoring is 50 (out of 100) for this test.

Related Publications

NATO STANAG 4370, Environmental Testing; 19 April 2005

Related International Standards

MIL-STD-883G Method 507.5 Humidity

IEC 60068-2-38Composite temperature/humidity cyclic test

5.4 Thermal Shock Test ELP

Thermal Shock Test ELP is a kind of environmental test to determine the thermal resistance of the Power Boards and Main Boards in +120°C / -40°C.

Board level thermal shock test is given by Figure 5.3.

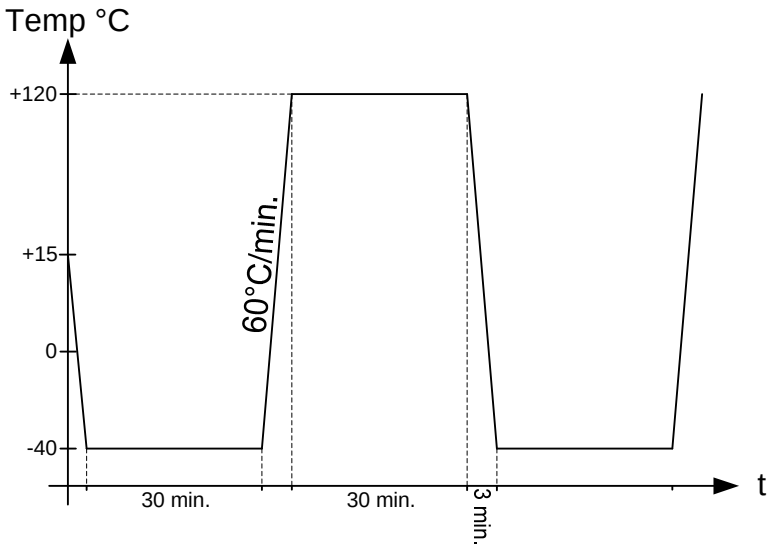

Figure 5.3 Thermal shock test condition

Thermal Shock Test ELP has 100 cycles and total duration is 100 hours. Thermal Shock Chamber or ESS Climatic Chamber can be used. All boards must work

properly after the test, any damage on components or solder is not accepted. Scoring is 50 (out of 100) for this test.

Related International Standards

MIL-STD-883G Method 503.5 Temperature Shock

IEC 60068-2-30Damp Heat Cycling

IEC 60068-2-14Change of Temperature

NATO STANAG 4370, Environmental Testing

5.5 Power On/Off Test ELP

The purpose of this electrical test is to define the performance and withstand capability of the power boards against ON/OFF switching. Test is performed on normal room temperature at 25±2ºC and 35% ±10 (or no humidity control for laboratory condition).

Table 5.2 Voltage levels of power On/Off ELP test

U	**Voltage**
Unom	220V
Umin	176V
Umax	264V
Umin & Umax depends on design specifications of Power Board	

Test Steps and Durations

1st Step

Uin: min

2000 cycles with dummy load

DP: 5 second ON, 5 second OFF

Test duration: About 5.5 hours

2nd Step

Uin: min

1000 cycles with dummy load

DP: 15 seconds ON, 15 seconds OFF

Test duration: About 8 hours

3rd Step

Uin: max

2000 cycles with dummy load

DP: 5 second ON, 5 second OFF

Test time: About 5.5 days

4th Step

Uin: max

1000 cycles with dummy load

DP: 15 seconds ON, 15 seconds OFF

Test time: About 8 days

PLC controlled pneumatic ON/OFF test setup, variable power source and dummy loads with different resistances are used during test. All boards must work properly after the test, any damage on components or solder is not accepted after the test. Scoring is 75 (out of 100) for this test. In the next chapter, the studies regarding software reliability will be introduced.

CHAPTER SIX
SOFTWARE RELIABILITY STUDIES

In this chapter, the studies in software reliability are introduced with two case studies. In the first case study, optimal test case design for consumer electronics products is defined. In the second case study, a special program called MATELO is used to generate optimal test cases and calculate the software reliability.

6.1 Optimal Test Case Design – Case Study 1

In this section, the optimal test case design is introduced. First, the importance of optimal test case design is given in Section 6.1.1. Then, usage profile is described in Section 6.1.2. In Section 6.1.3 modeling user behavior is introduced.

6.1.1 Introduction to Software Reliability

Testing is generally time consuming and induces significant cost. If it is automated, the testing effort is considerably reduced. Automated testing was traditionally mainly associated to automated test case execution, with test case generation still consuming significant amount of testing time. Even based on automated test case generation, testing can be inefficient, due to the fact that its quality is highly dependent on the structure and content of the test cases. If the test cases reveal defects within the functionality that will be intensively used by end-user, testing efficiency increases. Generally, for optimal testing, test cases should be designed to reduce overall testing time and to detect the failures that affect the user most.

6.1.2 Optimal Test Case Design - Creating Usage Profile

Creating usage profile is the first step of optimal testing and determining the software reliability of a consumer electronics product, as everyone can use the equipment with different commands. As an example, one can turn on a TFT LCD TV

set by pressing Program Up button and the other one can turn on by pressing Program Down or Stby On button. Furthermore, an adult or a child can send different commands to the software to perform the same action. So, an optimum usage profile should be determined and according to this optimum usage profile the probability of a transition from one state to another should be calculated. To get this data, the following instructions can be done.

- LCD TV sets were given to personnel,
- A questionnaire expressing how the samples were used was filled for each sample,
- The collected user behavior data and device operational data completely describe the expected device usage,
- User behavior can change according to the age, sexuality etc. as shown in Table 6.1.
- By using this data, usage profile with probabilities of changing states for each sample were determined,
- By using these usage profiles obtained from each unit, a general optimum usage profile with state changing probabilities was determined.

Table 6.1 Usage data for turn on operation for child and adult user groups

Function	**User group**	**Operation (Input)**	**Input probability**	**Expected output**
Turn on	Child	POWER ON button	0.8	Turned on
		Button 0	0	
		Button 1	0	
		Button 2	0	
		Button 3	0	
		Button 4	0	
		Button 5	0	
		Button 6	0	

Table 6.1 Continued

Function	User group	Operation (Input)	Input probability	Expected output
		Button 7	0	
		Button 8	0	
		Button 9	0	
		VOL+ Button	0.1	
		VOL- Button	0	
		CH+ Button	0.1	
		CH- Button	0	
	Adult	POWER ON button	0.6	Turned on
		Button 0	0.01	
		Button 1	0.1	
		Button 2	0.01	
		Button 3	0.01	
		Button 4	0.01	
		Button 5	0.01	
		Button 6	0.01	
		Button 7	0.01	
		Button 8	0.01	
		Button 9	0.01	
		VOL+ Button	0.07	
		VOL- Button	0.03	
		CH+ Button	0.08	
		CH- Button	0.03	

6.1.3 Optimal Test Case Design – Experimental Results

After user profile was created, in order to measure the correlation between the number of detected failures using the optimal test case generation and subjectively perceived failures, we have first generated the test set consisting of 1000 test cases

using the optimal test case generation. The test set was carried out automatically, and the revealed failures were recorded. Next, the experiments are used to estimate the relation (in terms of type and quantity) of detected failures with user perceived failures. The experiment included 6 subjects, which were asked to use the TV set and to report any failure they detect in usage. The failures most detected were reported for OSD layer non-functionality (30 failures in subjective evaluation, in comparison to 32 detected by the optimal test set, for menu list scrolling function, and 28 failures in subjective evaluation, in comparison to 25 failures detected by the optimal test set, for OSD element misalignment), next for artifacts occupying large portions of picture (25 failures in subjective evaluation, in comparison to 22 failures found using the optimal test set), then for input signal manipulation non-functionality (19 failures in subjective evaluation, in comparison to 21 failures detected using the optimal test set), and finally for artifacts occupying small portions of picture (17 failures were detected in both cases).

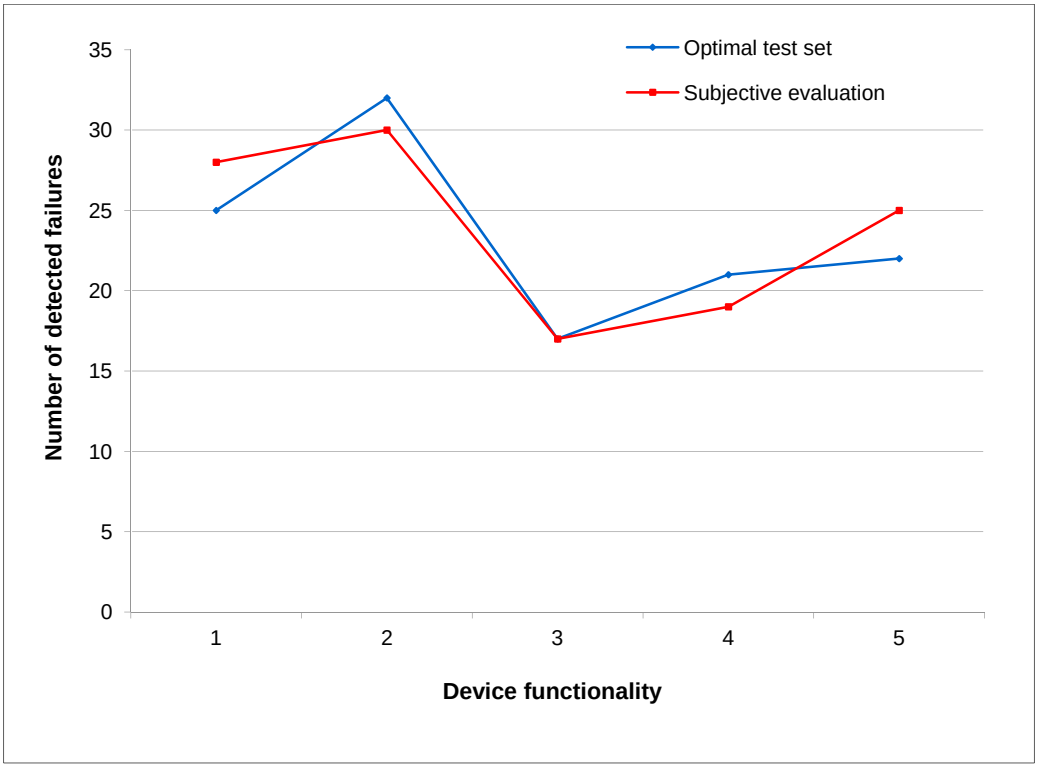

Figure 6.1 Correlation of failures detected by the optimal test set generated using the optimal test case design and subjectively perceived failures, for the particular TV set functionality: 1,2-OSD layer non-functionality, 3-artifacts occupying small portions of picture, 4-input signal manipulation non-functionality, 5-artifacts occupying large portions of picture

It is observed based on the experimental results that the proposed scheme for optimal test case design is well correlated with user perception of failures. The number of detected failures using the optimal test case design (blue line in Figure 6.1) is close to the number of subjectively perceived failures (red line in Figure 6.1).

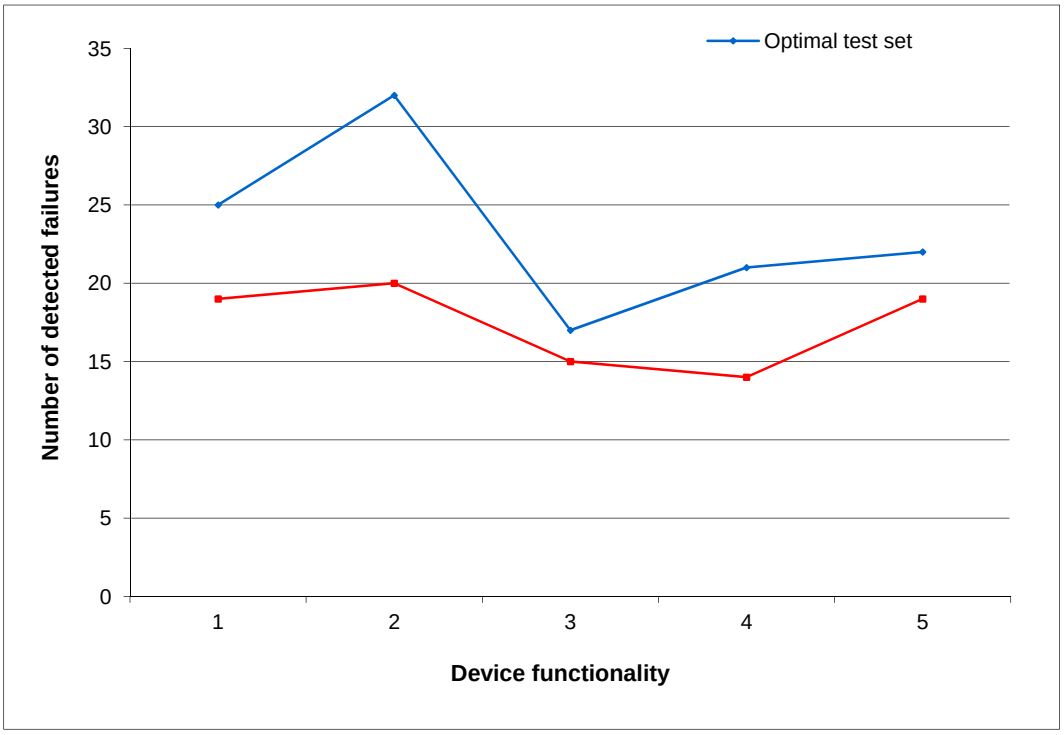

Figure 6.2 Correlation of failures detected by the optimal test set generated using the optimal test case design and the test set generated manually, for the particular TV set functionality: 1,2-OSD layer non-functionality, 3-artifacts occupying small portions of picture, 4-input signal manipulation non-functionality, 5-artifacts occupying large portions of picture.

As can be noticed from Figure 6.2, the number of failures detected by using the optimal test set based on the optimal test case design considerably differs from the number of failures detected by the test set generated manually. For menu list scrolling function, 25 failures are detected by the optimal test set, in comparison to 19 failures detected by the manually generated test set. In addition, for OSD element misalignment, 32 failures are detected by using the optimal test set, in comparison to 20 failures found by using the manually generated test set.

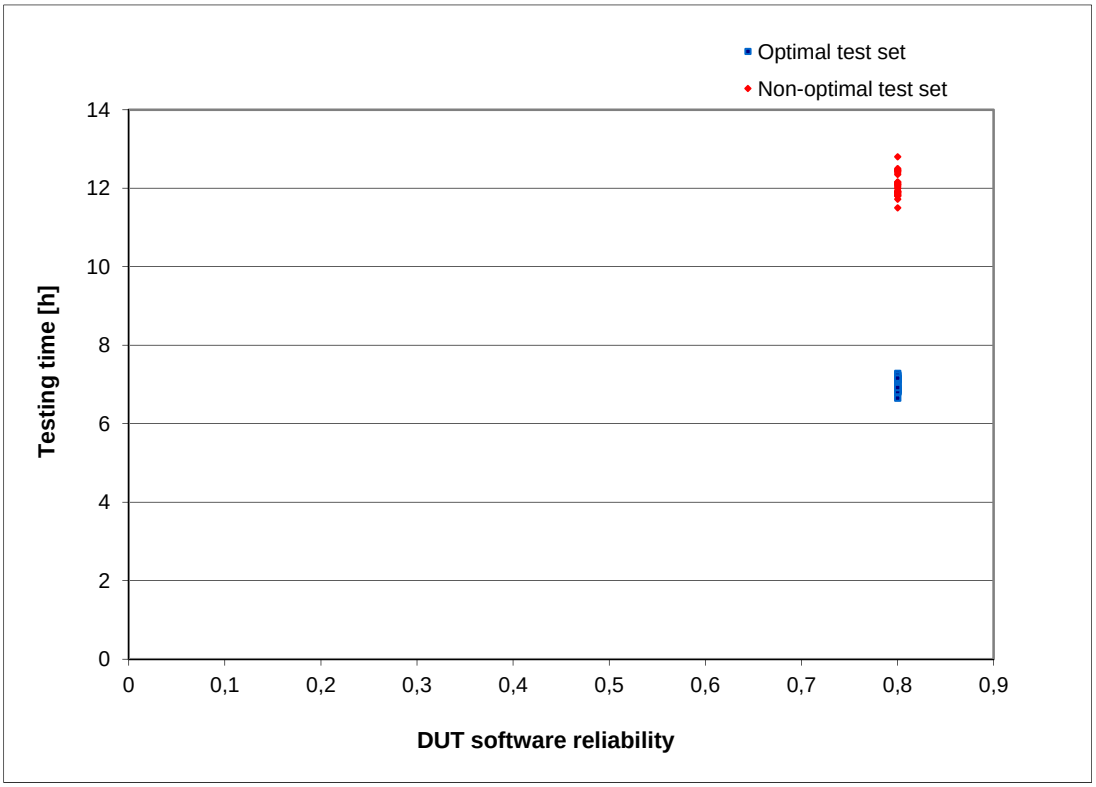

Figure 6.3 Comparison of the testing time for the optimal test set based on the proposed method and non-optimal test set, regarding the required quality level.

For the optimal test set, the average testing time was 6.94 hours which corresponds to about 1000 test cases. For the randomly generated test set, the average testing time was 12.5 hours which corresponds to about 1800 test cases.

From this case study, the following results were obtained;

- There is a strong correlation between optimal test set results and subjective evaluation.
- The number of failures detected using the optimal test set is greater than the number of failures detected by the test set generated manually.
- For the same required reliability values, the number of test cases and the test time for the optimal test set are less than overall test set

This case study shows the high efficiency of optimal test case design.

6.2 ASIC Based Concept – Case Study 2

ASIC based chassis was chosen for case study 2. The software of the chassis will be changed as it can record the state changes. 20 samples are planned to be delivered to the personnel to record the state changes. With this data, optimum usage profile will be created.

In parallel, the modeling of user behavior is started. The expected state table was created. When the recorded state changes are obtained, the state table will be updated. The user model was created with respect to expected state table which is shown with APPENDIX.

Some of the snapshots of the user modeling works by using MaTeLo are given in Figure 6.4, Figure 6.5 and Figure 6.6.

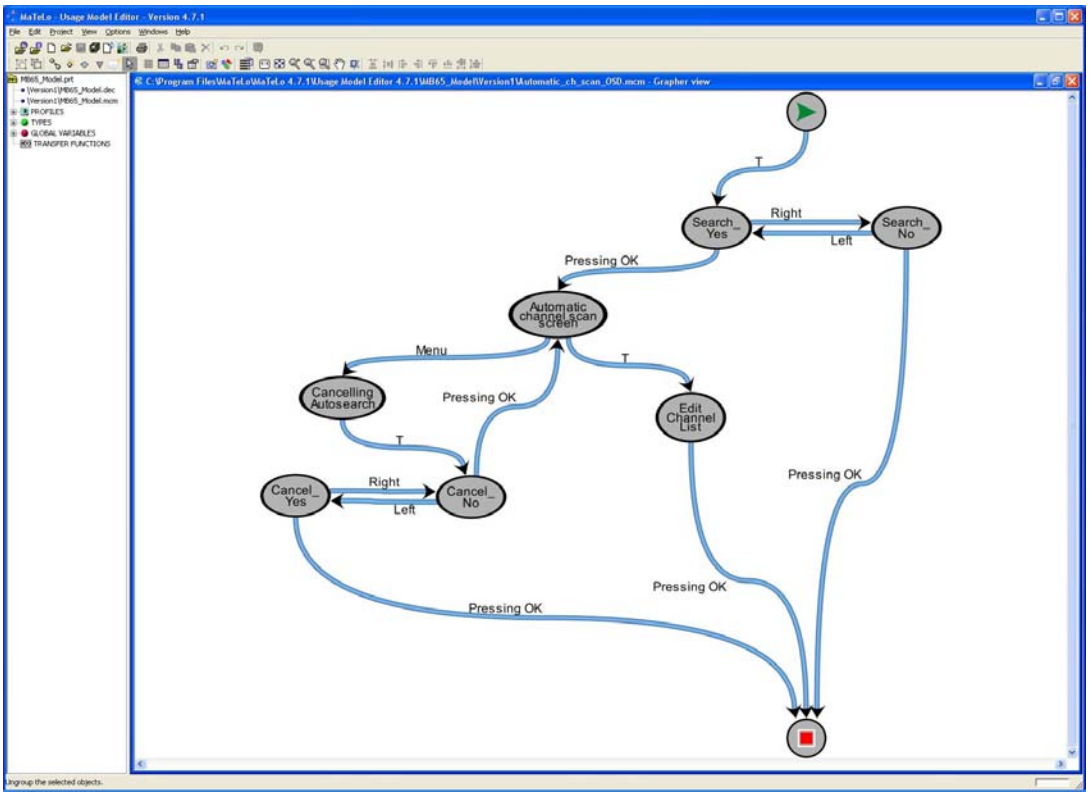

Figure 6.4 Auto scan menu

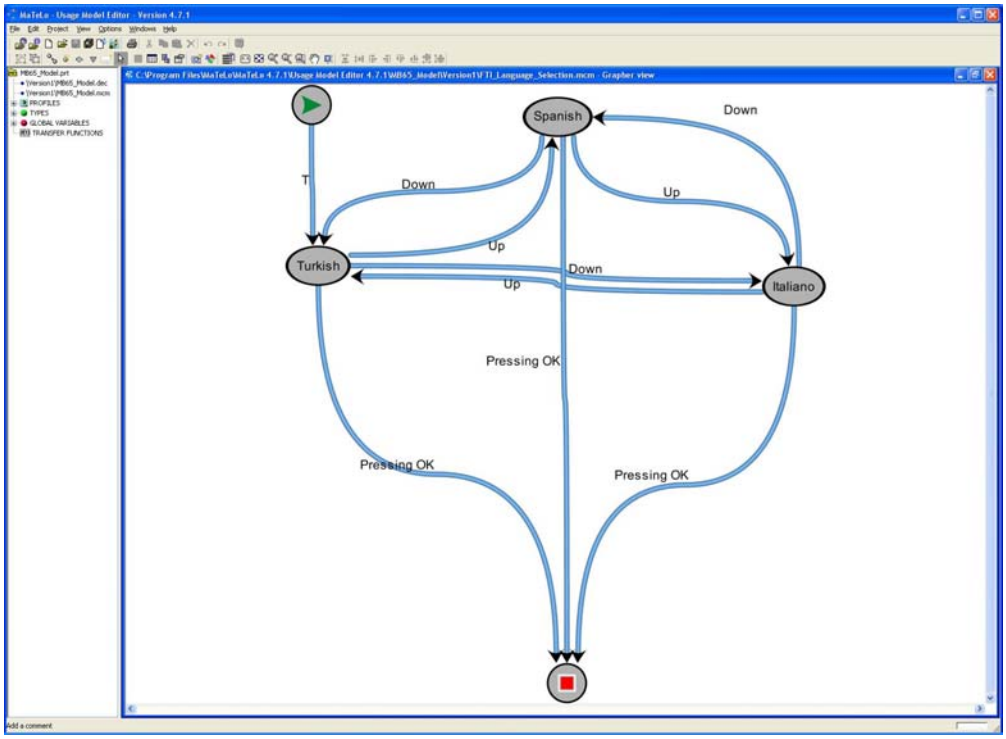

Figure 6.5 FTI language menu

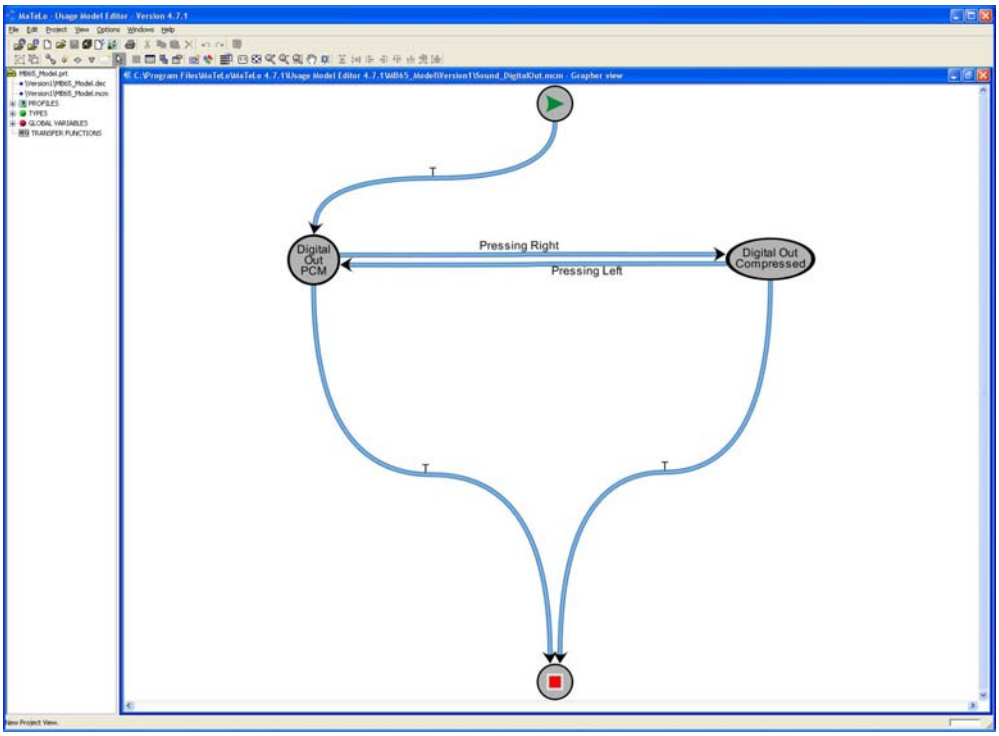

Figure 6.6 Sound digital out menu

CHAPTER SEVEN
FIELD RETURN RATE ESTIMATION

In this chapter, field return rate estimation method is introduced. First, the method of FRF in predictions is given in Section 7.1. Then, the proposed method is described with a real life case study in Section 7.2.

7.1 Using FRF in Prediction

The Failure Risk Factor (FRF) should be combined with traditional reliability and return rate predictions to get more accurate predictions. Two types of combination methods are given in the following sections.

7.1.1 First Method for Combining FRF with Other Predictions

$$PI = FRF \times \prod_{i=1}^{n} RR_n \tag{7.1}$$

where the symbols are defined as the following,

PI: Product Indicator which is also FRRI

FRF: Failure Risk Factor

RR: Predicted Return Rate for a specific period of time by using traditional methods

n: Number of Predicted Return Rate Values from Different Prediction Methods

The Product Indicator (PI) is a metric used to compare different projects, and it is not a measure of the product's return rate. In other words, PI is not an estimation of the product's return rate, rather a comparative metric whose magnitude is indicative of the relative magnitude of the field return rate (i.e., high or low), and it will be used in relation to the PI of other projects.

PI has a relation with the real/actual return rate of a $(n+1)^{th}$ degree for a specific time period, as it is calculated by multiplying (n+1) parameters which are all related in the 1^{st} degree with the real return rate.

$$\frac{PI_a}{PI_b} \approx m \times \left(\frac{RRR_a}{RRR_b} \right)^{n+1} \tag{7.2}$$

Where the symbols are defined as the following,

PI_a: a^{th} Project's Product Indicator

PI_b: b^{th} Project's Product Indicator

RR_a: a^{th} Project's Real Return Rate

RR_b: b^{th} Project's Real Return Rate

m: Relation Coefficient

To predict a new project's reliability and return rate more accurately by using this model, all the ratios of PI values and cube of the ratios of return rate values of old projects with respect to each other must be calculated. These ratios are called X-Points and Y-Points.

After the X and Y-points are determined, these points are plotted on the X-Y coordinate system. Then, the equation of the nearest line (y=mx+n) to these X-Y points is determined by using regression methods. It is assumed that, the new X-Y points of the new projects are on this line. By using this estimated line, every old project can have an effect on the predictions of new projects.

Then, the PI values of new projects are calculated. The ratios of new projects' PI values to old projects' PI values are called new X-points. After calculating new X-Points, new Y-Points are determined by using the line equation. New Y-Points are cube of the ratios of new projects' return rates to the old project's return rates. As the return rate values of old projects are known, return rate of new projects can be calculated. A real life case study for these calculations is given in the fourth section.

7.1.2 Second Method for Combining FRF with Other Predictions

In this method, PI function is changed as the following,

$$PI = FRF \times \left[\left(\sum_{i=1}^{n} RR_n \right) / n \right] \tag{7.3}$$

Where the symbols are defined as the following,

PI: Product Indicator

FRF: Failure Risk Factor

RR: Predicted Return Rate for a specific period of time by using traditional methods

n: Number of Predicted Return Rate Values from Different Prediction Methods

According to (7.3), PI has a relation with the real/actual return rate of a 2nd degree for a specific time period, as it is calculated by multiplying 2 types of parameters which are all related in the 1st degree with the real return rate. Therefore, (7.2) is changed into (7.4) as the following,

$$\frac{PI_a}{PI_b} \approx m \times \left(\frac{RRR_a}{RRR_b} \right)^2 \tag{7.4}$$

The other steps are the same with the previous method. The results of the 2 methods and the real data are given in the following section.

7.2 Case Study

A real life case study of predicting 1st year return rate of 7 TFT LCD TV projects with CCFL and LED panels (4 old, 3 new projects) are given. The PI values of all projects and the return rate values of old projects are given in Table 7.1.

In Table 7.1, each project number refers to a real TFT LCD TV product. RR_1 denotes the return rate calculated by MIL-HDBK-217F, RR_2 denotes the return rate calculated by applying accelerated life tests, and FRF denotes “failure risk factor”

calculated by applying the tests described in Section 2.5 and Section 2.6. PI_1 denotes "product indicator" which is calculated by using (7.1) and PI_2 denotes "product indicator" which is calculated by using (7.3) and RRR denotes real field return rate.

Table 7.1 PI and return rate values

Project	RR_1 (%)	RR_2 (%)	FRF	PI_1	PI_2	RRR(%)
1	10.69	4.00	0.351	14.992	2.575	4.190
2	7.56	1.82	0.173	2.373	0.809	2.600
3	4.85	0.26	0.064	0.081	0.164	0.870
4	5.02	2.83	0.105	1.492	0.412	1.570
5	5.00	0.48	0.090	0.216	0.247	RRR_5
6	3.61	0.46	0.114	0.190	0.233	RRR_6
7	7.61	1.21	0.090	0.829	0.397	RRR_7

7.2.1 Results of 1st Method

X and Y points are given in Table 7.2. Then, X-Y points are plotted and the equation of the estimated line is determined, which is given in Figure 7.1.

Table 7.2 *X-Points and Y-Points according to 1st method*

Product Indicator Ratios (X-Points)		Cube of Return Rate Ratios (Y-Points)	
PI_1/PI_2	6.32	$(RRR_1/RRR_2)^3$	4.18
PI_1/PI_3	185.76	$(RRR_1/RRR_3)^3$	111.71
PI_1/PI_4	10.05	$(RRR_1/RRR_4)^3$	19.01
PI_2/PI_3	29.40	$(RRR_2/RRR_3)^3$	26.69
PI_2/PI_4	1.59	$(RRR_2/RRR_4)^3$	4.54
PI_4/PI_3	18.47	$(RRR_4/RRR_3)^3$	5.87

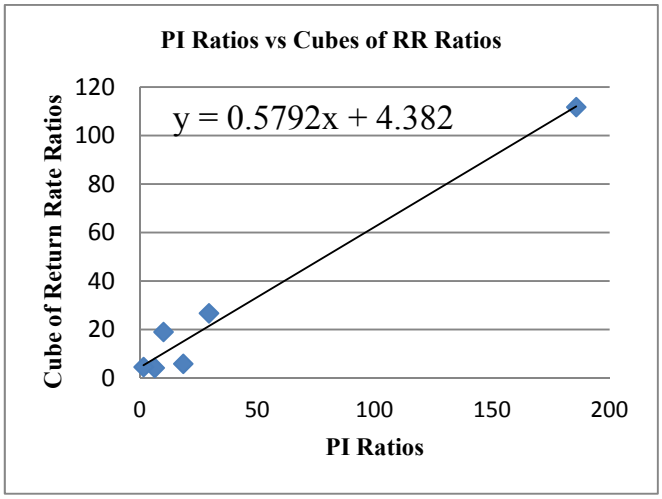

Figure 7.1 PI Ratio vs. Cube of return rate ratios

The ratios of old projects' PI values to new projects' PI values are calculated. These points are the "new X-points" (given in Table 7.3). With these new x-points, y-points are calculated by using the estimated line equation in Figure 7.1

Table 7.3 New X-Points and new Y-Points according to 1st method

PI Ratios (New X-Points)		**Cube of Return Rate Ratios (New Y-Points)**	
PI_1/PI_5	69.39	$(RRR_1/RRR_5)^3$	44.57
PI_2/PI_5	10.98	$(RRR_2/RRR_5)^3$	10.74
PI_5/PI_3	2.67	$(RRR_5/RRR_3)^3$	5.93
PI_4/PI_5	6.90	$(RRR_4/RRR_5)^3$	8.37
PI_1/PI_6	78.91	$(RRR_1/RRR_6)^3$	50.08
PI_2/PI_6	12.49	$(RRR_2/RRR_6)^3$	11.62
PI_6/PI_3	2.35	$(RRR_6/RRR_3)^3$	5.74
PI_4/PI_6	7.84	$(RRR_4/RRR_6)^3$	8.92
PI_1/PI_7	18.08	$(RRR_1/RRR_7)^3$	14.86
PI_2/PI_7	2.86	$(RRR_2/RRR_7)^3$	6.04
PI_7/PI_3	10.26	$(RRR_7/RRR_3)^3$	10.32
PI_4/PI_7	1.79	$(RRR_4/RRR_7)^3$	5.42

As the values of RR_1, RR_2, RR_3 and RR_4 are known (see Figure 7.1) RR5, RR6 and RR7 can be calculated. The results are given in Table 7.4.

At this point, 4 predicted field return rate values are obtained for each new project, as 4 old projects are used for prediction. Therefore, one can say that the field return rate of the new project for the 1st year will be between the lowest and the highest predicted value or will be around the average value.

Table 7.4 Return rate ratios and predicted return rate values

Return Rate Ratios		**Predicted Return Rate Values**		
			(%)	**Average (%)**
RRR_1/RRR_5	3.54	RRR_5	1.18	1.18
RRR_2/RRR_5	2.20	RRR_5	1.17	
RRR_5/RRR_3	1.81	RRR_5	1.57	
RRR_4/RRR_5	2.03	RRR_5	0.773	
RRR_1/RRR_6	3.68	RRR_6	1.13	1.15
RRR_2/RRR_6	2.26	RRR_6	1.15	
RRR_6/RRR_3	1.79	RRR_6	1.56	
RRR_4/RRR_6	2.07	RRR_6	0.757	
RRR_1/RRR_7	2.45	RRR_7	1.70	1.48
RRR_2/RRR_7	1.82	RRR_7	1.43	
RRR_7/RRR_3	2.17	RRR_7	1.89	
RRR_4/RRR_7	1.75	RRR_7	0.89	

7.2.2 Results of 2nd Method

X and Y points are given in Table 7.5. Then, X-Y points are plotted and the equation of the estimated line is determined, which is given in Figure 7.2.

Table 7.5 X-Points and Y-points according to 2nd method

Product Indicator Ratios (X-Points)		**Square of Return Rate Ratios (Y-Points)**	
PI_1/PI_2	3.18	$(RRR_1/RRR_2)^2$	2.59
PI_1/PI_3	15.74	$(RRR_1/RRR_3)^2$	23.19

Table 7.5 Continued

Product Indicator Ratios (X-Points)		Square of Return Rate Ratios (Y-Points)	
PI_1/PI_4	6.25	$(RRR_1/RRR_4)^2$	7.12
PI_2/PI_3	4.94	$(RRR_2/RRR_3)^2$	8.93
PI_2/PI_4	1.96	$(RRR_2/RRR_4)^2$	2.74
PI_4/PI_3	2.52	$(RRR_4/RRR_3)^2$	3.25

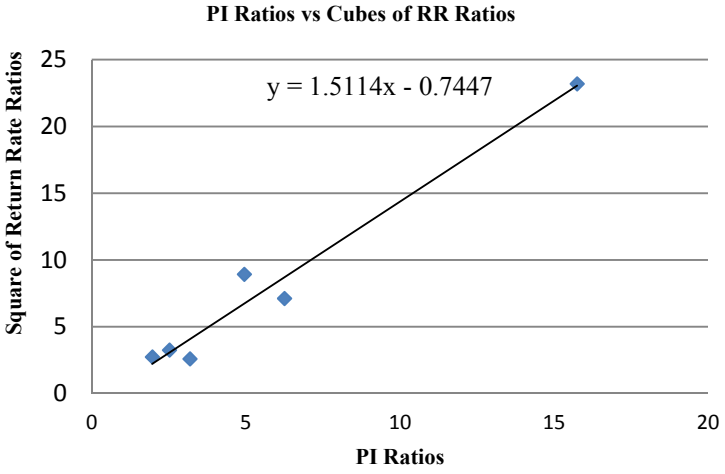

Figure 7.2 PI Ratio vs. Square of return rate ratios

The ratios of old projects' PI values to new projects' PI values are calculated. These points are the "new X-points" (given in Table 7.6). With these new x-points, y-points are calculated by using the estimated line equation in Figure 7.2 PI Ratio vs. Square of return rate ratios (also given in Table 7.6)

Table 7.6 X-Points and Y-Points according to 2nd method

PI Ratios (New X-Points)		Square of Return Rate Ratios (New Y-Points)	
PI_1/PI_5	10.44	$(RRR_1/RRR_5)^2$	15.03
PI_2/PI_5	3.28	$(RRR_2/RRR_5)^2$	4.21
PI_5/PI_3	1.50	$(RRR_5/RRR_3)^2$	1.53
PI_4/PI_5	1.67	$(RRR_4/RRR_5)^2$	1.78
PI_1/PI_6	11.06	$(RRR_1/RRR_6)^2$	15.97
PI_2/PI_6	3.47	$(RRR_2/RRR_6)^2$	4.50

Table 7.6 Continued

PI Ratios (New X-Points)		Square of Return Rate Ratios (New Y-Points)	
PI_6 / PI_3	1.42	$(RRR_6/RRR_3)^2$	1.40
PI_4 / PI_6	1.77	$(RRR_4/RRR_6)^2$	1.93
PI_1/PI_7	6.48	$(RRR_1/RRR_7)^2$	9.06
PI_2 / PI_7	2.04	$(RRR_2/RRR_7)^2$	2.33
PI_7 / PI_3	2.42	$(RRR_7/RRR_3)^2$	2.92
PI_4 / PI_7	1.04	$(RRR_4/RRR_7)^2$	0.82

The prediction results are given in Table 7.7.

Table 7.7 Return rate ratios and predicted return rate values

Return Rate Ratios		Predicted Return Rate Values		
			(%)	Average (%)
RRR_1/RRR_5	3.87	RRR_5	1.08	1.15
RRR_2/RRR_5	2.05	RRR_5	1.26	
RRR_5/RRR_3	1.24	RRR_5	1.08	
RRR_4/RRR_5	1.33	RRR_5	1.18	
RRR_1/RRR_6	3.99	RRR_6	1.05	1.11
RRR_2/RRR_6	2.12	RRR_6	1.22	
RRR_6/RRR_3	1.18	RRR_6	1.03	
RRR_4/RRR_6	1.38	RRR_6	1.13	
RRR_1/RRR_7	3.01	RRR_7	1.39	1.58
RRR_2/RRR_7	1.52	RRR_7	1.70	
RRR_7/RRR_3	1.70	RRR_7	1.48	
RRR_4/RRR_7	0.90	RRR_7	1.73	

7.2.3 Comparison of the Results with Real Data

The real 1st year return rate of the predicted products are given in Table 7.8. The values in Table 7.8 are obtained from the company's services.

Table 7.8 Real return rates of predicted products

Real 1st Year Field Return Rate Values (%)	
RRR_5	1.19
RRR_6	1.14
RRR_7	1.47

Comparison of all predictions with real 1st year field return rate values is given in Table 7.9.

Table 7.9 Comparison of all predictions with real 1st year return rate values

Project	**RR_1 (%)**	**RR_2 (%)**	**RR of 1st Method (%)**	**RR of 2nd Method (%)**	**Real RR (%)**
5	5.00	0.48	1.18	1.15	1.19
6	3.61	0.46	1.15	1.11	1.14
7	7.61	1.21	1.48	1.58	1.47

RR_1 denotes the return rate calculated by MIL-HDBK-217F (also given in Table 7.1). RR_2 denotes the return rate calculated by applying accelerated life tests (also given in Table 7.1).

As can be seen from table 7.9, the results of traditional prediction methods (RR_1 and RR2) are very different from the real return rate value. However, the predicted return rate values by using proposed methods are very close to real return rate values. Moreover, 1st method gives very close results to the real return rate data.

Reliability and return rate predictions are currently performed mainly by using stress based standards or applying accelerated life tests. However, these methods do not express every failure reason seen in the field. Therefore, a parameter, which is described in section 2, should be created to account for these “qualitative” issues, and this parameter should be used to adjust the return rate and reliability predictions of products. After this modification is done, more accurate predictions of reliability and return rate can be obtained.

CHAPTER EIGHT
INCORPORATING MATURITY LEVEL IN FIELD RETURN RATE PREDICTIONS USING ARTIFICIAL NEURAL NETWORKS

Additional method is disclosed in this chapter to combine Maturity Level with traditional prediction methods. To demonstrate the methodology and the accuracy of the model, a real life case study on 4 LCD TFT TV projects is given.

At this point, the challenge is to combine the computed Robustness Level Factor with predictions made from life tests. As mentioned previously, the motivation is to consider these qualitative failures in our predictions since they represent possible failures in the field. Failing to consider the design robustness in any predictions could result in less accurate estimations. Since the ML is a qualitative factor (i.e. it does not represent an actual probability) it cannot be easily related to field failures. In order to achieve this, we chose ANN, where a relationship between ML and life test predictions vs. actual field return rate (based on past projects) can be established / learned. In other words, from past projects, ML and reliability predictions based on life tests will be the inputs and the actual field return rate the output, and an ANN will be used to "learn" the function between them. Based on the established function, the ML and the life test reliability prediction of the product under development, we will infer its field return rate.

In engineering and science, ANNs are used whenever a function between inputs and outputs needs to be established, where such function is very complex to be determined with other methods or non-applicable (e.g. linear regression). The problem of combining robustness tests results and life test results under the investigation falls under this category where no known relationship exists and using ANN thus offers an approach to establish it.

In order to increase the accuracy in the predictions and to take into account the maturity level of the design, ANNs will be utilized. In other words, the proposed methodology aims to improve the field return rate prediction by taking into account

the accelerated life test results and the ML. ANN requires existing inputs and outputs to be provided and based on those a function is built. The existing inputs and outputs are called the "training set." In other words, these are the set of values where the algorithm will learn the pattern. In our application, the training set will be the ML, reliability predictions based on life tests and actual field returns of past projects. The higher the number of past projects used in the training set the more accurate the relationship between inputs and outputs is expected to be. It should also be noted that the proposed methodology and the past projects used apply when making predictions for similar products and for products where history exists (i.e. evolutionary designs).

There are different techniques and algorithms for creating ANNs which are beyond the scope of this thesis. In our application, since we only consider two inputs and one output, we used a simple single layer ANN. A real life case study for a LCD TFT TV set is given in the following section.

8.1 ANN Case Study

A real life case study to predict reliability and 1st year field return rate values of 3 LCD TFT TV Set projects, with CCFL and LED panels, is given by using 4 older projects' RLF values, accelerated life test predictions, and actual field return rate data (Table 8.1). These 3 products are currently in the field for more than a year, and their actual 1st year return rates will be provided as a comparison to the predicted ones, to illustrate the applicability of the model.

Table 8.1 Rlf values, accelerated life test results and actual field return rate values

Project	RR_{ALT} (%)	90% 1S UPPER RR_{ALT} (%)	ML	AFRR (%)
1	4.00	7.98	0,6494	4.19
2	1.82	9.26	0.8275	2.60
3	0.26	4.60	0.9360	0.87
4	2.83	11.75	0.8950	1.57

In Table 8.1, each project number refers to a real TFT LCD TV product. RR_{ALT} denotes the estimated return rate (50% confidence level) calculated by applying accelerated life tests, 90% 1S UPPER RR_{ALT} denotes the 90% upper one-sided bound return rate, and ML denotes "robustness level factor" calculated by applying the tests described in Section II and using the same scoring points provided in that same section. AFRR denotes actual field return rate.

There are a few observations that can be made by examining the information provided in Table 8.1.

1. The upper bounds are significantly higher than the estimated values. This is due to the small sample sizes used during the ALT,
2. The upper bounds are significantly higher than the actual field return rates,
3. The estimated values (i.e. 50% confidence level) are closer to the actual field return rates.

One could observe that the actual field returns rates are below the upper bound computed from the ALT analysis, which is the reason of using confidence bounds, i.e. to contain the uncertainty due to sample size. The statement that can be made is that we are 90% confident that the true field returns rate will be below the upper bound. However, it can be seen that this bound is very conservative and additionally we need to keep in mind that it does not consider any robustness related failures in the field. In other words, even though the true values given in Table 8.1 are contained within the bounds, one need to be careful because it is no indication that the robustness related failures are included in the estimation. There may very well be situations where if sufficient number of samples were tested during the ALT, the upper bound would be close to the estimate and could also be below the actual.

We would now like to better understand the relationship between the ALT predictions and the robustness of the product in order to make more intelligent field

return rate predictions. For this, we will use ANN. Table 8.2 provides the ALT results and the ML values for 3 projects currently in the field over 1 year. The actual field returns rates are known but we will use the proposed methodology to estimate them and later compare them to the actual values.

Table 8.2 Rlf values and accelerated life test results

Project	**RR_{ALT} (%)**	**90% 1S UPPER RR_{ALT} (%)**	**ML**
5	0.48	0.66	0.9100
6	0.46	19.55	0.8856
7	1.21	13.73	0.9100

In Table 8.2 we can see that for Project 5 it is expected that the true field return rate will be below 0.66% based on the ALT analysis. In this project it can also be seen that the 90% upper bound is close to the estimated value. This is due to the fact that sufficient samples were tested and for sufficient duration during the development of this product. On the other hand, in projects 6 and 7, less time and samples were available during development and this is reflected in the width between the estimated values and the upper bounds. Based on the history of these products (these 3 products are evolutions of the previous 4 products given in table 8.1), we do not expect the actual field return rate to be as high as predicted by 90% upper bound estimates. In addition, our robustness tests have shown that the robustness of these 3 products is high as reflected in the ML values.

To summarize, we have high confidence in the prediction for project 5 and the actual field return rate is expected to be close to this prediction. However, we need to keep in mind that this prediction does not take into account any robustness related failures which may occur in the field. On the other hand, we are more uncertain about the ALT predictions for projects 6 and 7 and we believe (based on history) that the actual field return rate should be less than these predictions, which also do not include robustness related failures. Finally, all 3 projects have quite high ML values thus we expect less robustness related failures in the field.

8.2 Analysis and Results

To apply the methodology, we will use the values provided in table 8.1 as the "training set" for the ANN algorithm. Based on this training set, the ANN will create a relationship between the inputs which are the ALT estimates and the ML values, and the output which is the AFRR. We will use the 90% upper confidence bound estimate as the ALT input since it provides an estimate which contains the uncertainty of the result.

An ANN was created using the training set described above. We used a single layer ANN with no neuron in hidden layers, a minimum weight delta of 0.0001, a learning rate of 0.3, and a zero-based Log-sigmoid-function for the activation function. Based on this ANN and the training set of table 8.1, the field return rate of the 3 projects with inputs given table 8.2 was predicted, and is given in table 8.3.

Table 8.3 Predicted field return rate values

Predicted Field Return Rate Values (%)	
$PFRR_5$	0.929
$PFRR_6$	2.277
$PFRR_7$	1.459

The following observations can be made from the results of Table 8.3;

1. The predicted field return rate for Project 5 is higher than the 90% upper bound value based on ALT analysis. This outcome is actually reasonable, since, as we mentioned previously, the ALT does not consider any robustness related failures where in the field we do expect to see such failures.

2. For projects 6 and 7 the predicted field return rates are much lower than the 90% upper bound value based on accelerated life test analysis. This is also a

reasonable outcome as these projects have historically much less failures than what was predicted by the ALT analysis. In addition, they also have a high ML value which implies consistency and/or improvement over past projects thus similar expectations regarding robustness related failures.

8.3 Comparison of Predictions with Actual Field Return Rates

As mentioned before, these 3 products are already in the field for more than a year. To illustrate the accuracy of the proposed model and prediction, the actual field returned rates (as obtained from our service department) are given in table 8.4 and are compared to the predicted values in Table 8.3.

Table 8.4 Actual and predicted 1st year field return rate values

Project	Predicted Field Return Rate (%)	Actual Field Return Rate
5	0.929	1.19
6	2.277	1.14
7	1.459	1.47

As it can be seen from Table 8.4, the results of the predicted field return rate values by using proposed method are very close to the actual field return rate values and thus more realistic.

CHAPTER NINE
CONCLUSIONS

Many companies have reliability test programs and perform reliability tests during the design phase. However, in this thesis, the outcome of the reliability tests is used to calculate a metric, which is called maturity level, and this metric is combined by traditional reliability prediction methods to predict the reliability of the product more accurately. First, the maturity level calculation method is introduced and the required tests (reliability approval tests, design verification tests and board level tests) are defined. These tests are robustness related tests which should be performed during design phase. Secondly, the studies on software reliability are given. Software reliability testing is time consuming so, in this thesis, optimal test case design is introduced with a real life case study. Finally, the combination of maturity level with traditional reliability prediction methods is given to predict reliability more accurately.

Reliability and return rate predictions are currently performed mainly by using stress based standards or applying accelerated life tests. However, these methods do not capture every failure reason seen in the field, and specifically robustness related failures. In addition, there is typically a variety of robustness tests performed during development whose outcome indicates the likelihood of observing such failures in the field. Traditionally, the lessons learned and the outcomes of these tests are not taken into consideration when field predictions are performed. It is reasonable to assume that such information regarding a product's robustness should have an influence on the field return rate. For these reasons, we first proposed a parameter to quantify a product's maturity, i.e., ML, using scoring points for the different robustness tests (as described in section II), and then, we used this parameter in conjunction with life test results in order to make more realistic field return rate predictions. To achieve this, we used information from past projects and artificial neural networks in order to create a relationship between the life test results, the ML and the actual field return rate. The choice of ANNs as a technique was based on the fact that we are not certain about the form of the relationship between these inputs

and the output, which could also vary by the application, the product, the historical information, etc. Thus, ANNs provide a general approach which can be used in a variety of products and industries.

The methodology has been proved to be a significantly useful approach by providing more realistic predictions, which was demonstrated in this thesis by the provided case study. Further utilization of this approach by other industries or reliability engineers would be helpful in order to determine its applicability and value. It should also be noted that our presented approach is an attempt to consider this very real case of including information regarding the robustness of a product and in general any type of qualitative information and test results in the final field return rate prediction. We hope that this approach can also generate interest in this topic and provide stimulation for further research. In fact, the authors are currently also considering other approaches such as using Bayesian statistics as a future work.

The outcome of all these long procedures and numerous tests is a very reliable and robust product with an affordable cost. It is obvious that a complete trouble or failure free power board cannot be produced; however, the error types and risk levels are estimated, before the mass production.

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APPENDIX

EXPECTED STATE TABLE

Table A.1 Expected state table

STATE_SRC	TRANSITION	TRANSITION PROB.	EVENT	EVENT PROB.	STATE_DEST.	DELAY
Initial State(Power off)	Plug on	1.0	Power_on	1.0	Power on_Stbyon	
Power on_Stbyon	Turning on with Digit keys	0.3	0	0.1	FTI Menu-Language	20
			1	0.1		
			2	0.1		
			3	0.1		
			4	0.1		
			5	0.1		
			6	0.1		
			7	0.1		
			8	0.1		
			9	0.1		
	Turning on with Navigation keys	0.3	Arrow_Up	0.25		20
			Arrow_Down	0.25		
			Prog_Up	0.25		
			Prog_Down	0.25		
	Turning on with Stby key	0.4	Stby_key	1		20
Turkish	Pressing OK	0.34	OK_Select	1	FTI Country	
	Up	0.33	Arrow_Down	1	Spanish	
	Down	0.33	Arrow_Up	1	Italiano	
Spanish	Pressing OK	0.34	OK_Select	1	FTI Country	
	Up	0.33	Arrow_Down	1	Italiano	
	Down	0.33	Arrow_Up	1	Turkish	
Italiano	Pressing OK	0.34	OK_Select	1	FTI Country	
	Up	0.33	Arrow_Down	1	Spanish	
	Down	0.33	Arrow_Up	1	Turkish	
Turkey	Left	0.3	Arrow_Left	1	Switzerland	
	Right	0.2	Arrow_Right	1	Croatia	
	Up	0.1	Arrow_Up	1	FTI Scan Encrypted channels	

Table A.1 Continued

STATE_SRC	TRANSITION	TRANSITION PROB.	EVENT	EVENT PROB.	STATE_DEST.	DELAY
	Down	0.1	Arrow_Down	1	FTI Teletext Language	
	Pressing OK	0.3	OK_Select	1	Automatic Scan OSD	
Switzerland	Left	0.3	Arrow_Left	1	Croatioa	
	Right	0.2	Arrow_Right	1	Turkey	
	Up	0.1	Arrow_Up	1	FTI Scan Encrypted channels	
	Down	0.1	Arrow_Down	1	FTI Teletext Language	
	Pressing OK	0.3	OK_Select	1	Automatic Scan OSD	
Croatia	Left	0.3	Arrow_Left	1	Turkey	
	Right	0.2	Arrow_Right	1	Switzerland	
	Up	0.1	Arrow_Up	1	FTI Scan Encrypted channels	
	Down	0.1	Arrow_Down	1	FTI Teletext Language	
	Pressing OK	0.3	OK_Select	1	Automatic Scan OSD	
Yes	Right	0.2	Arrow_Right	0.5	No	
	Left	0.2	Arrow_Left	0.5	No	
	Up	0.1	Arrow_Up	1	FTI Teletext Language	
	Down	0.1	Arrow_Down	1	FTI Country	
	Pressing OK	0.4	OK_Select	1	Automatic Scan OSD	
No	Left	0.2	Arrow_Left	0.5	Yes	
	Right	0.2	Arrow_Right	0.5	Yes	
	Up	0.1	Arrow_Up	1	FTI Teletext Language	
	Down	0.1	Arrow_Down	1	FTI Country	
	Pressing OK	0.4	OK_Select	1	Automatic Scan OSD	
West	Right	0.3	Arrow_Right	1	East	

Table A.1 Continued

STATE_SRC	TRANSITION	TRANSITION PROB.	EVENT	EVENT PROB.	STATE_DEST.	DELAY
	Left	0.2	Arrow_Left	1	Arabic	
	Down	0.1	Arrow_Down	1	FTI Scan Encrypted channels	
	Up	0.1	Arrow_Up	1	FTI Country	
	Pressing OK	0.3	OK_Select	1	Automatic Scan OSD	
East	Right	0.3	Arrow_Right	1	Cyrillic	
	Left	0.2	Arrow_Left	1	West	
	Down	0.1	Arrow_Down	1	FTI Scan Encrypted channels	
	Up	0.1	Arrow_Up	1	FTI Country	
	Pressing OK	0.3	OK_Select	1	Automatic Scan OSD	
Cyrillic	Right	0.3	Arrow_Right	1	Turk/Gre	
	Left	0.2	Arrow_Left	1	East	
	Down	0.1	Arrow_Down	1	FTI Scan Encrypted channels	
	Up	0.1	Arrow_Up	1	FTI Country	
	Pressing OK	0.3	OK_Select	1	Automatic Scan OSD	
Turk/Gre	Right	0.3	Arrow_Right	1	Arabic	
	Left	0.2	Arrow_Left	1	Cyrillic	
	Down	0.1	Arrow_Down	1	FTI Scan Encrypted channels	
	Up	0.1	Arrow_Up	1	FTI Country	
	Pressing OK	0.3	OK_Select	1	Automatic Scan OSD	
Arabic	Right	0.3	Arrow_Right	1	West	
	Left	0.2	Arrow_Left	1	Turk/Gre	
	Down	0.1	Arrow_Down	1	FTI Scan Encrypted channels	
	Up	0.1	Arrow_Up	1	FTI Country	

Table A.1 Continued

STATE_SRC	TRANSITION	TRANSITION PROB.	EVENT	EVENT PROB.	STATE_DEST.	DELAY
	Pressing OK	0.3	OK_Select	1	Automatic Scan OSD	
Search_Yes	Right	0.4	Arrow_Right	1	No	
	Pressing OK	0.6	OK_Select	1	Automatic Channel Scan	
Search_No	Left	0.4	Arrow_Right	1	Yes	
	Pressing OK	0.6	OK_Select	1	Automatic Channel Scan	
Automatic Channel Scan	Menu	1	Menu	1	Cancelling Auto Search	
Cancel_Yes	Right	0.4	Arrow_Right	1	Cancel_No	
	Pressing OK	0.6	OK_Select	1	RF Receive Mode	
Cancel_No	Left	0.4	Arrow_Left	1	Cancel_No	
	Pressing OK	0.6	OK_Select	1	RF Receive Mode	
RF Receive Mode	Pressing menu	0.6	Menu	1	menu_cond	
	Pressing Source	0.4	Source	1	source_cond	
source_cond					TV	
					EXT1	
					EXT2	
					EXT2-S	
					SIDE AV	
					HDMI 1	
					HDMI 2	
					HDMI 3	
					HDMI 4	
					YPbPr	
					VGA/PC	
TV	Pressing OK	1	OK_Select	1	TV mode	
EXT1	Pressing OK	1	OK_Select	1	EXT1 mode	
EXT2	Pressing OK	1	OK_Select	1	EXT2 mode	
EXT2-S	Pressing OK	1	OK_Select	1	EXT2-S mode	
SIDE AV	Pressing OK	1	OK_Select	1	SIDE AV mode	

Table A.1 Continued

STATE_SRC	TRANSITION	TRANSITION PROB.	EVENT	EVENT PROB.	STATE_DEST.	DELAY
HDMI 1	Pressing OK	1	OK_Select	1	HDMI 1 mode	
HDMI 2	Pressing OK	1	OK_Select	1	HDMI 2 mode	
HDMI 3	Pressing OK	1	OK_Select	1	HDMI 3 mode	
HDMI 4	Pressing OK	1	OK_Select	1	HDMI 4 mode	
YPbPr	Pressing OK	1	OK_Select	1	YPbPr mode	
VGA/PC	Pressing OK	1	OK_Select	1	VGA/PC mode	
TV mode	Pressing menu	1	Menu	1	menu_cond	
EXT1 mode	Pressing menu	1	Menu	1	menu_cond	
EXT2 mode	Pressing menu	1	Menu	1	menu_cond	
EXT2-S mode	Pressing menu	1	Menu	1	menu_cond	
SIDE AV mode	Pressing menu	1	Menu	1	menu_cond	
HDMI 1 mode	Pressing menu	1	Menu	1	menu_cond	
HDMI 2 mode	Pressing menu	1	Menu	1	menu_cond	
HDMI 3 mode	Pressing menu	1	Menu	1	menu_cond	
HDMI 4 mode	Pressing menu	1	Menu	1	menu_cond	
YPbPr mode	Pressing menu	1	Menu	1	menu_cond	
VGA/PC mode	Pressing menu	1	Menu	1	menu_cond	
menu_cond					Picture	
					Sound	
					Settings	
					Install and Retune	
					Channel List	
					Media Browser	
Picture	Pressing Right	0.3	Arrow_Right	1	Sound	
	Pressing Left	0.2	Arrow_Left	1	Media Browser	
	Pressing OK	0.3	OK_Select	1	Picture Menu	
Sound	Pressing Right	0.3	Arrow_Right	1	Settings	
	Pressing Left	0.2	Arrow_Left	1	Picture	
	Pressing OK	0.3	OK_Select	1	Sound Menu	
Settings	Pressing Right	0.3	Arrow_Right	1	Install and Retune	
	Pressing Left	0.2	Arrow_L	1	Sound	

Table A.1 Continued

STATE_SRC	TRANSITION	TRANSITION PROB.	EVENT	EVENT PROB.	STATE_DEST.	DELAY
			eft			
	Pressing OK	0.3	OK_Select	1	Settings Menu	
Install and Retune	Pressing Right	0.3	Arrow_Right	1	Channel List	
	Pressing Left	0.2	Arrow_Left	1	Settings	
	Pressing OK	0.3	OK_Select	1	Install and Retune Menu	
Channel List	Pressing Right	0.3	Arrow_Right	1	Media Browser	
	Pressing Left	0.2	Arrow_Left	1	Install and Retune	
	Pressing OK	0.3	OK_Select	1	Channel List Menu	
Media Browser	Pressing Right	0.3	Arrow_Right	1	Picture	
	Pressing Left	0.2	Arrow_Left	1	Channel List	
	Pressing OK	0.3	OK_Select	1	Media Browser Menu	
PictureMenu_dynamic	Pressing Right	0.3	Arrow_Right	1	Picture Menu_natural	
	Pressing Left	0.2	Arrow_Left	1	Picture Menu_game	
	Pressing Up	0.2	Arrow_Up	1	Dynamic_Reset	
	Pressing Down	0.2	Arrow_Down	1	Dynamic_Contrast	
	Pressing Back	0.1	Return	1	Picture	
PictureMenu_natural	Pressing Right	0.3	Arrow_Right	1	Picture Menu_cinema	
	Pressing Left	0.2	Arrow_Left	1	Picture Menu_dynamic	
	Pressing Up	0.2	Arrow_Up	1	Natural_Reset	
	Pressing Down	0.2	Arrow_Down	1	Natural_Contrast	
	Pressing Back	0.1	Return	1	Picture	
PictureMenu_cinema	Pressing Right	0.3	Arrow_Right	1	Picture Menu_game	
	Pressing Left	0.2	Arrow_Left	1	Picture Menu_natural	
	Pressing Up	0.2	Arrow_Up	1	Cinema_Reset	
	Pressing Down	0.2	Arrow_Down	1	Cinema_Contrast	
	Pressing Back	0.1	Return	1	Picture	

Table A.1 Continued

STATE_SRC	TRANSITION	TRANSITION PROB.	EVENT	EVENT PROB.	STATE_DEST.	DELAY
PictureMenu_game	Pressing Right	0.3	Arrow_Right	1	PictureMenu_dynamic	
	Pressing Left	0.2	Arrow_Left	1	PictureMenu_natural	
	Pressing Up	0.2	Arrow_Up	1	Game_Colorshift	
	Pressing Down	0.2	Arrow_Down	1	Game_picturezoom	
	Pressing Back	0.1	Return	1	Picture	
Dynamic_Contrast	Pressing Up	0.4	Arrow_Up	1	PictureMenu_dynamic	
	Pressing Down	0.4	Arrow_Down	1	Dynamic_Brightness	
	Pressing Back	0.2	Return	1	Picture	
Dynamic_Brightness	Pressing Up	0.4	Arrow_Up	1	Dynamic_Contrast	
	Pressing Down	0.4	Arrow_Down	1	Dynamic_Sharpness	
	Pressing Back	0.2	Return	1	Picture	
Dynamic_Sharpness	Pressing Up	0.4	Arrow_Up	1	Dynamic_Brightness	
	Pressing Down	0.4	Arrow_Down	1	Dynamic_Colour	
	Pressing Back	0.2	Return	1	Picture	
Dynamic_Colour	Pressing Up	0.4	Arrow_Up	1	Dynamic_Sharpness	
	Pressing Down	0.4	Arrow_Down	1	Dynamic_ColourShift	
	Pressing Back	0.2	Return	1	Picture	
Dynamic_ColourShift	Pressing Up	0.4	Arrow_Up	1	Dynamic_Colour	
	Pressing Down	0.4	Arrow_Down	1	Dynamic_Colourtemp	
	Pressing Back	0.2	Return	1	Picture	
Dynamic_Colourtemp	Pressing Up	0.25	Arrow_Up	1	Dynamic_ColourShift	
	Pressing Down	0.25	Arrow_Down	1	Dynamic_NoiseReduction	
	Pressing Back	0.1	Return	1	Picture	
	Pressing Right	0.2	Arrow_Right	0.5	Dynamic_Colourte	

Table A.1 Continued

STATE_SRC	TRANSITION	TRANSITION PROB.	EVENT	EVENT PROB.	STATE_DEST.	DELAY
					mp_Normal	
	Pressing Left	0.2	Arrow_Left	0.5	Dynamic_Colourtemp_Normal	
Dynamic_Colourtemp_Normal	Pressing Right	0.5	Arrow_Right	0.5	Dynamic_Colourtemp_Warm	
	Pressing Left	0.5	Arrow_Left	0.5	Dynamic_Colourtemp_Cool	
Dynamic_Colourtemp_Warm	Pressing Right	0.5	Arrow_Right	0.5	Dynamic_Colourtemp_Cool	
	Pressing Left	0.5	Arrow_Left	0.5	Dynamic_Colourtemp_Normal	
Dynamic_Colourtemp_Cool	Pressing Right	0.5	Arrow_Right	0.5	Dynamic_Colourtemp_Normal	
	Pressing Left	0.5	Arrow_Left	0.5	Dynamic_Colourtemp_Warm	
Dynamic_NoiseReduction	Pressing Up	0.25	Arrow_Up	1	Dynamic_Colourtemp	
	Pressing Down	0.25	Arrow_Down	1	Dynamic_PicZoom_Sub	
	Pressing Back	0.1	Return	1	Picture	
	Pressing Right	0.2	Arrow_Right	0.5	Dynamic_NoiseReduction_Low	
	Pressing Left	0.2	Arrow_Left	0.5	Dynamic_NoiseReduction_Low	
Dynamic_NoiseReduction_Low	Pressing Right	0.5	Arrow_Right	1	Dynamic_NoiseReduction_Medium	
	Pressing Left	0.5	Arrow_Left	1	Dynamic_NoiseReduction_Off	
Dynamic_NoiseReduction_Medium	Pressing Right	0.5	Arrow_Right	1	Dynamic_NoiseReduction_High	
	Pressing Left	0.5	Arrow_Left	1	Dynamic_NoiseReduction_Low	
Dynamic_NoiseReduction_High	Pressing Right	0.5	Arrow_Right	1	Dynamic_NoiseReduction_Off	
	Pressing Left	0.5	Arrow_Left	1	Dynamic_NoiseReduction_Medium	
Dynamic_NoiseReduction_Off	Pressing Right	0.5	Arrow_Right	1	Dynamic_NoiseReduction_Low	

Table A.1 Continued

STATE_SRC	TRANSITION	TRANSITION PROB.	EVENT	EVENT PROB.	STATE_DEST.	DELAY
	Pressing Left	0.5	Arrow_Left	1	Dynamic_NoiseReduction_High	
Dynamic_PicZoom_Sub	Pressing Up	0.25	Arrow_Up	1	Dynamic_NoiseReduction	
	Pressing Down	0.25	Arrow_Down	1	Dynamic_Reset	
	Pressing Back	0.1	Return	1	Picture	
	Pressing Right	0.2	Arrow_Right	1	Dynamic_PicZoom_14:9	
	Pressing Left	0.2	Arrow_Left	1	Dynamic_PicZoom_16:9	
Dynamic_PicZoom_14:9	Pressing Right	0.5	Arrow_Right	1	Dynamic_PicZoom_14:9_Zoom	
	Pressing Left	0.5	Arrow_Left	1	Dynamic_PicZoom_Sub	
Dynamic_PicZoom_14:9_Zoom	Pressing Right	0.5	Arrow_Right	1	Dynamic_PicZoom_4:3	
	Pressing Left	0.5	Arrow_Left	1	Dynamic_PicZoom_14:9	
Dynamic_PicZoom_4:3	Pressing Right	0.5	Arrow_Right	1	Dynamic_PicZoom_Panoramic	
	Pressing Left	0.5	Arrow_Left	1	Dynamic_PicZoom_14:9_Zoom	
Dynamic_PicZoom_Panoramic	Pressing Right	0.5	Arrow_Right	1	Dynamic_PicZoom_Cinema	
	Pressing Left	0.5	Arrow_Left	1	Dynamic_PicZoom_4:3	
Dynamic_PicZoom_Cinema	Pressing Right	0.5	Arrow_Right	1	Dynamic_PicZoom_Auto	
	Pressing Left	0.5	Arrow_Left	1	Dynamic_PicZoom_Panoramic	
Dynamic_PicZoom_Auto	Pressing Right	0.5	Arrow_Right	1	Dynamic_PicZoom_16:9	
	Pressing Left	0.5	Arrow_Left	1	Dynamic_PicZoom_Cinema	
Dynamic_PicZoom_16:9	Pressing Right	0.5	Arrow_Right	1	Dynamic_PicZoom_Sub	
	Pressing Left	0.5	Arrow_Left	1	Dynamic_PicZoom	

Table A.1 Continued

STATE_SRC	TRANSITION	TRANSITION PROB.	EVENT	EVENT PROB.	STATE_DEST.	DELAY
					_Auto	
Dynamic_Reset	Pressing Up	0.25	Arrow_Up	1	Dynamic_PicZoom_Sub	*
	Pressing Down	0.25	Arrow_Down	1	PictureMenu_dynamic	
	Pressing Back	0.1	Return	1	Picture	
	Pressing Ok	0.4	OK_Select	1	Dynamic_Reset	
Natural_Contrast	Pressing Up	0.4	Arrow_Up	1	PictureMenu_natural	
	Pressing Down	0.4	Arrow_Down	1	Natural_Brightness	
	Pressing Back	0.2	Return	1	Picture	
Natural_Brightness	Pressing Up	0.4	Arrow_Up	1	Natural_Contrast	
	Pressing Down	0.4	Arrow_Down	1	Natural_Sharpness	
	Pressing Back	0.2	Return	1	Picture	
Natural_Sharpness	Pressing Up	0.4	Arrow_Up	1	Natural_Brightness	
	Pressing Down	0.4	Arrow_Down	1	Natural_Colour	
	Pressing Back	0.2	Return	1	Picture	
Natural_Colour	Pressing Up	0.4	Arrow_Up	1	Natural_Sharpness	
	Pressing Down	0.4	Arrow_Down	1	Natural_ColourShift	
	Pressing Back	0.2	Return	1	Picture	
Natural_ColourShift	Pressing Up	0.4	Arrow_Up	1	Natural_Colour	
	Pressing Down	0.4	Arrow_Down	1	Natural_Colourtemp	
	Pressing Back	0.2	Return	1	Picture	
Natural_Colourtemp	Pressing Up	0.25	Arrow_Up	1	Natural_ColourShift	
	Pressing Down	0.25	Arrow_Down	1	Natural_NoiseReduction	
	Pressing Back	0.1	Return	1	Picture	
	Pressing Right	0.2	Arrow_Right	0.5	Natural_Colourtemp_Normal	
	Pressing Left	0.2	Arrow_Left	0.5	Natural_Colourtemp_Normal	
Natural_Colou	Pressing	0.5	Arrow_R	1	Natural	

Table A.1 Continued

STATE_SRC	TRANSITION	TRANSITION PROB.	EVENT	EVENT PROB.	STATE_DEST.	DELAY
rtemp_Normal	Right		ight		_Colourtemp_Warm	
	Pressing Left	0.5	Arrow_Left	1	Natural_Colourtemp_Cool	
Natural_Colourtemp_Warm	Pressing Right	0.5	Arrow_Right	1	Natural_Colourtemp_Cool	
	Pressing Left	0.5	Arrow_Left	1	Natural_Colourtemp_Normal	
Natural_Colourtemp_Cool	Pressing Right	0.5	Arrow_Right	1	Natural_Colourtemp_Normal	
	Pressing Left	0.5	Arrow_Left	1	Natural_Colourtemp_Warm	
Natural_NoiseReduction	Pressing Up	0.25	Arrow_Up	1	Natural_Colourtemp	
	Pressing Down	0.25	Arrow_Down	1	Natural_PicZoom_Sub	
	Pressing Back	0.1	Return	1	Picture	
	Pressing Right	0.2	Arrow_Right	0.5	Natural_NoiseReduction_Low	
	Pressing Left	0.2	Arrow_Left	0.5	Natural_NoiseReduction_Low	
Natural_NoiseReduction_Low	Pressing Right	0.5	Arrow_Right	1	Natural_NoiseReduction_Medium	
	Pressing Left	0.5	Arrow_Left	1	Natural_NoiseReduction_Off	
Natural_NoiseReduction_Medium	Pressing Right	0.5	Arrow_Right	1	Natural_NoiseReduction_High	
	Pressing Left	0.5	Arrow_Left	1	Natural_NoiseReduction_Low	
Natural_NoiseReduction_High	Pressing Right	0.5	Arrow_Right	1	Natural_NoiseReduction_Off	
	Pressing Left	0.5	Arrow_Left	1	Natural_NoiseReduction_Medium	
Natural_NoiseReduction_Off	Pressing Right	0.5	Arrow_Right	1	Natural_NoiseReduction_Low	
	Pressing Left	0.5	Arrow_Left	1	Natural_NoiseReduction_High	
Natural_PicZo	Pressing Up	0.25	Arrow_	1	Natural	

Table A.1 Continued

STATE_SRC	TRANSITION	TRANSITION PROB.	EVENT	EVENT PROB.	STATE_DEST.	DELAY
om_Sub			Up		_NoiseReduction	
	Pressing Down	0.25	Arrow_Down	1	Natural_Reset	
	Pressing Back	0.1	Return	1	Picture	
	Pressing Right	0.2	Arrow_Right	1	Natrual_PicZoom_14:9	
	Pressing Left	0.2	Arrow_Left	1	Natural_PicZoom_16:9	
Natural_PicZoom_14:9	Pressing Right	0.5	Arrow_Right	1	Natural_PicZoom_14:9_Zoom	
	Pressing Left	0.5	Arrow_Left	1	Natural_PicZoom_Sub	
Natural_PicZoom_14:9_Zoom	Pressing Right	0.5	Arrow_Right	1	Natural PicZoom_4:3	
	Pressing Left	0.5	Arrow_Left	1	Natural_PicZoom_14:9	
Natural_PicZoom_4:3	Pressing Right	0.5	Arrow_Right	1	Natural_PicZoom_Panoramic	
	Pressing Left	0.5	Arrow_Left	1	Natural_PicZoom_14:9_Zoom	
Natural_PicZoom_Panoramic	Pressing Right	0.5	Arrow_Right	1	Natural_PicZoom_Cinema	
	Pressing Left	0.5	Arrow_Left	1	Natural_PicZoom_4:3	
Natural_PicZoom_Cinema	Pressing Right	0.5	Arrow_Right	1	Natural_PicZoom_Auto	
	Pressing Left	0.5	Arrow_Left	1	Natural_PicZoom_Panoramic	
Natural_PicZoom_Auto	Pressing Right	0.5	Arrow_Right	1	Natural_PicZoom_16:9	
	Pressing Left	0.5	Arrow_Left	1	Natural_PicZoom_Cinema	
Natural_PicZoom_16:9	Pressing Right	0.5	Arrow_Right	1	Natural_PicZoom_Sub	
	Pressing Left	0.5	Arrow_Left	1	Natural_PicZoom_Auto	
Natural_Reset	Pressing Up	0.25	Arrow_Up	1	Natural_PicZoom_Sub	*
	Pressing Down	0.25	Arrow_Down	1	Picture Menu_natural	

Table A.1 Continued

STATE_SRC	TRANSITION	TRANSITION PROB.	EVENT	EVENT PROB.	STATE_DEST.	DELAY
	Pressing Back	0.1	Return	1	Picture	
	Pressing Ok	0.4	OK_Select	1	Natural_Reset	
Cinema_Contrast	Pressing Up	0.4	Arrow_Up	1	Picture Menu_cinema	
	Pressing Down	0.4	Arrow_Down	1	Cinema Brightness	
	Pressing Back	0.2	Return	1	Picture	
Cinema_Brightness	Pressing Up	0.4	Arrow_Up	1	Cinema_Contrast	
	Pressing Down	0.4	Arrow_Down	1	Cinema_Sharpness	
	Pressing Back	0.2	Return	1	Picture	
Cinema_Sharpness	Pressing Up	0.4	Arrow_Up	1	Cinema_Brightness	
	Pressing Down	0.4	Arrow_Down	1	Cinema_Colour	
	Pressing Back	0.2	Return	1	Picture	
Cinema_Colour	Pressing Up	0.4	Arrow_Up	1	Cinema Sharpness	
	Pressing Down	0.4	Arrow_Down	1	Cinema_ColourShift	
	Pressing Back	0.2	Return	1	Picture	
Cinema_ColourShift	Pressing Up	0.4	Arrow_Up	1	Cinema_Colour	
	Pressing Down	0.4	Arrow_Down	1	Cinema_Colourtemp	
	Pressing Back	0.2	Return	1	Picture	
Cinema_Colourtemp	Pressing Up	0.25	Arrow_Up	1	Cinema_ColourShift	
	Pressing Down	0.25	Arrow_Down	1	Cinema_NoiseReduction	
	Pressing Back	0.1	Return	1	Picture	
	Pressing Right	0.2	Arrow_Right	0.5	Cinema_Colourtemp_Normal	
	Pressing Left	0.2	Arrow_Left	0.5	Cinema_Colourtemp_Normal	
Cinema_Colourtemp_Normal	Pressing Right	0.5	Arrow_Right	1	Cinema_Colourtemp_Warm	
	Pressing Left	0.5	Arrow_Left	1	Cinema_Colourtemp_Cool	
Cinema_Colourtemp_Warm	Pressing Right	0.5	Arrow_Right	1	Cinema_Colourtemp_Cool	

Table A.1 Continued

STATE_SRC	TRANSITION	TRANSITION PROB.	EVENT	EVENT PROB.	STATE_DEST.	DELAY
	Pressing Left	0.5	Arrow_Left	1	Cinema_Colourtemp_Normal	
Cinema_Colourtemp_Cool	Pressing Right	0.5	Arrow_Right	1	Cinema_Colourtemp_Normal	
	Pressing Left	0.5	Arrow_Left	1	Cinema_Colourtemp_Warm	
Cinema_Noise Reduction	Pressing Up	0.25	Arrow_Up	1	Cinema_Colourtemp	
	Pressing Down	0.25	Arrow_Down	1	Cinema_PicZoom_Sub	
	Pressing Back	0.1	Return	1	Picture	
	Pressing Right	0.2	Arrow_Right	0.5	Cinema_NoiseReduction_Low	
	Pressing Left	0.2	Arrow_Left	0.5	Cinema_NoiseReduction_Low	
Cinema_Noise Reduction_Low	Pressing Right	0.5	Arrow_Right	1	CinemaNoiseReduction_Medium	
	Pressing Left	0.5	Arrow_Left	1	Cinema_NoiseReduction_Off	
Cinema_Noise Reduction_Medium	Pressing Right	0.5	Arrow_Right	1	Cinema_NoiseReduction_High	
	Pressing Left	0.5	Arrow_Left	1	Cinema_NoiseReduction_Low	
Cinema_Noise Reduction_High	Pressing Right	0.5	Arrow_Right	1	Cinema_NoiseReduction_Off	
	Pressing Left	0.5	Arrow_Left	1	Cinema_NoiseReduction_Medium	
Cinema_Noise Reduction_Off	Pressing Right	0.5	Arrow_Right	1	Cinema_NoiseReduction_Low	
	Pressing Left	0.5	Arrow_Left	1	Cinema_NoiseReduction_High	
Cinema_PicZoom_Sub	Pressing Up	0.25	Arrow_Up	1	Cinema_NoiseReduction	
	Pressing Down	0.25	Arrow_Down	1	Cinema_Reset	
	Pressing Back	0.1	Return	1	Picture	
	Pressing Right	0.2	Arrow_Right	1	Cinema_PicZoom_	

Table A.1 Continued

STATE_SRC	TRANSITION	TRANSITION PROB.	EVENT	EVENT PROB.	STATE_DEST.	DELAY
					14:9	
	Pressing Left	0.2	Arrow_Left	1	Cinema_PicZoom_16:9	
Cinema_PicZoom_14:9	Pressing Right	0.5	Arrow_Right	1	Cinema_PicZoom_14:9_Zoom	
	Pressing Left	0.5	Arrow_Left	1	Cinema_PicZoom_Sub	
Cinema_PicZoom_14:9_Zoom	Pressing Right	0.5	Arrow_Right	1	Cinema_PicZoom_4:3	
	Pressing Left	0.5	Arrow_Left	1	Cinema_PicZoom_14:9	
Cinema_PicZoom_4:3	Pressing Right	0.5	Arrow_Right	1	Cinema_PicZoom_Panoramic	
	Pressing Left	0.5	Arrow_Left	1	Cinema_PicZoom_14:9_Zoom	
Cinema_PicZoom_Panoramic	Pressing Right	0.5	Arrow_Right	1	Cinema_PicZoom_Cinema	
	Pressing Left	0.5	Arrow_Left	1	Cinema_PicZoom_4:3	
Cinema_PicZoom_Cinema	Pressing Right	0.5	Arrow_Right	1	Cinema_PicZoom_Auto	
	Pressing Left	0.5	Arrow_Left	1	Cinema_PicZoom_Panoramic	
Cinema_PicZoom_Auto	Pressing Right	0.5	Arrow_Right	1	Cinema PicZoom_16:9	
	Pressing Left	0.5	Arrow_Left	1	Cinema_PicZoom_Cinema	
Cinema_PicZoom_16:9	Pressing Right	0.5	Arrow_Right	1	Cinema_PicZoom_Sub	
	Pressing Left	0.5	Arrow_Left	1	Cinema_PicZoom_Auto	
Cinema_Reset	Pressing Up	0.25	Arrow_Up	1	Cinema_PicZoom_Sub	
	Pressing Down	0.25	Arrow_Down	1	Picture Menu_cinema	
	Pressing Back	0.1	Return	1	Picture	
	Pressing Ok	0.4	OK_Select	1	Cinema_Reset	
Game_Colour Shift	Pressing Up	0.4	Arrow_Up	1	Picture Menu_game	

Table A.1 Continued

STATE_SRC	TRANSITION	TRANSITION PROB.	EVENT	EVENT PROB.	STATE_DEST.	DELAY
	Pressing Down	0.4	Arrow_Down	1	Game_NoiseReduction_Low	
	Pressing Back	0.2	Return	1	Picture	
Game_NoiseReduction	Pressing Up	0.25	Arrow_Up	1	Game_ColourShift	
	Pressing Down	0.25	Arrow_Down	1	Game_PicZoom_Sub	
	Pressing Back	0.1	Return	1	Picture	
	Pressing Right	0.2	Arrow_Right	1	Game_NoiseReduction_Low	
	Pressing Left	0.2	Arrow_Left	1	Game_NoiseReduction_Low	
Game_NoiseReduction_Low	Pressing Right	0.5	Arrow_Right	1	Game_NoiseReduction_Medium	
	Pressing Left	0.5	Arrow_Left	1	Game_NoiseReduction_Off	
Game_NoiseReduction_Medium	Pressing Right	0.5	Arrow_Right	1	Game_NoiseReduction_High	
	Pressing Left	0.5	Arrow_Left	1	Game_NoiseReduction_Low	
Game_NoiseReduction_High	Pressing Right	0.5	Arrow_Right	1	Game_NoiseReduction_Off	
	Pressing Left	0.5	Arrow_Left	1	Game_NoiseReduction_Medium	
Game_NoiseReduction_Off	Pressing Right	0.5	Arrow_Right	1	Game_NoiseReduction_Low	
	Pressing Left	0.5	Arrow_Left	1	Game_NoiseReduction_High	
Game_PicZoom_Sub	Pressing Up	0.25	Arrow_Up	1	Game_NoiseReduction	
	Pressing Down	0.25	Arrow_Down	1	Picture menu_game	
	Pressing Back	0.1	Return	1	Picture	
	Pressing Right	0.2	Arrow_Right	1	Game_PicZoom_14:9	
	Pressing Left	0.2	Arrow_Left	1	Game_PicZoom_16:9	
Game_PicZoom_14:9	Pressing Right	0.5	Arrow_Right	1	Game_PicZoom_14:9_Zoom	

Table A.1 Continued

STATE_SRC	TRANSITION	TRANSITION PROB.	EVENT	EVENT PROB.	STATE_DEST.	DELAY
	Pressing Left	0.5	Arrow_Left	1	Game_PicZoom_Sub	
Game_PicZoom_14:9_Zoom	Pressing Right	0.5	Arrow_Right	1	Game_PicZoom_4:3	
	Pressing Left	0.5	Arrow_Left	1	Game_PicZoom_14:9	
Game_PicZoom_4:3	Pressing Right	0.5	Arrow_Right	1	Game_PicZoom_Panoramic	
	Pressing Left	0.5	Arrow_Left	1	Game_PicZoom_14:9_Zoom	
Game_PicZoom_Panoramic	Pressing Right	0.5	Arrow_Right	1	Game_PicZoom_Cinema	
	Pressing Left	0.5	Arrow_Left	1	Game_PicZoom_4:3	
Game_PicZoom_Cinema	Pressing Right	0.5	Arrow_Right	1	Game_PicZoom_Auto	
	Pressing Left	0.5	Arrow_Left	1	Game_PicZoom_Panoramic	
Game_PicZoom_Auto	Pressing Right	0.5	Arrow_Right	1	Game_PicZoom_16:9	
	Pressing Left	0.5	Arrow_Left	1	Game_PicZoom_Cinema	
Game_PicZoom_16:9	Pressing Right	0.5	Arrow_Right	1	Game_PicZoom_Sub	
	Pressing Left	0.5	Arrow_Left	1	Game_PicZoom_Auto	
SoundMenu_vol	Pressing Up	0.4	Arrow_Up	1	Digital Out	
	Pressing Down	0.4	Arrow_Down	1	Equalizer	
	Pressing Back	0.2	Return	1	Sound	
Equalizer	Pressing Up	0.25	Arrow_Up	1	Sound Menu_vol	
	Pressing Down	0.25	Arrow_Down	1	Balance	
	Pressing Back	0.1	Return	1	Sound	
	Pressing OK	0.4	OK_Select	1	EQ_User	
EQ_User	Pressing Right	0.4	Arrow_Right	1	EQ_Music	
	Pressing Left	0.4	Arrow_Left	1	EQ_Classic	
	Pressing Back	0.2	Return	1	hangisinin üzerinde	*

Table A.1 Continued

STATE_SRC	TRANSITION	TRANSITION PROB.	EVENT	EVENT PROB.	STATE_DEST.	DELAY
					return'e bastıysa	
EQ_Music	Pressing Right	0.4	Arrow_Right	1	EQ_Movie	
	Pressing Left	0.4	Arrow_Left	1	EQ_User	
	Pressing Back	0.2	Return	1	hangisinin üzerinde return'e bastıysa	
EQ_Movie	Pressing Right	0.4	Arrow_Right	1	EQ_Speech	
	Pressing Left	0.4	Arrow_Left	1	EQ_Music	
	Pressing Back	0.2	Return	1	hangisinin üzerinde return'e bastıysa	
EQ_Speech	Pressing Right	0.4	Arrow_Right	1	EQ_Flat	
	Pressing Left	0.4	Arrow_Left	1	EQ_Movie	
	Pressing Back	0.2	Return	1	hangisinin üzerinde return'e bastıysa	
EQ_Flat	Pressing Right	0.4	Arrow_Right	1	EQ_Classic	
	Pressing Left	0.4	Arrow_Left	1	EQ_Speech	
	Pressing Back	0.2	Return	1	hangisinin üzerinde return'e bastıysa	
EQ_Classic	Pressing Right	0.4	Arrow_Right	1	EQ_User	
	Pressing Left	0.4	Arrow_Left	1	EQ_Flat	
	Pressing Back	0.2	Return	1	hangisinin üzerinde return'e bastıysa	
Balance	Pressing Up	0.4	Arrow_Up	1	Equalizer	
	Pressing Down	0.4	Arrow_Down	1	Headphone	
	Pressing Back	0.2	Return	1	Sound	
Headphone	Pressing Up	0.4	Arrow_Up	1	Balance	
	Pressing Down	0.4	Arrow_Down	1	AVL	*
	Pressing Back	0.2	Return	1	Sound	
AVL_on	Pressing	0.3	Arrow_R	0.5	AVL_o	

Table A.1 Continued

STATE_SRC	TRANSITION	TRANSITION PROB.	EVENT	EVENT PROB.	STATE_DEST.	DELAY
	Right		ight		ff	
	Pressing Left	0.3	Arrow_Left	0.5	AVL_off	
	Pressing Up	0.15	Arrow_Up	1	Headphone	
	Pressing Down	0.15	Arrow_Down	1	Dynamic Bass	
	Pressing Back	0.1	Return	1	Sound	
AVL_off	Pressing Right	0.3	Arrow_Right	0.5	AVL_on	
	Pressing Left	0.3	Arrow_Left	0.5	AVL_on	
	Pressing Up	0.15	Arrow_Up	1	Headphone	
	Pressing Down	0.15	Arrow_Down	1	Dynamic Bass	*
	Pressing Back	0.1	Return	1	Sound	
Dynamic Bass_on	Pressing Right	0.3	Arrow_Right	0.5	Dynamic Bass _off	
	Pressing Left	0.3	Arrow_Left	0.5	Dynamic Bass _off	
	Pressing Up	0.15	Arrow_Up	1	AVL	
	Pressing Down	0.15	Arrow_Down	1	Surround Sound	
	Pressing Back	0.1	Return	1	Sound	
Dynamic Bass_off	Pressing Right	0.3	Arrow_Right	0.5	Dynamic Bass_on	
	Pressing Left	0.3	Arrow_Left	0.5	Dynamic Bass_on	
	Pressing Up	0.15	Arrow_Up	1	AVL	
	Pressing Down	0.15	Arrow_Down	1	Surround Sound	
	Pressing Back	0.1	Return	1	Sound	
Surround Sound_on	Pressing Right	0.3	Arrow_Right	0.5	Surround sound_off	
	Pressing Left	0.3	Arrow_Left	0.5	Surround sound_off	
	Pressing Up	0.15	Arrow_Up	1	Dynamic Bass	
	Pressing Down	0.15	Arrow_Down	1	Digital Out	
	Pressing Back	0.1	Return	1	Sound	
Surround sound_off	Pressing Right	0.3	Arrow_Right	0.5	Surround Sound_on	
	Pressing Left	0.3	Arrow_Left	0.5	Surround Sound_on	
	Pressing Up	0.15	Arrow_Up	1	Dynamic Bass	
	Pressing Down	0.15	Arrow_Down	1	Digital Out	*
	Pressing Back	0.1	Return	1	Sound	

Table A.1 Continued

STATE_SRC	TRANSITION	TRANSITION PROB.	EVENT	EVENT PROB.	STATE_DEST.	DELAY
Digital Out_PCM	Pressing Right	0.3	Arrow_Right	0.5	Digital Out_Compressed	
	Pressing Left	0.3	Arrow_Left	0.5	Digital Out_Compressed	
	Pressing Up	0.15	Arrow_Up	1	Surround Sound	
	Pressing Down	0.15	Arrow_Down	1	Sound Menu_vol	
	Pressing Back	0.1	Return	1	Sound	
Digital Out_Compressed	Pressing Right	0.3	Arrow_Right	0.5	Digital Out_PCM	
	Pressing Left	0.3	Arrow_Left	0.5	Digital Out_PCM	
	Pressing Up	0.15	Arrow_Up	1	Surround Sound	
	Pressing Down	0.15	Arrow_Down	1	Sound Menu_vol	
	Pressing Back	0.1	Return	1	Sound	