DOKUZ EYLÜL UNIVERSITY
GRADUATE SCHOOL OF NATURAL AND APPLIED SCIENCES

SINGLE PHASE INVERTER DESIGN FOR LCD TV

by
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March, 2007
İZMİR

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M.Sc THESIS EXAMINATION RESULT FORM

We have read the thesis entitled **"SINGLE PHASE INVERTER DESIGN FOR LCD TV"** completed by **İsmail YILMAZLAR** under supervision of **Prof. Dr Eyüp AKPINAR** and we certify that in our opinion it is fully adequate, in scope and in quality, as a thesis for the degree of Master of Science.

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İsmail YILMAZLAR

SINGLE PHASE INVERTER DESIGN FOR LCD TV

ABSTRACT

This thesis discusses a new, CCFL (cold cathode fluorescent lamp) inverter for LCD (Liquid Crystal Display) TVs. LCDs need backlight illumination so they are generally using CCFLs as a backlight unit. To drive this unit, system needs inverter, because the CCFLs are supplied from high voltage high frequency ac signal. Several inverter topologies are exist but new approach for this drive unit by using parallel resonant inverter topology without a transformer will be introduced. This new approach will reduce overall system size. Also the total power demand is changing for LCD TVs, because backlight unit generally consumes %40 of input power. The previous inverter is supplied from SMPS but this inverter is supplied from regulated output of rectifier. In this thesis a parallel resonant inverter is used. There are different resonant inverter topologies like as series inverter, parallel resonant inverter and series parallel resonant inverter circuits. The voltage transfer function of this inverter will be examined and compared. THD of output voltage of these inverters are analyzed. 15'' panel is chosen for application, lamp model is defined and whole circuit is performed. By using the component values estimated simulation is carried out in PSPICE package program. The simulation results are compared with the experimental results in this thesis.

Keywords: CCFL inverter, backlight inverter, LCD TV, Cold Cathode fluorescent lamp.

LCD TELEVİZYONLAR İÇİN TEK FAZLI İNVERTER TASARIMI

ÖZ

LCD televizyonların görüntü verebilmesi için arka ışık aydınlatılması yapılmalı. Bu aydınlatma işlemi genel olarak CCFL denen floresan lambalar ile yapılmaktadır. Bu lambaların düzgün aydılatılma yapılabilmesi için, yüksek voltaj ve yüksek frekansa sahip bir alternatif akım ile sürülmesi gerekir. Gerekli olan bu işareti lambaya uygulayabilmek için çevirgeç kullanımına ihtiyaç duyulmuştur ve değişik çevirgeçler tasarlanmıştır. Bu tezde de yeni bir çevirgeç tasarımı üzerine çalışılmıştır. Bu çevirgeç in daha önceden kullanılan çevirgeçlere göre bir takım avantajları vardır basit olarak bu çevirgecin diğer çevirgeçlerden temel farkı giriş voltajında, diğer çevirgeçlerde olduğu gibi düşük voltajlı doğru akım yerine yüksek voltajlı doğru akım kullanılmasıdır. Bu sayede lambaları sürmek için herhangi bir trafoya ihtiyaç duyulmamaktadır. Ayrıca herhangi bir LCD televizyonda gerekli olan güç gereksiminin yaklaşık olarak %40 lık kısmı bu lambaları sürmek için harcanmaktadır ve güç gereksimi için gerekli olan tüm enerji anahtarlamalı güç kaynağı üzerinden aktarılmaktadır. Fakat bu yeni tasarımda artık inverter için gerekli olan besleme anahtarlamalı güç kaynağından alınmadığı için anahtarlamalı güç kaynağı üzerindeki enerji dönüşüm miktarı azaltılmaktadır. Bu tezde gerekli olan çevirgeç parallel rezonans çevirgeç devresi ile yapılmıştır. Seri rezonans, parallel rezonans ve seri paralel rezonans devreleri üzerine çalışmalar yapılmış voltaj transfer fonksiyonları çıkarılmıştır. Bu üç değişik inverter ın toplam harmonik bozulma seviyeleri incelenmiştir. Uygulama için 15'' bir panel seçilmiş ve devre gerçekleştirilmiştir. Gerçekleştirilen devrenin simulasyonu PSPICE adlı program yardımı ile yapılmıştır. Simulasyon ve deney sonuçları bu tezde karşılaştırılmıştır.

Anahtar sözcükler :Soğuk katot floresan lamba çevirgeci, arka ışık çevirgeci, LCD TV, Soğuk katot flerosan lamba

CONTENTS

CHAPTER ONE
INTRODCUTION

LCD panels are very good solution for portable devices because they are very thin, consumes low power during operation and can be supplied from low voltage. For example most of the cellular phones, portable DVD players and laptops are using LCD panels. Also nowadays LCD panels are becoming very popular for LCD TVs because it has the significant advantages over CRT (Cathode Ray Tube) TVs. (incorporated, 2006)

One of the biggest advantages of LCD TV is that they are compact, lightweight and space-efficient (only 15-20% of volume of CRT). A LCD TV has a very thin screen as opposed to the bulky tube of a CRT monitor. This means that they can be used in many places where a larger CRT TV can not fit. LCD TVs picture is smooth and colorful. LCDs have none of those annoying scan lines that conventional sets do. This owes to the fact that each sub pixel has its own transistor electrode, which creates smooth, evenly lit images across the entire surface of the display. LCD TV is multi-functional and long-lived. They are capable of displaying HDTV, regular TV, and home video. It's also a computer monitor. In fact, it can accept any video format. CRT monitors are known to emit harmful radiation, whereas LCD monitors do not. LCD TVs are significantly brighter and have higher contrasts than traditional CRT sets. Which means that a LCD TVs will perform exceedingly well under most ambient light conditions

LCD panels are transmissive displays so it needs backlight illumination. The cold cathode fluorescent lamps (CCFL's) are commonly used to provide this backlight illumination. The CCFLs have following advantages.

- Small size
- High efficiency
- Long life

CCFLs are gas discharge device and operating with sinusoidal voltage. The voltage rating is generally between 400Vrms-800Vrms and it's frequency is in the

range of 30 KHz to 70 KHz. In order to start ionization, the voltage more than 1000Vrms should be applied. This voltage range at this frequency can be obtained by using inverter. Different inverter topologies are avaliable in literature. The requirements of the CCFL for a proper usage bring the limitation on the selection of inverter requirements.

The inverter must provide the voltage up to 2000V (dependent to the lamp type) peak ignition voltage for CCFL (Redl & Arakawa, 1997). This level is also important to start ionization for the lamp which affects lifetime of lamp. In this application CCFL inverter input voltage is equal to 390V which is the output of active power factor correction circuit.

The other important parameter on the selection is the efficiency because the cost of the energy is high and energy efficient devices are more popular in market. To ensure high efficiency and small interference, a low-distortion sine-wave drive is needed at the output. (Redl & Arakawa, 1997) This inverter will be used in TV set, where the audio and video signals are at low voltage level carried. This means that the interferences from inverter can be seen at the screen and can be audible from speaker.

DC voltage across the lamp is not allowed because it will lead to uneven light emission, due to redistribution of the mercury ions inside the tube. Capacitive ballasting is not acceptable if there is even-harmonic distortion in the drive waveform, because that, together with the asymmetrical nonlinearity of the lamp characteristic, will lead to dc voltage across the lamp. In many applications the inverter must be able to provide dimming to the lamp. (Redl & Arakawa, 1997)

The nominal operating voltage of the CCFL is in the several-hundred-volt range. CCFLs, like all gas discharge lamps, are very nonlinear. Additionally the lamps show negative resistance at low frequency. The inverter must provide proper ballasting for the lamp to prevent failure or system instabilities. (Redl & Arakawa, 1997)

As CCFL is a gas discharge device and its mathematical model is nonlinear. The CCFL shows different characteristic at different dimming (voltage) level. Its impedance is changing with respect to applied voltage and applied frequency. The volt-ampare characteristic of a CCFL lamp is given Figure 1.1.

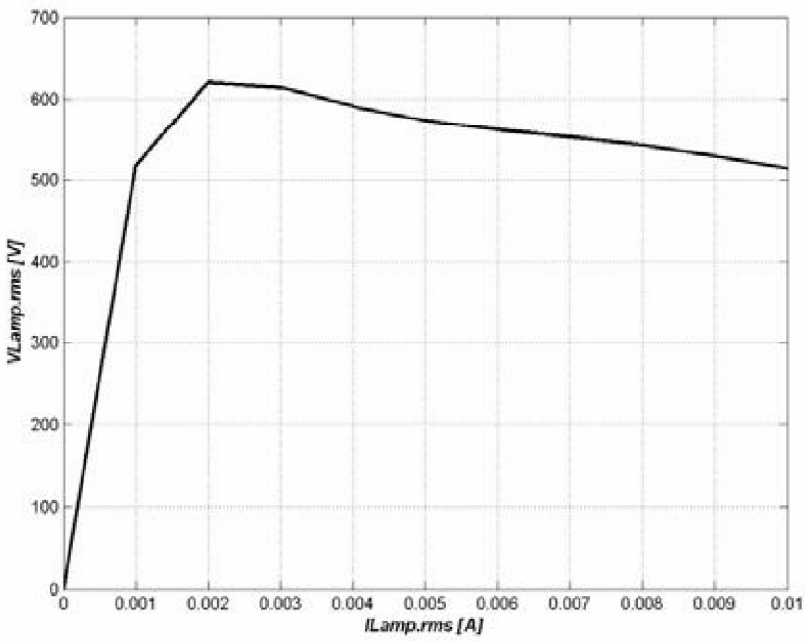

Figure 1.1 A sample CCFL characteristic

This characteristic shows positive impedance if the current is less than 2 mA. The negative impedance appears over this current level. To express these two different dimming characteristics of the lamp, the following equations can be used (Kim, et all., 2005)

$$Vrms = A0 + A1 \cdot e^{(-A2 \cdot Irms)} - A3 \cdot e^{(-A4 \cdot Irms)} \tag{1-1}$$

Where A0, A1, A2, A3 and A4 are constants.

For high frequency operating point.

$$Rlamp = \frac{Vrms}{Irms} \tag{1-2}$$

So

$$Rlamp = \frac{A0 + A1 \cdot e^{(-A2 \cdot Irms)} - A3 \cdot e^{(-A4 \cdot Irms)}}{Irms} \tag{1-3}$$

And

$$V(t) = Rlamp \cdot I(t) \tag{1-4}$$

So

$$V(t) = \left[\frac{A0 + A1 \cdot e^{(-A2 \cdot Irms)} - A3 \cdot e^{(-A4 \cdot Irms)}}{Irms} \right] \cdot I(t) \tag{1-5}$$

This equation gives us instantaneous voltage variation on the lamp.

The operating point will be chosen at where a frequency and voltage level are predefined. For this operating point a single resistance model will be used. An inverter must supply this voltage at the predefined frequency, otherwise the model with single resistance can fail. Also during preheat mode lamp is assumed as a open circuit because at this mode ionization is not started.

To block diagram of the power flow in LCD TVs is shown in Figure 1.2.

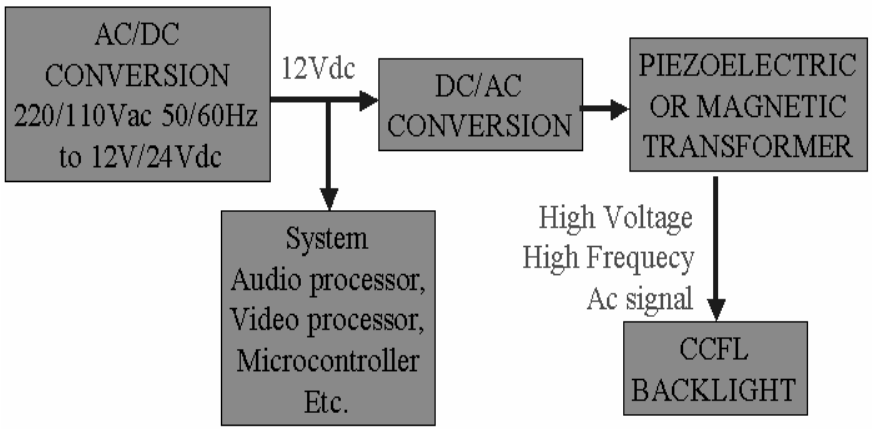

Figure 1.2 General power flowing block diagram of LCD TVs.

As it can be clearly observed the power requirements of inverter is supplied by the SMPS. At LCD TVs the CCFL lamps consumes approximately %40 of input power.

The AC/DC converter (SMPS) must be designed not only for the main board but also designed for the inverter by taking the efficiency into account. This type of power management is chosen because formerly LCD displays are designed for portable devices and these portable devices are supplied from battery because of that inverters are designed for low voltage supply (generally 12 to 24V). The LCD TV manufacturers are using this implementation of inverter with low input voltage. However, in this type of structure, the inverters must be designed with step-up transformers. These transformers are power dissipating device and cost inefficient solution.

The LCD TVs are supplied from the power system in domestic use so another approach can be used as being shown in Figure 1.3.

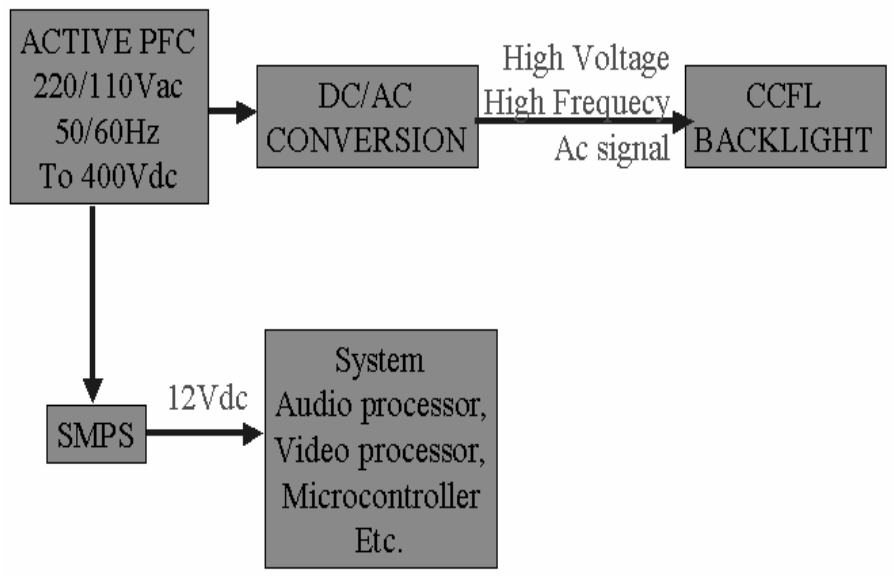

Figure 1.3 Proposed power flowing of LCD TVs.

At this type of design, the inverter is supplied from the rectifier output controlled with PFC. The SMPS is dedicated only for the system. The system means main board; which is composed video decoder, audio decoder, microcontroller etc. And at the inverter input, which is connected to output of active pfc at 400V dc. The output of the inverter can be connected to the lamp without transformers, if a parallel resonant type of inverter is selected.

Also, with this approach the power rating of the SMPS is reduce so the SMPS cost will be decreased.

Also it is obvious that the SMPS consumes some amount of power during power conversion. Therefore the power loss in the SMPS will decrease by this approach.

CHAPTER TWO
PRESENT INVERTER TOPOLOGIES.

There are several inverter topologies for CCFL drive. In this chapter, these techniques will be reviewed. And all of these topologies have a transformer and low input voltage as easily seen from schematics. Therefore, these inverters can be implemented by selecting proper turns ratio of the transformers.

2.1 Current Feed Push Pull Inverter

The current feed push pull inverter topology is the most popular inverter type for the ccfl driver. Generally LCD TV manufacturers use this topology.

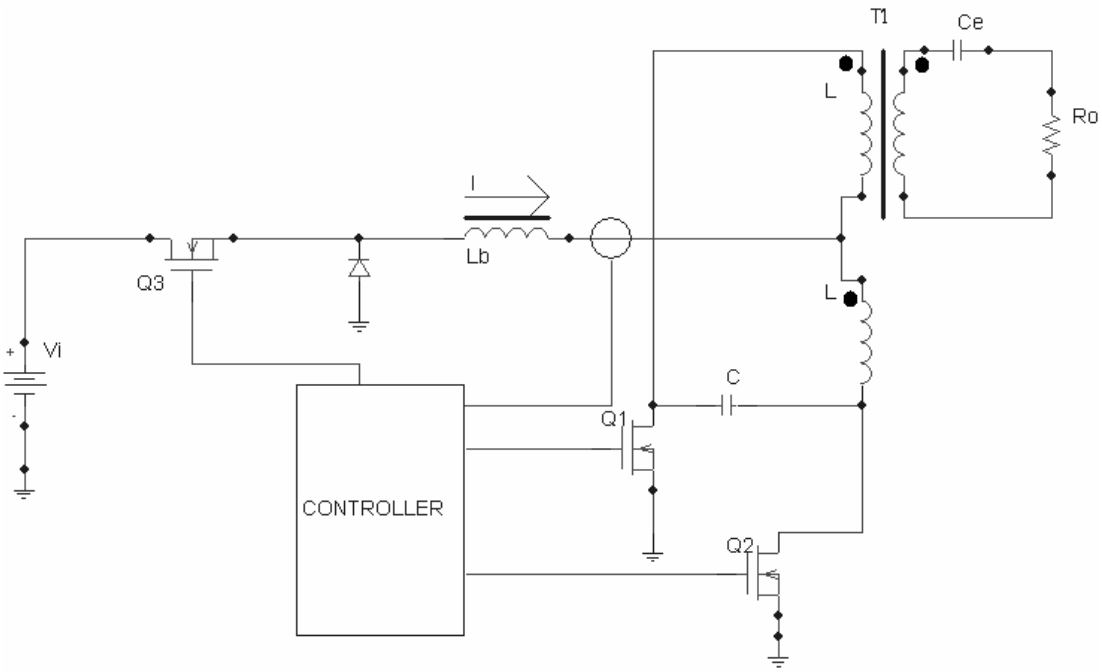

Figure 2.1 Current feed push pull inverter topology

Typical schematic of the current feed push pull inverter is given at figure 2.1.This design have a two stage control. The Current-Fed Buck converter controlled by Q3, with a large inductor Lb provides a nearly constant current to the push pull inverter. Switching devices Q1 and Q2 are driven at %50 duty cycle alternatively (Lin & Witulski, 1996)

But at this design, the most critical device is the transformer because amplifying and resonance is done by the transformer. Designers should have a very good talent for transformer design.

The present day inverter topologies are based on a modified power oscillator driven by a buck or boost switching regulator. The buck or boost switching stage preregulates the power that is applied to the oscillator section (Nalbant & Garden, 1995).

The electrical efficiency (and as a result light output efficiency) in such a system is the product of the two individual efficiencies of the two power processing stages. Even if individual efficiencies are 92% the resulting total efficiency would only be 85 % (Nalbant & Garden, 1995) and this value may be low for this application.

In a ROYER oscillator the primary winding inductance is of relatively low value and is used as part of the resonant network, necessitating the insertion of a gap in the core structure of the transformer. The lower inductance causes circulating currents that increase the copper losses of the winding. Also the gap in the core results in fringe fields that produce eddy current losses in surrounding conductive areas resulting in more losses. (Nalbant & Garden, 1995)

Also in this design lamp voltage and current is not purely sinusoidal because the transformer's leakage inductance is not absorbed into the load network, and the ripple current flowing into the inverter section. So this reduces overall efficiency. The other disadvantage of this design is high cost due to complex circuit topology and expensive control IC. (Nalbant & Garden, 1995)

2.2 Current Synchronous Zero Voltage Switching (CS-ZVS) Topology

Figure 2.2, shows the basic schematic diagram of the CS-ZVS inverter topology. The key elements in the circuit are the lamp impedance matching network components. They perform the impedance matching and operating point stabilization functions for the CCFLs. The circuit is operated above resonance and that enables

zero voltage switching which results in lowered EMI and switching losses. (Nalbant, et all., 1995)

At initial start-up the synchronous detector circuitry integrated in the LXl580 IC senses the resonant current that flows through R1 and it synchronizes the operating frequency of Q 1 and Q2 to match the resonant frequency of the impedance matching network. This enables the rapid build-up of voltage necessary for lamp ignition. After ignition the loaded lamp impedance matching network current is sensed and again the synchronous detector circuitry forces the switching frequency of Q1 and Q2 to settle at the maximum brightness point (Nalbant, et all., 1995)

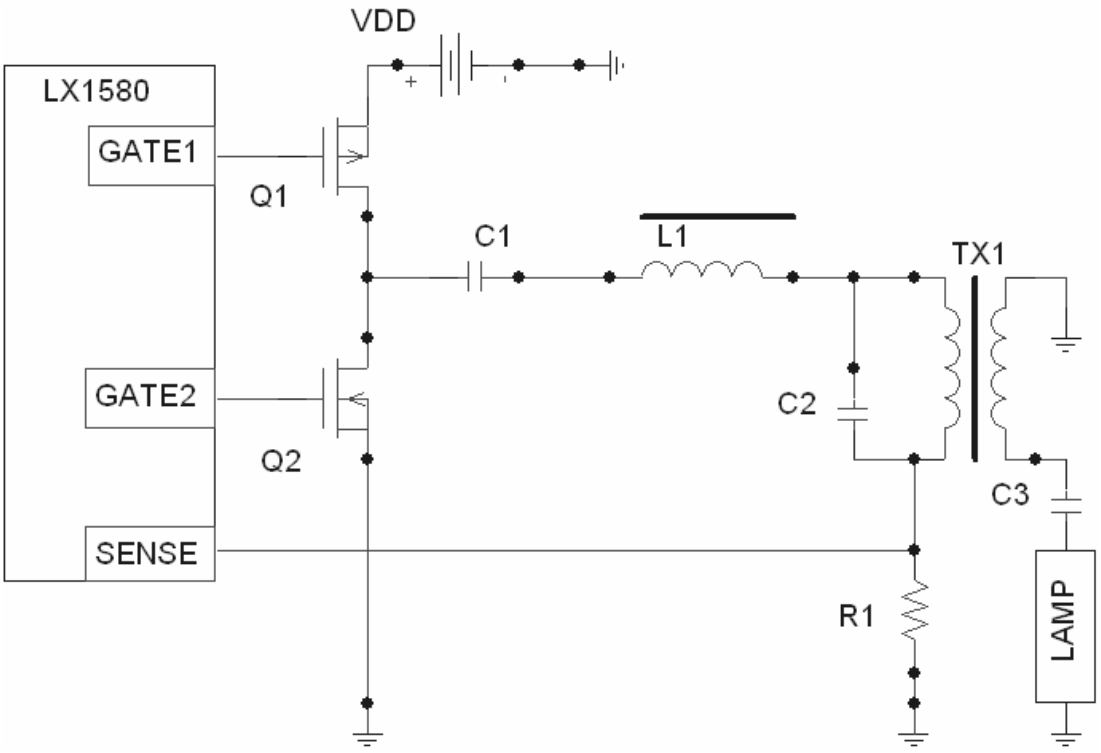

Figure 2.2 Current Synchronous Zero Voltage Switching (CS-ZVS) topology

The circuit is more efficient than the current synchronous parallel resonant and buck-preregulator combination, but it has also a rather complex topology, with two controlled switches, two magnetic, and three capacitors in the power train. (Redl & Arakawa, 1997)

Other drawbacks of the circuit are; the leakage inductance of the transformer is not absorbed in the load network, leading to significant lamp voltage distortion and reduced efficiency, the topology is claimed to be proprietary, and can be used only with an expensive single-source dedicated control IC, When used with the dedicated control IC, the inverter requires complementary (n-channel and p-channel) MOSFETs; alternatively it would require a floating drive. (Redl & Arakawa, 1997)

2.3 Class L Inverter

An other topology is the class L inverter topology. Circuit diagram of this inverter is given figure 2.3.

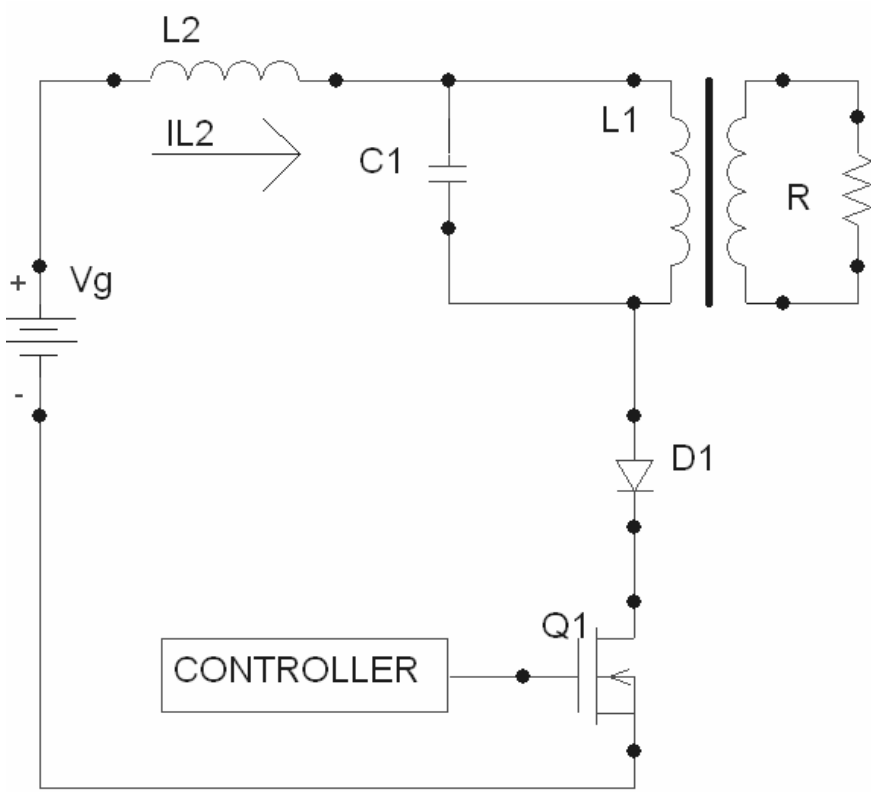

Figure 2.3 Class L inverter topology

The Class-L inverter is comprised a single controlled switch and an external LC network connected in such a way that the switching of large current and large voltage do not occur simultaneously. The external network, also shown in Fig. 2.3, consists of an inductor L2 and a parallel resonant tank circuit L1-C1 with which the load is coupled. The resonant circuit is designed so that only the fundamental component of

the current in the switch at the switching frequency is flowing into the load. (Lin & Witulski, 1997)

The energy transferring components form a "L" shape, where of the Class-L inverter is named. For simplification of the analysis, we assume that resonant tank is a high Q parallel tuned network. The higher harmonics of the resonant voltage are negligible so that a pure sinusoidal voltage is assumed at the output. (Lin & Witulski, 1997)

2.4 LCC Inverter

In this section, an other topology called as LCC (series/parallel) resonant inverter is explained.

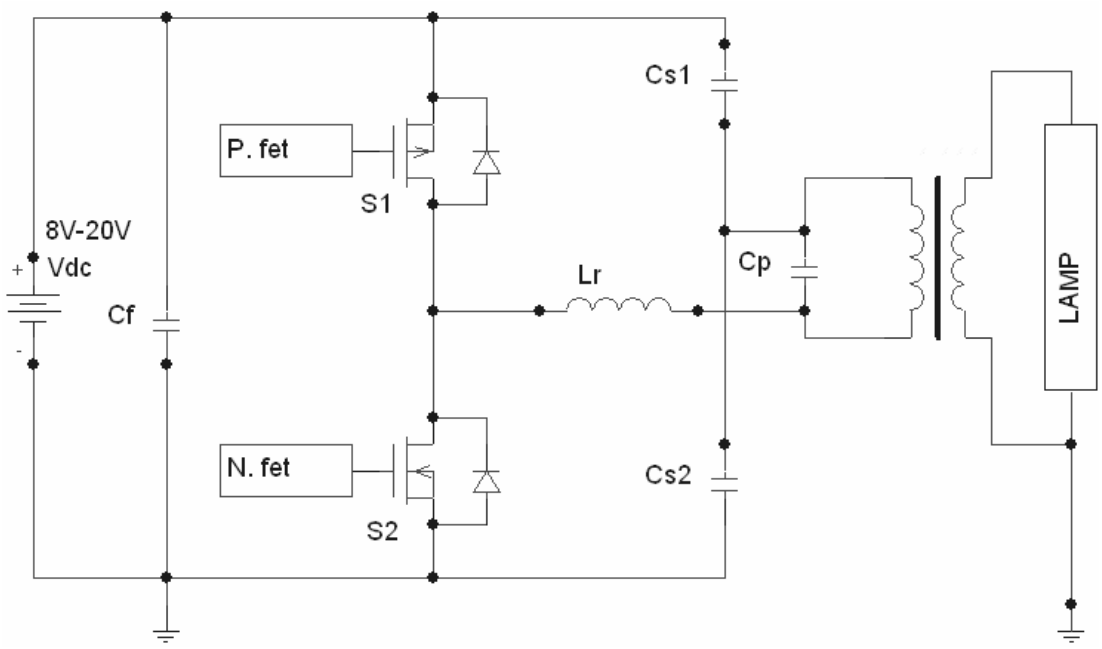

Figure 2.4 LCC (series/parallel) resonant inverter

It is a half-bridge inverter where capacitors CSl and CS2 are not only used to split the input voltage, but also used as the series resonant capacitor. The circuit employs only two switches, and these are right across the input dc rail, so they have access to the maximum available voltage. The transformer primary is in series with the resonant inductor and the series resonant capacitance. If the switching frequency is

above the series resonant frequency the load appears to be driven by a current source. Because of the current source characteristic, no separate ballast impedance is necessary and the output voltage is equal to the lamp voltage. This results in a relatively low turns ratio, and therefore, a smaller transformer is possible. Since the transformer is paralleled with the parallel resonant capacitance, under pre-ionized conditions, the circuit performs like a parallel-loaded resonant converter and the output tends to behave as a controllable voltage source. As a result of the voltage-boost characteristic of the parallel-loaded converter, the necessary ionization voltage can be generated. (Donahue & Jovanovic, 1994)

2.5 Class E Inverter Topology.

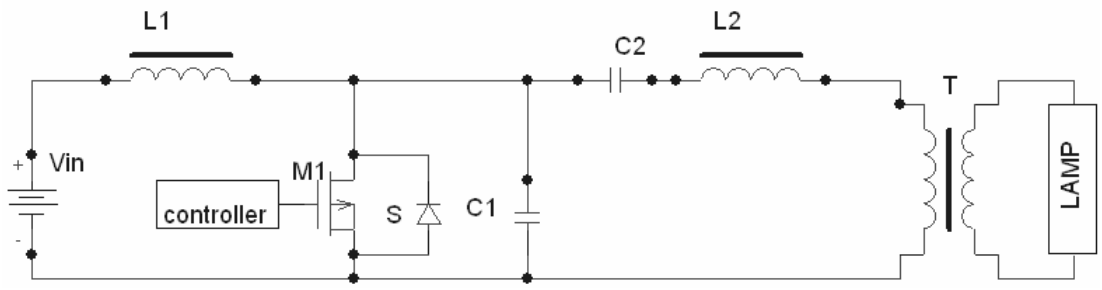

Figure 2.5 Class E inverter topology

At the Figure 2.5, the schematic of the Class E inverter is given. The detail of operating principle and analysis are given at Redl, et all, 1997. Basically this inverter has following advantages; a) Only one switch is required; that simplifies the drive circuit. b) The leakage inductance of the transformer is absorbed in the load network, leading to smooth lamp waveforms and high efficiency. c) The inverter is fed with an inductance (at least in the basic version), therefore the interference current reflected back to the source is small. d) The switch voltage waveform is smooth with a low dv/dt, so the capacitive interference is reduced (Redl & Arakawa, 1997).

But it has a slightly asymmetrical output voltage due to the inherent second-harmonic component in the output voltage of the inverter. This may cause the possible migration of mercury ions and the resulting asymmetrical light emission of the CCFL (Redl & Arakawa, 1997).

In the class E inverter, the resonant inductor L_2, is in series with the primary winding of the output transformer. This allows the absorption of the leakage inductance of the transformer in the resonant network; it also offers the possibility of integrating the resonant inductor with the transformer. The integration of two magnetic parts leads to the reduction of the overall cost (Nalbant, et all., 1995).

CHAPTER THREE
RESONANT INVERTER TOPOLOGIES

Resonant inverters connect dc system to an ac system. These inverters are widely used in practice where high frequency ac voltage is required

The DC to AC converters has some shortcomings. During turning on and turning off of the switching elements high voltage and/or high current appears across the switch and this leads power consumption during switching also this consumption is increasing with switching frequency. Because of switching the high voltage and current it is possible to see high di/dt or high dv/dt which leads EMI problems. The first stage of this converter consists switching elements in order to obtain square wave. This square wave can be effectively obtained by using full bridge configuration. The half bridge configuration can also be used as a matter of fact that a dc component appears in the output voltage waveform. This dc component can be eliminated by using dc blocking capacitor. The second stage is composed of resonant circuit having a resonant capacitor, resonant inductor and a resistor. Generally resistor denotes load connected to the output. The elements of the circuit are selected at the values such that the fundamental frequency of square wave is close to the resonant frequency. In this case, the harmonics of the square wave are eliminated at the load. This reduces the EMI problems. By changing operating frequency it is possible to obtain different voltage levels at the load. If the operating frequency is far away from resonant frequency then the unwanted harmonics can be seen in the load voltage. At the full bridge configuration, the output voltage can be controlled by changing duty ratio as well.

Mainly resonant inverters can be divided into three groups

a)Series (or voltage-source) inverters
b)Parallel (or current-source) inverters.
c)Series parallel resonant inverter.

Resonant inverters can be functionally divided into two parts: the switching part and the resonant part. A block diagram of an inverter is shown in Figure 3.1.

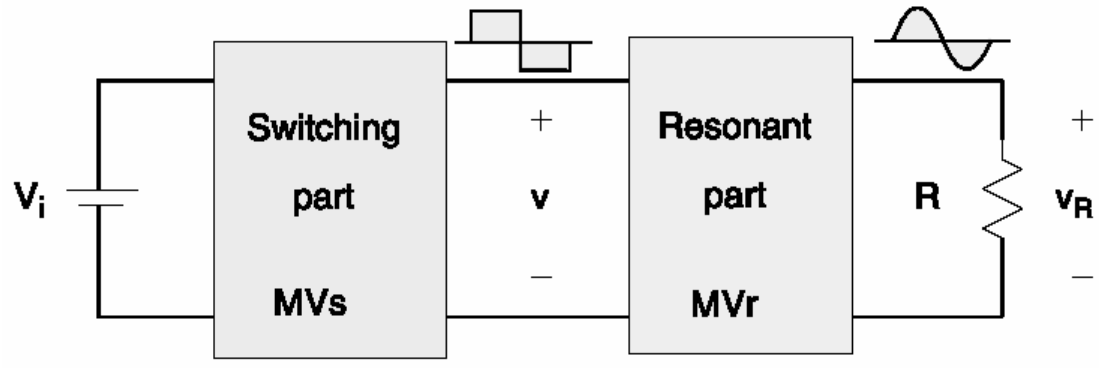

Figure 3.1 General block diagram of resonant inverters

The switching part comprises a DC input voltage source Vi and a set of switches. The switches are controlled to produce a square-wave voltage v. Since a resonant circuit forces a sinusoidal current, only the power of the fundamental component is transferred from the switching part to the resonant part. Hence, consideration of only the fundamental component of the voltage at the input to the resonant circuit yields proper power relationships. A voltage transfer function of the switching part can be defined as

$$MVs = \frac{Vrms}{Vi} \tag{3-1}$$

Where Vrms is the rms value of the fundamental component of the input voltage V to resonant part. For a half-bridge inverter,

$$MVs = \frac{\sqrt{2}}{\pi} = 0.45 \tag{3-2}$$

In a full-bridge configuration, $MV_s = 0.9$. The resonant part of an inverter converts a square-wave voltage V into sinusoidal current or voltage signal.

3.1 Series Resonant (Voltage Source) Inverters

3.1.1 Circuit and Waveforms

A circuit of the voltage-source half-bridge series-resonant inverter (SRI) is presented in Figure 3.2. It is composed of two bidirectional switches S1 and S2 and a series-resonant circuit L-C-R. Each switch consists of a transistor (power MOSFET, IGBT, or BJT) and an antiparallel diode. The switch can carries either positive or negative current. A positive or negative current can flow through the switch. If the transistor is on, then a positive current can flow through the transistor. If the transistor is OFF, then the switch can conduct only a negative current, which flows through the diode. The transistors are driven by nonoverlapping gating signals with a small dead time at the operating frequency f = 1/T. Switches S1 and S2 are alternately ON and OFF with a duty ratio of 50% or slightly less. The dead time is the time interval when both controllable devices are off. Resistance R is an AC load. (Skvarenina, 2002)

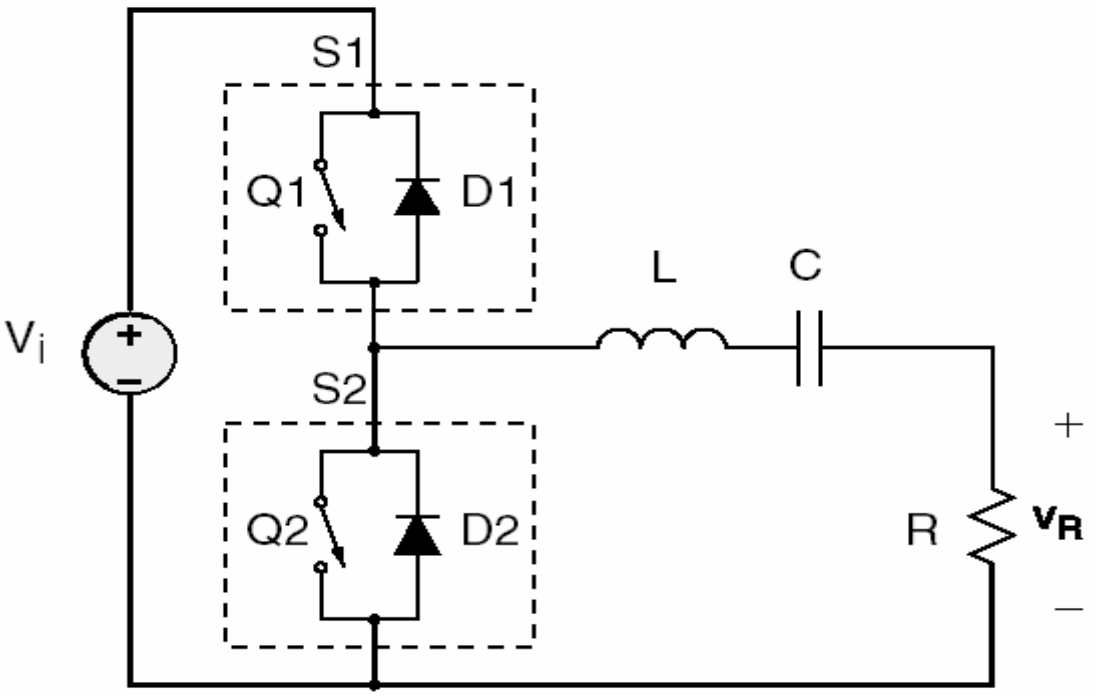

Figure 3.2 Series resonant inverter

Selected waveforms in the voltage-source resonant inverter are shown in below Figure 3.3. The voltage that feeds the series-resonant circuit is a square wave. If the quality factor of the resonant circuit is high enough, the current through the circuit is nearly a sine wave. When f = fo (fo will be examined in section 3.1.2), the controllable devices turn on and off at zero current. The antiparallel diodes do not conduct. This yields zero switching losses and high efficiency. The operating frequency f is, however, rarely equal to the resonant frequency fo because the output power or the output voltage is controlled by changing f. Figure 3.3 shows the waveforms for f < fo and f > fo, respectively. Transistors should be turned off for f < fo or turned on for f > fo during the time interval when the switch current is negative. During this time interval, the switch current can flow through the antiparallel diode. To prevent shorting of the input voltage source (or, in other words, cross conduction or a shoot-through current), the gating signals of transistors cannot overlap and, additionally, must have a sufficient dead time. MOSFETs exhibit a delay time and bipolar devices (IGBTs and BJTs) have a storage time at turn-off. If the dead time is too short, one transistor still remains on while the other turns on. Hence, both transistors may be ON at the same time, which results in short-circuiting the input voltage source by small transistor on resistances. To allow for a positive current flow through the switches, the dead time should not be too long. (Skvarenina, 2002)

For f < fo, the inductor current leads the fundamental component of the S2 voltage by a phase angle ψ.It is said that the series-resonant circuit represents a capacitive load to the switches. Therefore, the switch current is positive after switch turn-on and is negative before switch turn-off. The semiconductor devices conduct in a sequence Q1–D1–Q2–D2. The inductor current is diverted from the diode of one switch to the transistor of the other switch. Consider the turn-on of switch S2. Prior to this transition, the inductor current flows through antiparallel diode D1 of switch S1. When transistor Q2 is turned on by its gating signal, the voltage across S2 decreases, causing the voltage across S1 to increase. Therefore, diode D1 turns off and the inductor current is diverted from D1 to Q2.(Skvarenina, 2002)

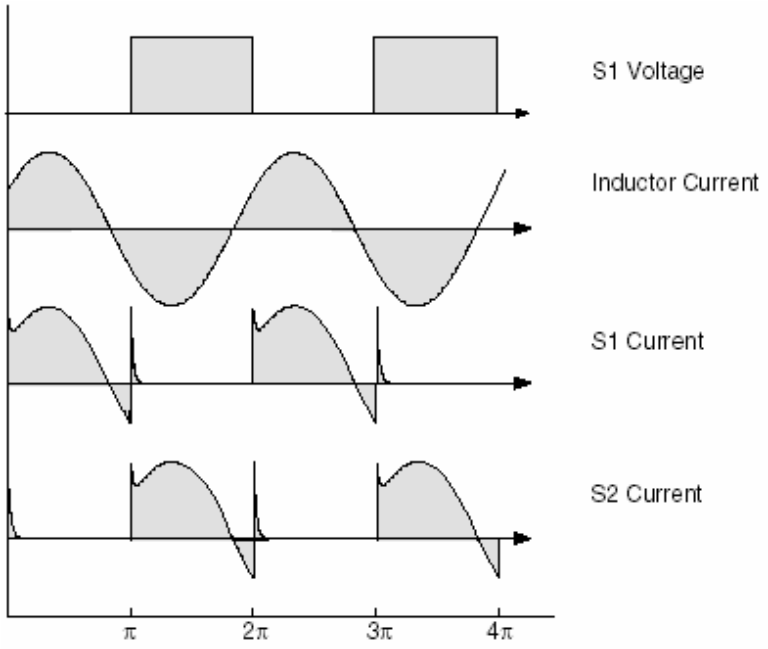

Figure 3.3 Current and voltage waveforms of series resonant inverter

For f < fo , the turn-off switching loss is zero, but the turn-on switching loss is not zero. The transistors are turned on at a high voltage, equal to the power supply voltage. When the transistor is turned on, its snubber capacitance Cs is discharged, causing a switching loss. The total power loss associated with charging and discharging the snubber capacitance is

$$P = f \cdot Cs \cdot Vi^2 \tag{3-3}$$

In summary, for f < fo , there is a turn-on switching loss in the transistor and a turn-off (reverse recovery) switching loss in the diode. The transistor turn-off and the diode turn-on are lossless. (Skvarenina, 2002)

For f > fo, the series-resonant circuit represents an inductive load to the switches. The inductor current lags behind the fundamental component of the S1 voltage by a phase angle ψ. The switch current is negative after turn-on (for part of the switch "on" interval) and positive before turn-off. The semiconductor devices conduct in a sequence D1–Q1–D2–Q2. Consider the turn-off of switch S1. When transistor Q1 is turned off by its gating signal, the voltage across it increases, causing the voltage

across the switch S2 to decrease. Eventually, D2 turns on and the inductor current is diverted from transistor Q1 to diode D2. (Skvarenina, 2002)

The transistors are turned on at almost zero voltage. There is a small negative voltage of the antiparallel diode, but this voltage is negligible comparison with the input voltage. Hence, the turn-on switching loss is eliminated (Skvarenina, 2002)

In summary, for f > for , there is a turn-off switching loss in the transistor, while turn-on of the transistor and the diode are lossless. (Skvarenina, 2002)

3.1.2 Voltage Transfer Function

The parameters of the series-resonant circuit are defined as;

a) Resonant frequency(Wo)

$$Wo = \frac{1}{\sqrt{L \cdot C}} \tag{3-4}$$

b) The characteristic impedance

$$Zo = \sqrt{\frac{L}{C}} = Wo \cdot L = \frac{1}{Wo \cdot C} \tag{3-5}$$

c) The quality factor

$$Q = \frac{Wo \cdot L}{R} = \frac{1}{Wo \cdot C \cdot R} = \frac{Zo}{R} = \frac{\sqrt{\frac{L}{C}}}{R} \tag{3-6}$$

The input impedance of the series resonant circuit is

$$Z = Z \cdot e^{i \cdot \psi} = R \cdot \left(1 + i \cdot Q \left(\frac{W}{Wo} - \frac{Wo}{W} \right) \right) \tag{3-7}$$

where $i^2=-1$

and

$$\psi = \arctan\left(Q \left(\frac{W}{Wo} - \frac{Wo}{W} \right) \right) \tag{3-8}$$

As seen from the equation of ψ for $f < fo$, ψ is negative, which means that the resonant circuit represents a capacitive load to the switching part of the inverter. For $f > fo$, ψ is positive, which indicates that the resonant circuit represents an inductive load. (Skvarenina, 2002)

Vs and Vr are the fundamental components of voltages at the input and across the load resistor respectively. Let us find Vr by

$$Vr = \left(\frac{Vs}{Z} \right) \cdot R \tag{3-9}$$

So

$$\frac{Vr}{Vs} = \frac{1}{\left[1 + i \cdot Q \cdot \left(\frac{W}{Wo} - \frac{Wo}{W} \right) \right]} \tag{3-10}$$

$$MVr = \left| \frac{Vr}{Vs} \right| \cdot e^{(-i \cdot \psi)} \tag{3-11}$$

So

$$MVr = \frac{1}{\sqrt{1 + \left[Q \cdot \left(\frac{W}{Wo} - \frac{Wo}{W} \right) \right]^2}} \tag{3-12}$$

A voltage transfer function of the entire inverter is defined as

$$MVi = \frac{Vr}{Vi} = \frac{Vr}{Vrms} \cdot \frac{Vrms}{Vi} = MVs \cdot MVr = \frac{MVs}{\sqrt{1 + \left[Q \cdot \left(\frac{W}{Wo} - \frac{Wo}{W} \right) \right]^2}} \tag{3-13}$$

Here MVs depends on switching topology (full bridge or half bridge)

To find the frequency corresponding maximum output voltage the MATLAB package program is used. The commands are given in Appendix A.

And four roots are found Wo,-Wo,iWo,-iWo. The positive real value of root is selected as proper one.

If we set W=Wo we get MVr=1 then the maximum voltage is independent from component values. In this case, the output voltage can be controlled by changing fundamental component of input voltage.

The voltage transfer function of resonant circuit as a function of frequency is given in Figure 3.4. It is clear that the maximum output voltage is obtained at resonant frequency(f=fo).

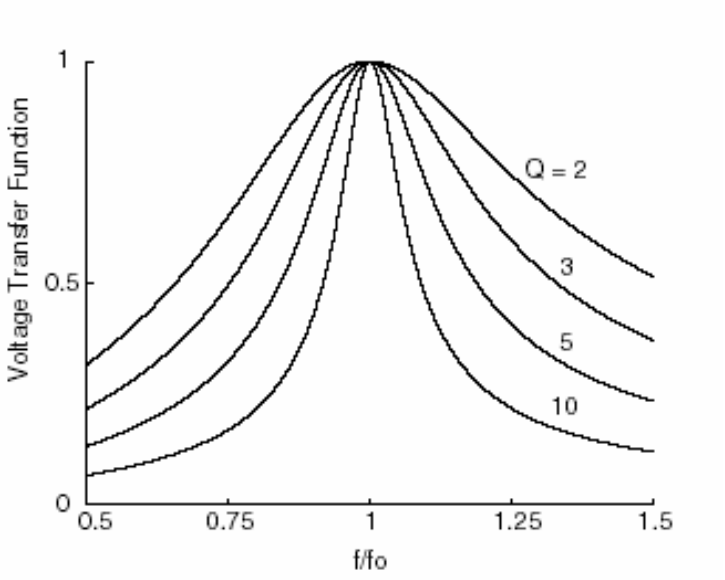

Figure 3.4 Frequency with respect to voltage gain for different quality factor of series inverter

3.2 Parallel-Resonant(Current-Source) Inverters

3.2.1 Circuit and Waveforms

In the voltage-source SRI presented in the preceding section, the load resistance is connected in series with the LC components. When the load resistance is increased, the current through the resonant circuit and the switches decreases. Consequently, the output power also decreases. In this section, parallel-resonant inverter (PRI) is discussed. The load resistance in this inverter is connected in parallel with the resonant capacitor. As a result, if the load resistance is much higher than the reactance of the resonant capacitor, the current through the resonant inductor and the switches is almost independent of the load. As the load resistance is increased, the voltage across the resonant capacitor and the load increases, causing the output power to increase. (Skvarenina, 2002)

A circuit of a voltage-source half-bridge PRI is shown in below figure.

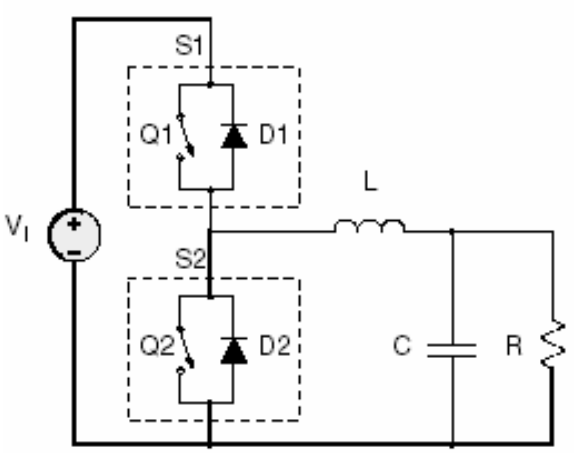

Figure 3.5 Circuit of parallel resonant inverter

It consists of two switches S1 and S2 , a resonant inductor L , and a resonant capacitor C. Resistance R represents a load to which the AC power is to be delivered and is connected in parallel with the resonant capacitor C. In practical realizations, a large DC-blocking capacitor should be connected in series with the load to cut off a DC current flow through the resistance R. The two bidirectional two-quadrant switches S1 and S2 and the DC input voltage source VI form a square-wave voltage source that drives the resonant circuit L– C– R . Each switch consists of a transistor and an antiparallel diode. The switches Q1 and Q2 are turned ON and OFF alternately at the switching frequency f=ω/2*Π. The duty cycle of the switches should be slightly less than 50% to avoid a shoot-through current. The resonant circuit in the inverter is a second-order low-pass filter and can be described by the following normalized parameters(Skvarenina, 2002)

a)The corner frequency (or the undamped natural frequency)

$$Wo = \frac{1}{\sqrt{L \cdot C}} \tag{3-14}$$

b) The characteristic impedance

$$Zo = \sqrt{\frac{L}{C}} = Wo \cdot L = \frac{1}{Wo \cdot C} \tag{3-15}$$

c) The quality factor at the corner frequency fo

$$Q = Wo \cdot C \cdot R = \frac{R}{Wo \cdot L} = \frac{R}{Zo} \tag{3-16}$$

so the input impedance

$$\vec{Z} = Z \cdot e^{i \cdot \psi} = (i \cdot W \cdot L) + \frac{\frac{R}{i \cdot W \cdot C}}{R + \frac{1}{i \cdot W \cdot C}} = \frac{R \cdot \left[1 - \left(\frac{W}{Wo} \right)^2 + i \cdot \frac{1}{Q} \cdot \left(\frac{W}{Wo} \right) \right]}{1 + i \cdot Q \cdot \left(\frac{W}{Wo} \right)} \tag{3-17}$$

where

$$\psi = \arctan\left[Q \cdot \left(\frac{W}{Wo} \right) \cdot \left[\left(\frac{W}{Wo} \right)^2 + \frac{1}{Q^2} - 1 \right] \right] \tag{3-18}$$

The resonant frequency fr is defined as a frequency at which the phase shift ψ is zero. Hence, from above equation, the ratio of the resonant frequency fr to the corner frequency fo is for Q>1

$$\frac{fr}{fo} = \sqrt{1 - \frac{1}{Q^2}} \tag{3-19}$$

Frequency fr forms the boundary between inductive and capacitive loads.

The input voltage of the resonant circuit is a square wave with a low-level value equal to zero (or equal to -Vi in the full-bridge configuration) and a high-level value equal to Vi. The analysis is simplified by assuming sinusoidal currents in L, C, and R. This approximation is valid if the loaded quality factor Q of the resonant circuit is high (e.g., $Q \geq 2.5$). If $Q < 2.5$, the inductor current waveform differs from a sine wave

and an accurate analytical solution is more difficult to obtain. However, the predicted results are still qualitatively correct. (Skvarenina, 2002)

3.2.2 Voltage Transfer Function

The voltage transfer function of the resonant circuit is,

$$\overrightarrow{MVi} = \frac{\vec{Vr}}{\sqrt{2}\cdot Vs} = \frac{\frac{\frac{R}{i\cdot W\cdot C}}{R+\frac{1}{i\cdot W\cdot C}}}{(i\cdot W\cdot L)+\frac{\frac{R}{i\cdot W\cdot C}}{R+\frac{1}{i\cdot W\cdot C}}} = \frac{1}{1-\left(\frac{W}{Wo}\right)^2+i\cdot\frac{1}{Q}\cdot\left(\frac{W}{Wo}\right)} = MVr\cdot e^{i\phi} \quad (3\text{-}20)$$

Where,

$$MVr = \frac{Vr}{Vs} = \frac{1}{\sqrt{\left[1-\left(\frac{W}{Wo}\right)^2\right]^2+\frac{1}{Q^2}\cdot\left(\frac{W}{Wo}\right)^2}} \quad (3\text{-}21)$$

$\vec{Vr}$ is the phasor of the voltage across R, and Vr is the rms value of $\vec{Vr}$.

MVr =Q at f/fo=1

$$MVr = \frac{1}{1-\left(\frac{W}{Wo}\right)^2} \text{ , if Q goes to infinity} \quad (3\text{-}22)$$

Also, the voltage transfer function can be given as a function of f as being in Figure 3.6.

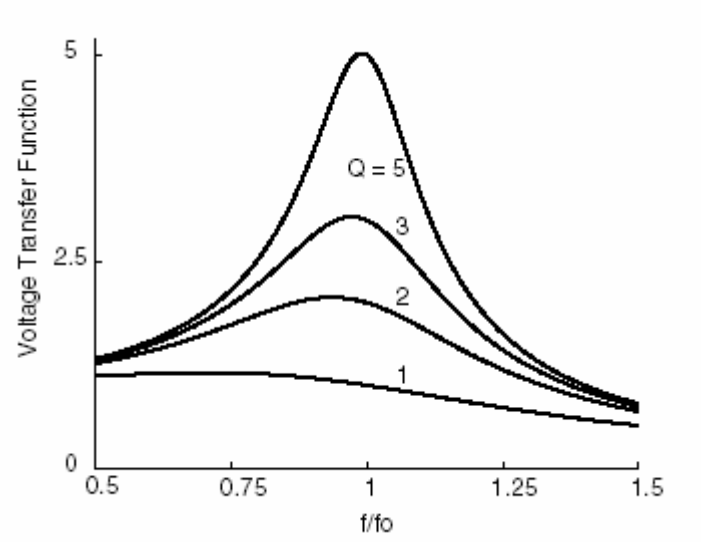

Figure 3.6 Frequency with respect to voltage gain for different quality factor of parallel inverter

The magnitude of the DC-to-AC voltage transfer function of the voltage-source PRI is obtained below;

$$MVi = \frac{Vr}{Vi} = MVs \cdot MVr = \frac{MVs}{\sqrt{\left[1 - \left(\frac{W}{Wo}\right)^2\right]^2 + \frac{1}{Q^2} \cdot \left(\frac{W}{Wo}\right)^2}} \tag{3-23}$$

To find the frequency corresponding to the maximum output voltage the MATLAB package program is used. The commands are given in Appendix A.

So Wmax is found as follows.

$$Wmax = \left(\frac{1}{2}\right) \cdot \frac{\sqrt{4 \cdot Q^2 - 2}}{Q} \cdot Wo \tag{3-24}$$

So when Q goes to infinity Wmax will be equal to Wo. But as seen from above equation we couldn't reach maximum value when W=Wo. To find MVrmax set Wmax value in the Mvr equation.

$$MVrmax = 2 \cdot \frac{Q^2}{\sqrt{-1 + 4 \cdot Q^2}} \tag{3-25}$$

So maximum value can be adjusted by setting Q.

3.3 Voltage Source Series Paralel Resonant Inverters

3.3.1 Circuit and waveforms

This section presents the circuit and major characteristics of a series–parallel-resonant inverter (SPRI). The topology of this inverter is the same as that of the PRI except for an additional capacitor in series with the resonant inductor, or the same as that of the SRI except for an additional capacitor in parallel with the load. As a result, the inverter exhibits the characteristics that are intermediate between those of the SRI and the PRI (Skvarenina, 2002).

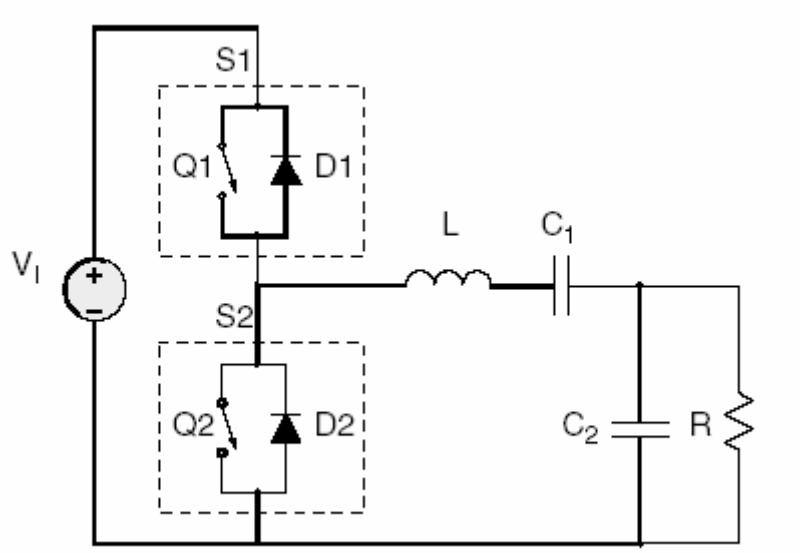

Figure 3.7 Circuit of series parallel resonant inverter

A circuit of the series–parallel-resonant inverter is shown in Figure 3.7. The inverter is composed of two bidirectional two-quadrant switches S1 and S2 and a resonant circuit L-C1-C2-R, where R is the AC load resistance. Capacitor C1 is connected in series with resonant inductor L as in the SRI and capacitor C2 is connected in parallel with the load as in the PRI. The switches consist of transistors

and antiparallel diodes. Each switch can conduct a positive or a negative current. Switches S1 and S2 are alternately turned ON and OFF at the switching frequency f = ω/2*Π with a duty cycle of 50%. If capacitance C1 becomes very large (that is, capacitor C1 is replaced by a DC-blocking capacitor), the SPRI becomes the PRI. If capacitance C2 becomes zero (that is, capacitor C2 is removed from the circuit), the SPRI becomes the SRI. Basic waveforms in the voltage-source SPRI are similar to those in the SRI, as shown previously. (Skvarenina, 2002)

3.3.2 Voltage Transfer Function

The resonant circuit in the inverter is a third-order low-pass filter. Under assumption of a nearly sinusoidal inductor current, the circuit can be described by the following normalized parameters;

a) The ratio of the capacitances

$$A = \frac{C2}{C1} \tag{3-26}$$

b) The equivalent capacitance of C1 and C2 in series

$$C = \frac{C1 \cdot C2}{C1 + C2} = \frac{C2}{1 + A} = \frac{C1}{1 + \frac{1}{A}} \tag{3-27}$$

c) The corner frequency (or the undamped natural frequency)

$$Wo = \frac{1}{\sqrt{L \cdot C}} = \sqrt{\frac{C1 + C2}{L \cdot C1 \cdot C2}} \tag{3-28}$$

d) The characteristic impedance

$$Zo = Wo \cdot L = \frac{1}{Wo \cdot C} = \sqrt{\frac{L}{C}} \tag{3-29}$$

e) The quality factor at the corner frequency fo

$$Q = (Wo \cdot C \cdot R) = \frac{R}{Wo \cdot L} = \frac{R}{Zo} \tag{3-30}$$

The input impedance of the resonant circuit

$$\vec{Z} = Z \cdot e^{i \cdot \psi} = R \cdot \frac{\left[(1 + A) \cdot \left[1 - \left(\frac{W}{Wo} \right)^2 \right] + i \cdot \left(\frac{1}{Q} \right) \cdot \left(\frac{W}{Wo} - \frac{Wo}{W} \cdot \frac{A}{A + 1} \right) \right]}{1 + i \cdot Q \cdot \left(\frac{W}{Wo} \right) \cdot (1 + A)} \tag{3-31}$$

Where

$$Z = Zo \cdot Q \cdot \sqrt{\frac{\left[(1 + A) \cdot \left[1 - \left(\frac{W}{Wo} \right)^2 \right] \right]^2 + \left[\left(\frac{1}{Q} \right) \cdot \left(\frac{W}{Wo} - \frac{Wo}{W} \cdot \frac{A}{A + 1} \right) \right]^2}{1 + \left[Q \cdot \left(\frac{W}{Wo} \right) \cdot (1 + A) \right]^2}} \tag{3-32}$$

$$\psi = \arctan\left[\left(\frac{1}{Q} \right) \cdot \left(\frac{W}{Wo} - \frac{Wo}{W} \cdot \frac{A}{A + 1} \right) - Q \cdot (1 + A)^2 \cdot \left(\frac{W}{Wo} \right) \cdot \left[1 - \left(\frac{W}{Wo} \right)^2 \right] \right] \tag{3-33}$$

at f/fo=1

$$Z = \frac{Zo}{(1 + A) \cdot \sqrt{1 + Q^2 \cdot (1 + A)^2}} \tag{3-34}$$

and for

$Q^2.(1+A)^2 >> 1$

$$Z = \frac{(Zo)^2}{R \cdot (1 + A)^2} \tag{3-35}$$

and

$$\psi = \operatorname{atan}\left[\frac{1}{Q \cdot (1 + A)}\right] \tag{3-36}$$

Thus, Z decreases with increasing A and R at f = fo. Since $\psi > 0$, the resonant circuit always represents an inductive load for the switches at f = fo. The resonant frequency fr is defined as the frequency at which the phase shift ψ is equal to zero. This frequency forms the boundary between capacitive and inductive loads. (Skvarenina, 2002)

The voltage transfer function of the resonant circuit is

$$\overrightarrow{MVr} = \frac{1}{(1 + A) \cdot \left[1 - \left(\frac{W}{Wo}\right)^2\right] + i \cdot \frac{1}{Q} \cdot \left(\frac{W}{Wo} - \frac{Wo}{W} \cdot \frac{A}{A + 1}\right)} = MVr \cdot e^{i \cdot \phi} \tag{3-37}$$

where

$$MVr = \frac{Vr}{Vs} = \frac{1}{\sqrt{(1 + A)^2 \cdot \left[1 - \left(\frac{W}{Wo}\right)^2\right]^2 + \frac{1}{Q^2} \cdot \left(\frac{W}{Wo} - \frac{Wo}{W} \cdot \frac{A}{A + 1}\right)^2}} \tag{3-38}$$

$$\phi = -\operatorname{atan}\left[\frac{\frac{1}{Q} \cdot \left(\frac{W}{Wo} - \frac{Wo}{W} \cdot \frac{A}{A + 1}\right)}{(1 + A) \cdot \left[1 - \left(\frac{W}{Wo}\right)^2\right]}\right] \tag{3-39}$$

Vr is the rms value of the voltage across R, and Vrms is the rms value of the fundamental component of the voltage at the input of the resonant circuit. Figure 3.8 shows the voltage transfer function as a function of f at selected values of Q for A = 1.

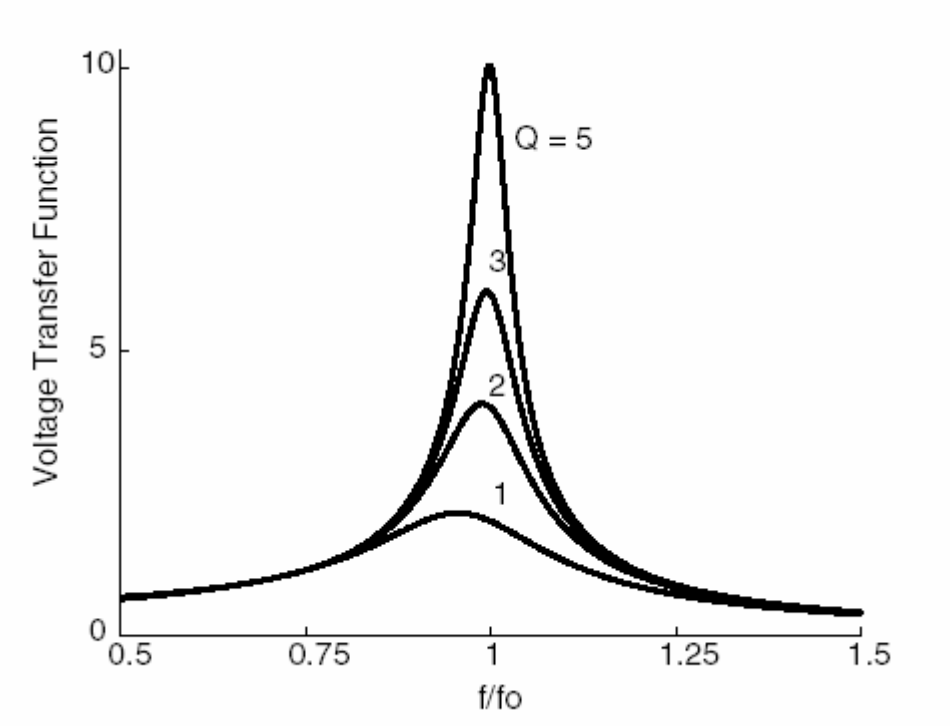

Figure 3.8 Frequency with respect to voltage gain for different quality factor of series parallel inverter

The magnitude of the DC-to-AC voltage transfer function of the voltage source SPRI can be expressed as

$$MVi = \frac{Vr}{Vi} = MVs \cdot MVr = \frac{MVs}{\sqrt{(1+A)^2 \cdot \left[1 - \left(\frac{W}{Wo}\right)^2\right]^2 + \frac{1}{Q^2} \cdot \left(\frac{W}{Wo} - \frac{Wo}{W} \cdot \frac{A}{A+1}\right)^2}} \quad (3\text{-}40)$$

Where MVs is the voltage transfer function of the switching part of the inverter and constant for a particular topology.

To find the frequency corresponding to maximum voltage the MATLAB package program is used. The commands are given in Appendix A. So Wmax can be found in the Appendix A.

In the Wmax equation if we set A=0 then

$$\text{Wmax} = \left(\frac{1}{2}\right) \cdot \frac{\sqrt{4 \cdot Q^2 - 2}}{Q} \cdot \text{Wo} \tag{3-41}$$

Also in the Wmax equation Wmax goes to Wo when A goes to infinity. Therefore, this shows that by changing A it is possible to obtain characteristic of series resonant or parallel resonant inverter.

3.4 Comparison of Resonant Inverters

Three types of inverters are analyzed here. They are the series-resonant inverter (SRI), the parallel resonant inverter (PRI), and the series–parallel-resonant inverter (SPRI). They have a switching block and a resonant circuit. The switching block produces square wave and this square wave is applied to the resonant circuit. The switching block can be composed of the half bridge or full bridge configuration. The full bridge configuration output voltage is the two times with respect to the half bridge configuration, also output power is the four times with respect to the half bridge configuration. The maximum output voltage of series resonant inverter could be equal to peak fundamental component of the square wave which is produced by the switching block, but at the parallel resonant the maximum output voltage could be adjusted by changing quality factor so theoretically, the output voltage can be controlled from zero to infinity. Also maximum output voltage can be controlled by changing quality factor (Q) and capacitance ratio (A) at the series parallel resonant inverter. The maximum voltages across the switches in voltage-source inverters (both half-bridge and full-bridge) are equal to the DC input voltage Vi.

The output voltage can be adjusted by changing switching frequency. As it can be seen in the chapter four output current is nearly constant in the parallel resonant

inverter but in the series resonant converter the output current changes with the load resistance.

Series parallel resonant inverters behavior changes between parallel resonant inverter and series resonant inverter. By decreasing A, the series parallel resonant inverters behave like as parallel resonant inverter. In that case series capacitor behaves like as a dc blocking capacitor.

3.5 THD Performance of Inverters

The main consideration of LCD inverter is to generate a pure sine wave because as being already mentioned a pure sine wave increases efficiency and reduces radiated EMC problems due to unwanted harmonic content. So the total harmonic distortion (THD) value gives us a good idea about performances of these inverters.

By definition,

$$THD = \frac{1}{V1} \cdot \left[\sum_{n=2}^{\infty} (Vn)^2 \right]^{\frac{1}{2}} \qquad (3\text{-}42)$$

V1: is the rms value of fundemantal.

Vn: is the rms value of the nth harmonic.

The THD is affected by the operating frequency and quality factor (Q) for the resonance inverters.

For all types of inverters, the input voltage of resonance circuit has waveform given in Figure 3.9.

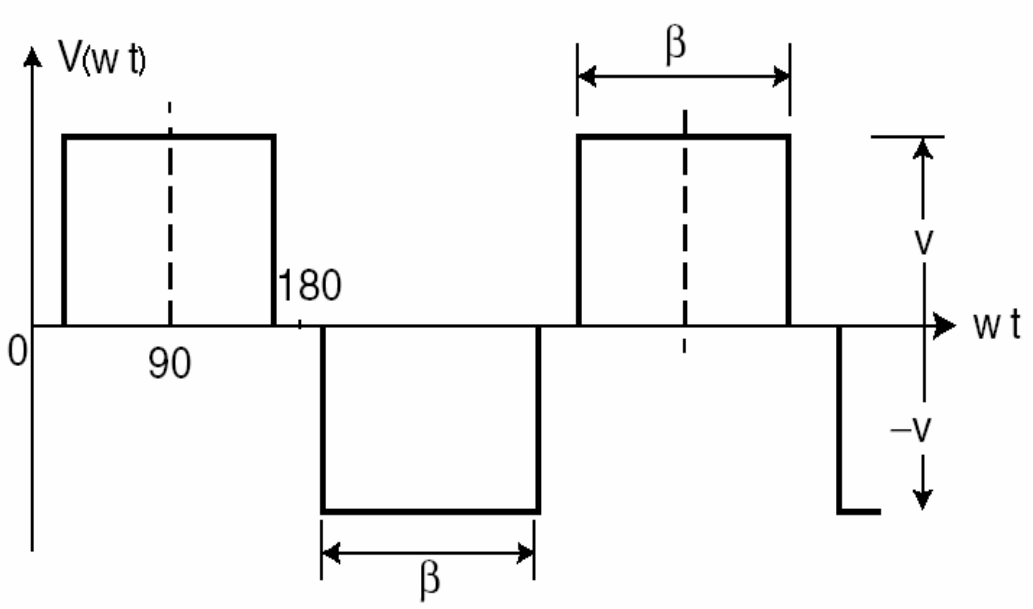

Figure 3.9 Input voltage waveform of resonant inverters

If the supply voltage is Vdc and the configuration is full bridge V=Vdc, if the configuration is half bridge V=Vdc/2 and dead time is equal to (Π-β) in radian.

The fourier series of the waveform will provide the rms value of the fundamental component as

$$V1 = \frac{2 \cdot \sqrt{2} \cdot V}{\Pi} \cdot \sin\left(\frac{\beta}{2}\right) \tag{3-43}$$

The rms value of the nth. harmonic component;

$$Vn = \frac{2 \cdot \sqrt{2} \cdot V}{\Pi \cdot n} \cdot \sin\left(\frac{n \cdot \beta}{2}\right) \tag{3-44}$$

The circuit will be analyzed at the resonant frequency so during simulations the resonance frequency will be used, and the effect of quality factor and dead time will be shown over THD by using the MATLAB mfile. The list of three programs for three different inverters are given in the AppendixB.

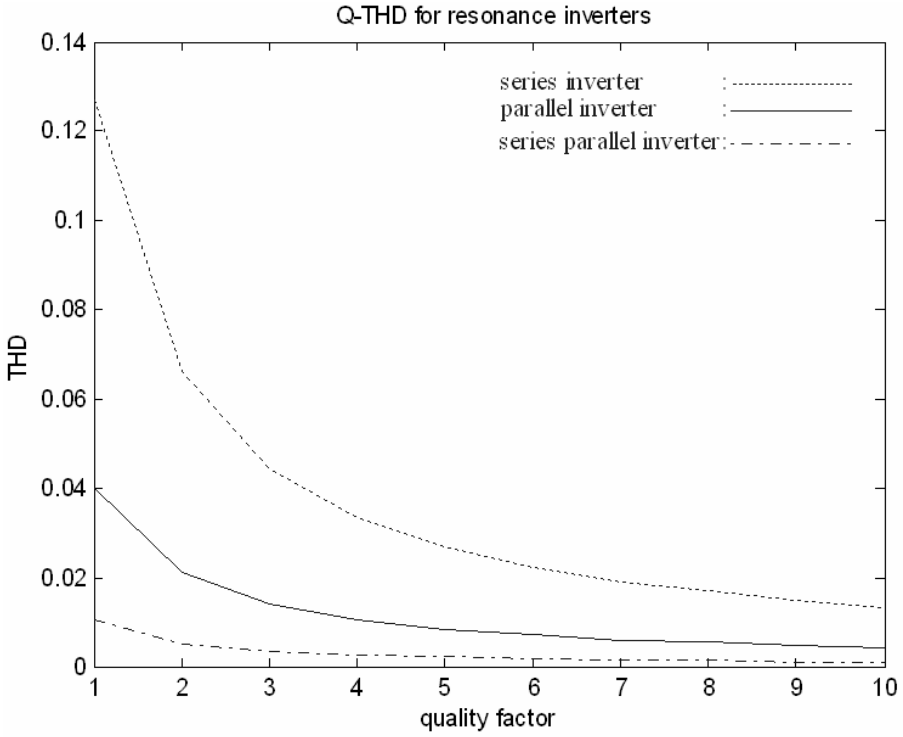

Figure 3.10 Quality factor versus total harmonic distortion of resonance inverters

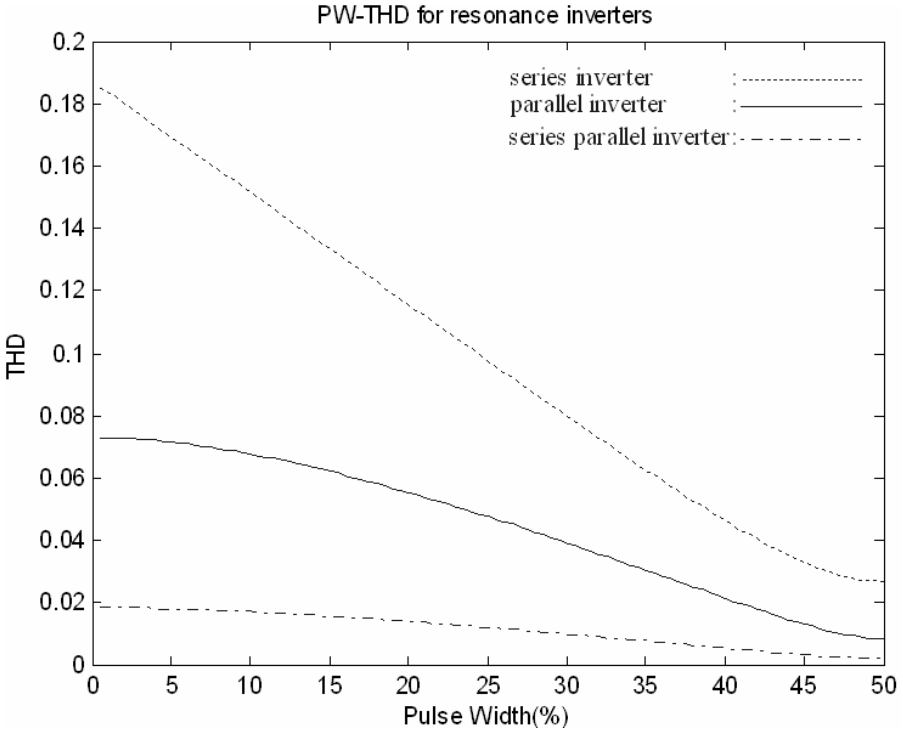

Figure 3.11 Pulse width versus total harmonic distortion of resonance inverters

CHAPTER FOUR
IMPLEMENTATION OF CIRCUIT IN A TFT TV

Parallel resonant inverter is chosen for implementation because of the following reasons.

A) System should be compatible with the solutions in past. The inverter should be supplied from 400Vdc because most of the power supplies uses active PFC circuit at the input stage and they have 400Vdc voltage at the active PFC output. Assume that the series resonant inverter is fed by full bridge inverter, since fundamental component of the input square wave 400**.**(0.9)=360Vrms, the voltage transfer function of series resonant inverter shows that it is impossible to obtain more than 360Vrms at the lamp terminals so, the series resonant inverter cannot be used. When the parallel resonant inverter is used, it is possible to use half bridge topology instead of full bridge(2 mosfet can be used instead of four) and fundamental component is 400**.**(0.45)=180Vrms. Due to the voltage transfer function, by adjusting quality factor the voltage can be set to desired level for the lamp terminals. Therefore it is obvious that due to voltage requirements, the parallel resonant inverter should be chosen.

B) Lamp is a gas discharge device and its brightness depends on the lamp current. In order to prevent flicker at the TFT screen, the lamp brightness can be kept constant by the control of lamp current.

The voltage transfer function has been obtained before as follows;

$$MVi = \frac{MVs \cdot R}{Wo \cdot L} \qquad (4\text{-}1)$$

The transfer function of the lamp current is

$$MIi = \frac{MVi}{R} = \frac{MVs}{Wo \cdot L} \tag{4-2}$$

As it is seen from the MIi equation, the lamp current is independent to the lamp resistance or lamp characteristic. But at the series resonant inverter, referring to the voltage transfer function and assuming that the operation is carried out at the resonant frequency, the voltage transfer function can be found as follows

$$MVi = MVs \tag{4-3}$$

The transfer function of the lamp current is

$$MIi = \frac{MVi}{R} = \frac{MVs}{R} \tag{4-4}$$

This means that the lamp current is related to the lamp resistance.

4.1 Component Selection and Circuit Realization

The proper operation of the circuit can be obtained by selecting its parameters. The following parameters have been defined.

a) Lamp operating frequency=f
b) Lamp operating voltage=Vr
c) Lamp operating current=Ir
d) Lamp typical starting voltage=Vst
e) Dead time=td
f) Topology of the bridge inverter (half or full)

The followings are given as specifications for the CCFL.

a) Lamp typical operating frequency	:50kHz to 60kHz
b) Lamp typical operating voltage	:560Vrms
c) Lamp typical operating current	:7.5 mArms

d) Lamp typical starting voltage :1300Vrms

The following waveforms are recorded on the CCFL in 15'' panel. This voltage waveform is generated by an inverter supplying power to the lamps via transformer. The operating point is got from these waveforms available on existing TVs.

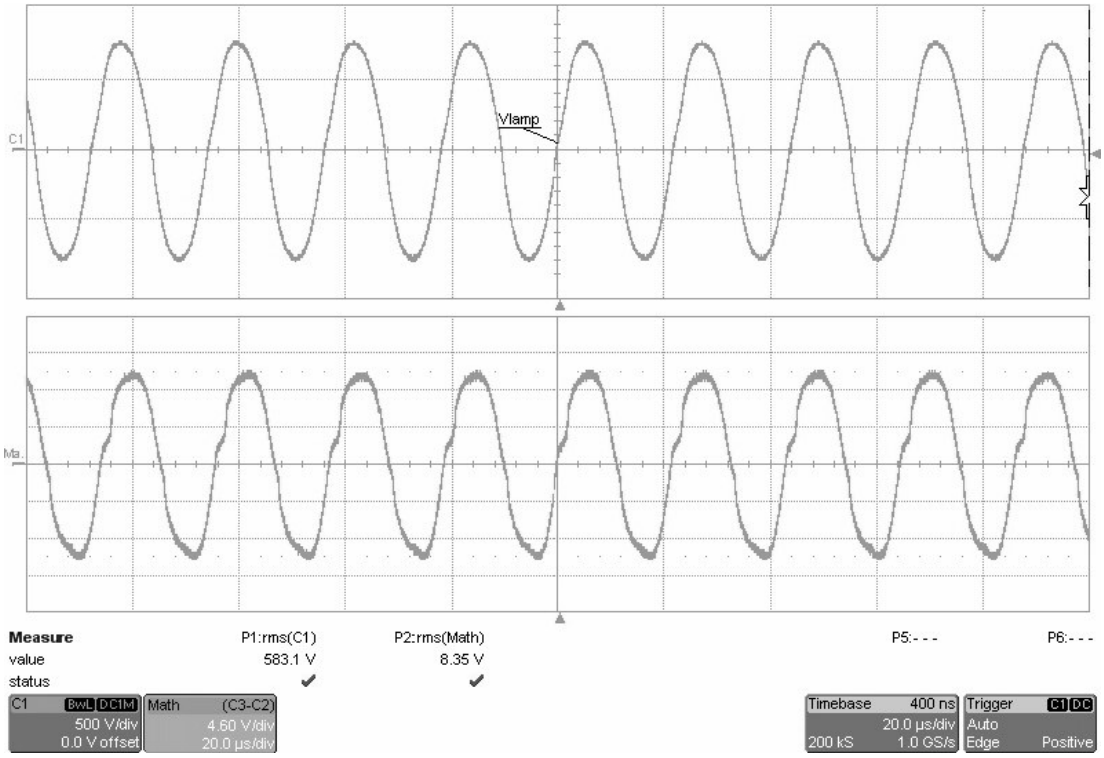

Figure 4.1 Sample lamp measurement

Figure 4.1 is taken from existing lamp.

a) Operating frequency=46.5 kHz

b) Operating voltage=583V

c) Operating current=8.35mA

d) Luminance=310 cd/m^2

During the operation of the lamp, there are two modes. One of them is 'run mode' and the other is 'preheat mode'.

The design of the circuit will be carried out for run mode according to the specification given below;

a) Lamp operating frequency, f=55khz
b) Lamp operating voltage , Vr=560Vrms
c) Lamp operating current, Ir=7.5mArms
d) Dead time, td=0
e) Half bridge topology selected

f=55e3⇒Wo=345580;
Vi=390;

$$MVs = \left(\frac{1}{2}\right)\cdot\left(\frac{4}{\pi}\right)\cdot\left(\frac{1}{\sqrt{2}}\right)\cdot\sin\left[(1-2\cdot f\cdot td)\cdot\left(\frac{\pi}{2}\right)\right] = 0.45 \tag{4-5}$$

$$Vs = Vrms = Vi\cdot\left(\frac{1}{2}\right)\cdot\left(\frac{4}{\pi}\right)\cdot\left(\frac{1}{\sqrt{2}}\right)\cdot\sin\left[(1-2\cdot f\cdot td)\cdot\left(\frac{\pi}{2}\right)\right] = 175 \tag{4-6}$$

At the resonant frequency W=Wo

$$MVr = Q \tag{4-7}$$

So

$$MVi = \frac{Vr}{Vi} = (MVr)\cdot(MVs) = Q\cdot 0.45 = 1.4359 \tag{4-8}$$

Note that Vi=390V
solve Q from (4-8)

$$Q = \frac{MVi}{MVs} = 3.19 \tag{4-9}$$

$$R = Rlamp = \frac{Vr}{Ir} = 75000 \tag{4-10}$$

Hence,

$$Q = R \cdot \frac{Wo}{L} \tag{4-11}$$

Find L

$$L = \frac{R}{(Wo \cdot Q)} = \frac{75000}{(345580 \cdot 3.19)} = 0.068H \tag{4-12}$$

Using

$$Wo = \frac{1}{\sqrt{L \cdot C}} \tag{4-13}$$

Finally find C as follows;

$$C = \frac{\left(\frac{1}{Wo \cdot Wo}\right)}{L} = \frac{\frac{1}{345580 \cdot 345580}}{0.068} = 120pF \tag{4-14}$$

During the preheat mode, the lamp is assumed as open circuit and the voltage across the lamp goes to infinity theoretically at the resonant frequency. Therefore, the operating frequency in this mode should be shifted (Rashid, M.H., 1993).

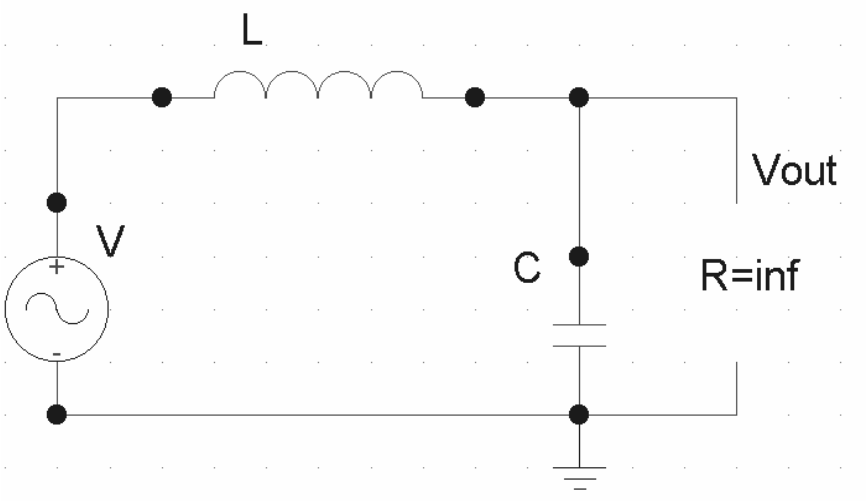

Figure 4.2 Preheat circuit behavior model (ionization is not available)

$$V = MVs \cdot Vi \tag{4-15}$$

$$\overrightarrow{Vout} = \frac{V}{(i \cdot W \cdot L) + \left(\frac{1}{i \cdot W \cdot C}\right)} \cdot \left(\frac{1}{i \cdot W \cdot C}\right) \tag{4-16}$$

$$Vout = \frac{V}{1 - W^2 \cdot L \cdot C} \tag{4-17}$$

by using above equation substitute W and find fph.

$Vi = 390V$

$MVs = 0.45$

$V = Vi \cdot MVs = 175V$

$Vout = 1300V$

Operating frequency during preheat is;

$$Wph = \sqrt{\frac{(Vout - V)}{Vout \cdot L \cdot C}} \tag{4-18}$$

Wph= 325570

fph=51.8kHz

4.2 Modification of Circuit for Two Lamps

There are more than one lamp in the TVs for backlight. The circuit designed for a lamp should supply power to all lamps in a TV. In a 32'' TV, there are more than 10 lamps and the backlight illumination brightness should be uniform on the panel surface. If this condition is not satisfied, some parts of the picture on the screen will be bright and some parts of the picture will be dark. This is the major disadvantage of LCDs compared to plasma displays. Therefore the uniformity of brightness should be obtained by controlling the light illumination of lamps fed by inverter. In this thesis, 15'' panel is taken into account. This panel has two CCFL lamps as shown in Figure 4.3.

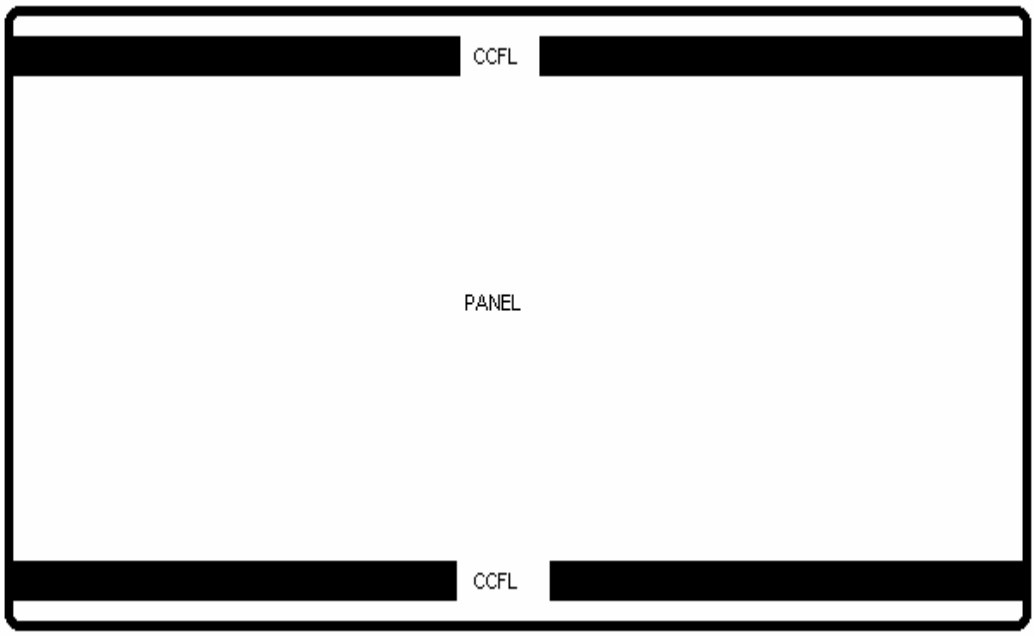

Figure 4.3 CCFL placement of 15'' LCD panel.

A uniform brightness on the screen can be obtained, if two lamps have same illumination. A typical value of luminance uniformity factor defined in equation 4-19 is given as 1.3 for this 15'' panel.

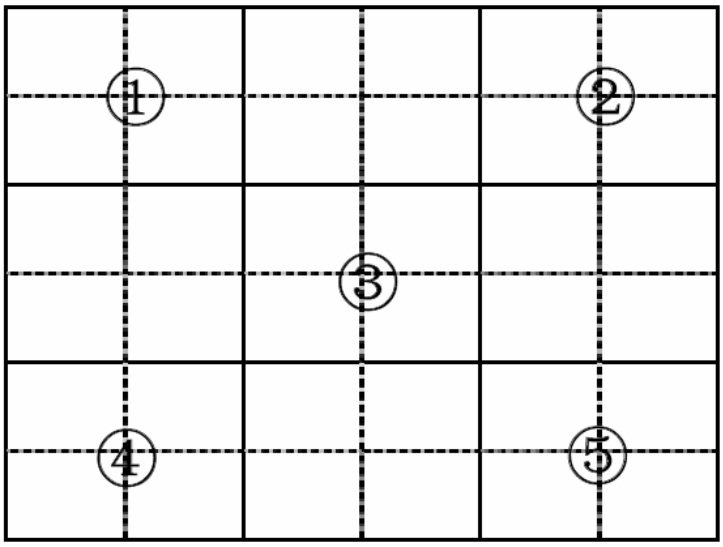

Figure 4.4 luminance measurement points for brightness uniformity

5 different points are chosen on the panel such that one of the points should be at the center of panel and other four points should be near the panel sides. At the chosen points the brightness is measured by using color analyzer (CA-210) manufactured by Konica Minolta. Five luminance information is obtained on the screen given in Figure 4.4 with the labels L1, L2, L3, L4, L5 and luminance uniformity defined as below.

$$\text{"luminance uniformity"} = \frac{\text{"maximum luminance from L1 to L5'}}{\text{"minimum luminance from L1 to L5"}} \tag{4-19}$$

This 15'' panel is inspected for brightness uniformity when the lamps are driven by a conventional inverter. And the luminance values are obtained as given below.
L1=234 cd/m^2, L2=243 cd/m^2, L3=301 cd/m^2, L4=240 cd/m^2, L5=260 cd/m^2.

So luminance uniformity is

$$\frac{301}{234} = 1.286$$

Even if two resonant circuits of two lamps are fed at the resonant frequency, two lamps may not provide equal brightness. The component tolerances and parasitic capacitances are important parameters for a resonant circuit. Therefore, the output

voltage of the resonant circuits may be different for two lamps and brightness uniformity may not be satisfied. The block diagram of circuit is given Figure 4.5.

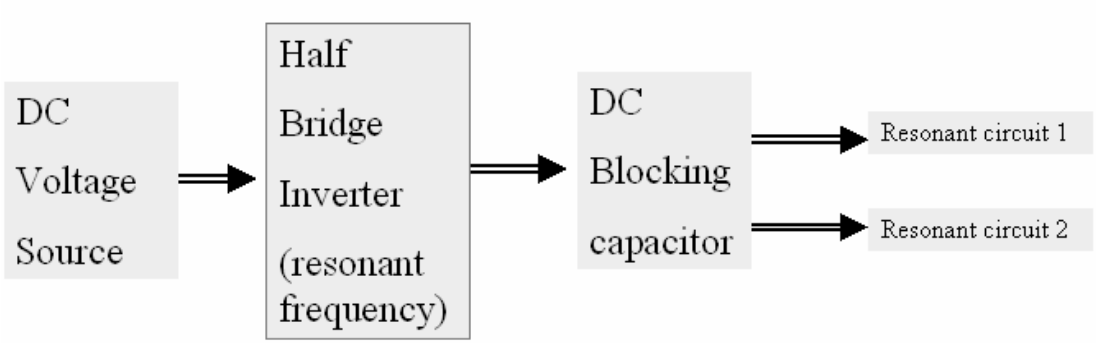

Figure 4.5 Block diagram of CCFL inverter with brightness uniformity problem

In order to solve this brightness uniformity problem, the following approaches can be used;

a)Different resonant frequency for different resonant circuits.

The operating frequency of half bridge inverter can be adjusted to compensate component tolerances and parasitic capacitance effect. But it is obvious that an inverter for each lamp is required and this solution increases total cost. This solution is depicted in the following figure.

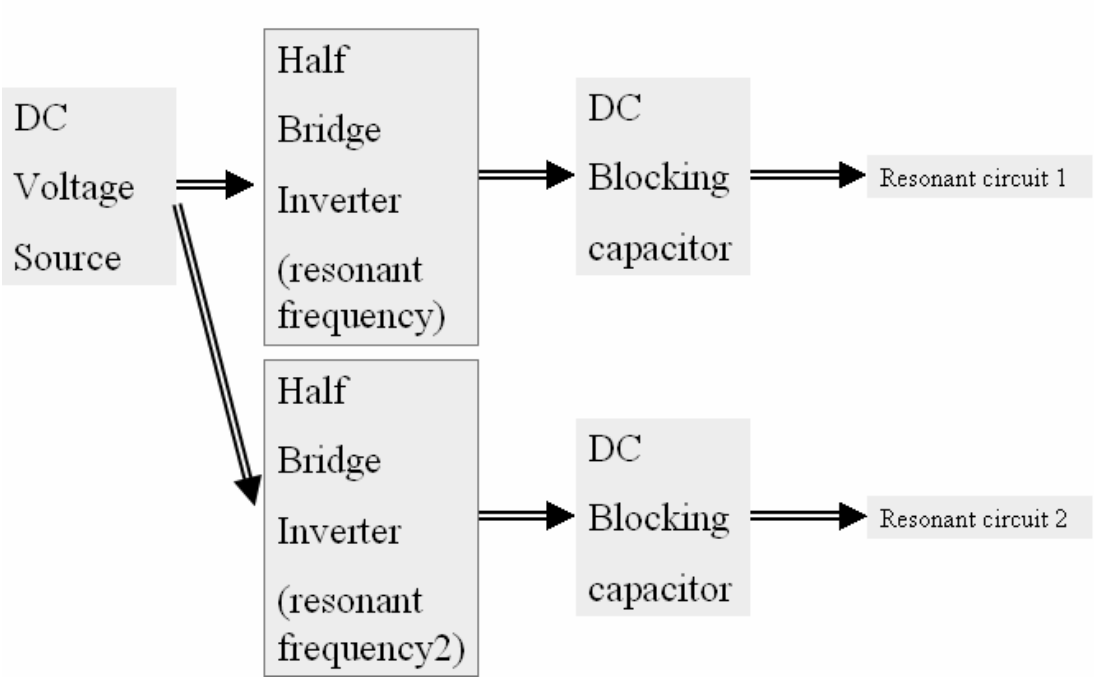

Figure 4.6 Block diagram of different resonant frequency for different resonant circuit to solve brightness uniformity problem

b)Decrease quality factor

By decreasing the quality factor, as shown in Figure 3.6, the output voltage sensitivity due to variation of circuit elements decreases. Therefore, the quality factor can be reduced to make the circuit stable against parasitic effects and component tolerances. However, the magnitude of output voltage decreases. In order to compensate this reduction, the input voltage can be boosted. But the input voltage is kept constant by the power supply. It is clear that this is not a proper solution for this application.

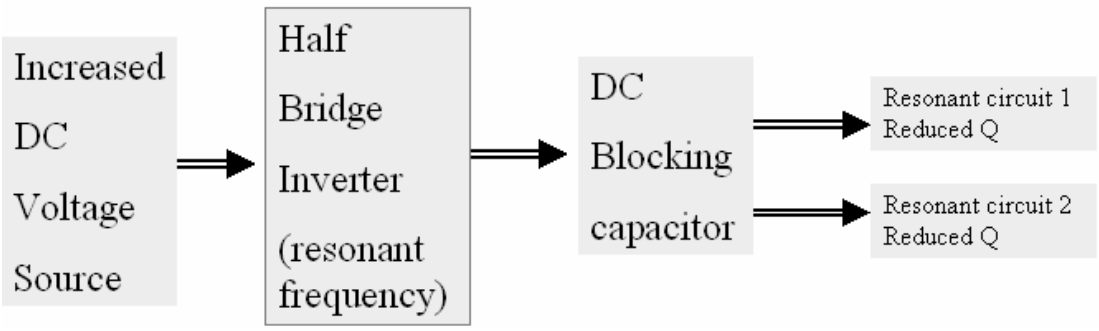

Figure 4.7 Block diagram of decreased quality factor for solving brightness uniformity problem

c) Select the frequency of inverter

An other method for solving brightness uniformity problem is to shift the operating frequency out of resonance. This shifting makes the circuit more stable against the parameter variation. The reduction of output voltage can be compensated by increasing quality factor to a new one. This technique is implemented in this study.

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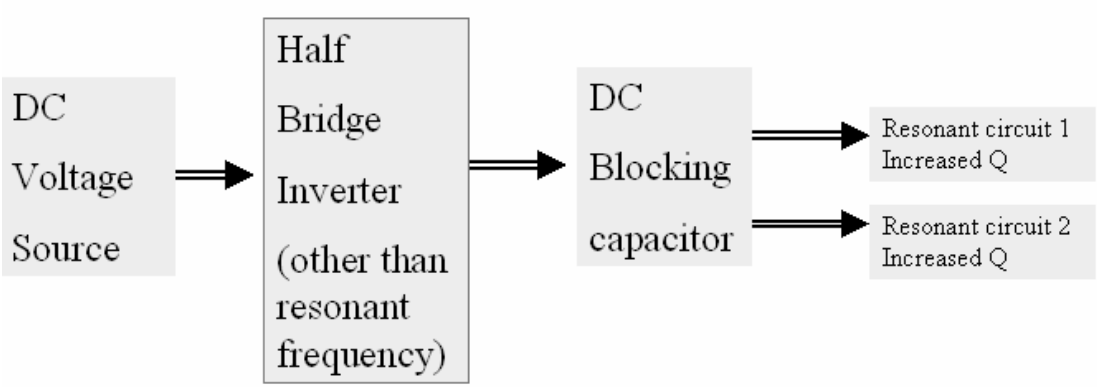

Figure 4.8 Block diagram of implemented circuit to solve brightness uniformity problem

4.2.1 Analysis of Circuit for New Operating Frequency

The parasitic effects can be minimized by increasing capacitor in parallel to the lamp. This value is selected as 270 pF. In order to keep the resonant frequency almost constant, the inductance is decreased, due to its availability in market, to a value of 25 mH. These values yield the resonant frequency at 62 kHz. The new operating point is set to 54 kHz which is in the range of lamp specifications. The parallel resonance circuit is analyzed in PSPICE package program.

The results of run mode simulations are given in Figure 10,12,13,14,15. The Figure 10 shows the variation of voltage across a lamp with respect to frequency which is called as an ac analysis. For this ac analysis, the schematic given in Figure 9, was used. For this analysis the fundamental component will be used for input. Peak value of first fundamental component is (390/2).(4/Π)=248.28Vrms. It is clear that the

operating point is on the smooth variation part of curve, below the resonance. The peak of output voltage is almost 800V at this operating point. For the steady state run mode condition the schematics, which is given at Figure 4.11, was used. The variation of voltage and lamp current in time are given Figure 12 and Figure 13 respectively. At Figure 14 output of half bridge circuit is given which is measured from point A. In Figure 4.15 shows the voltage at the point B. This waveform clearly shows that the dc level is hold by the capacitor located between the points A and B.

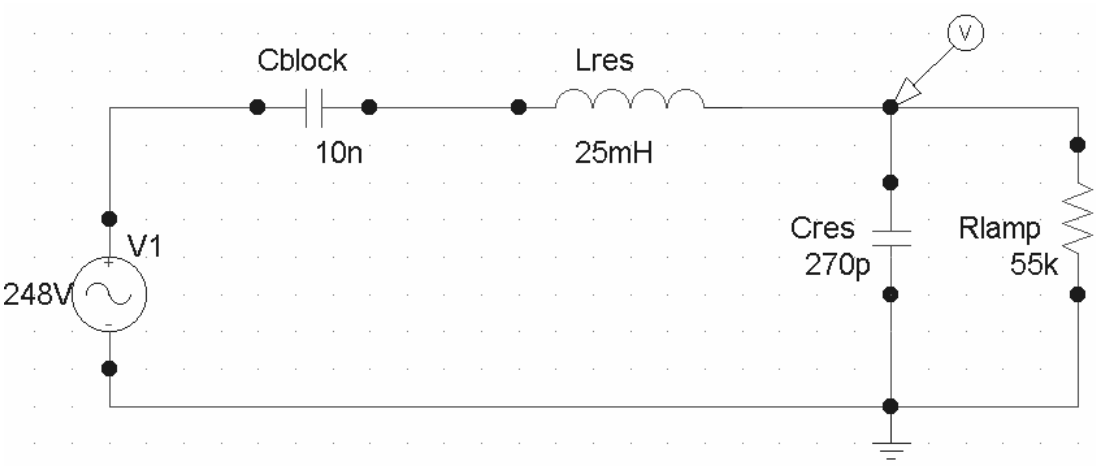

Figure 4.9 PSPICE simulation schematics for run mode ac analysis.

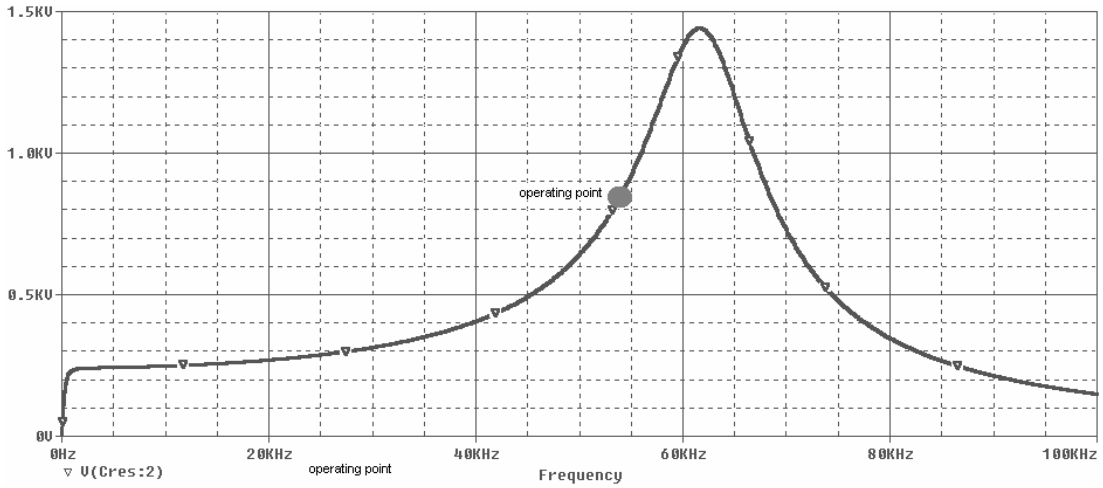

Figure 4.10 Run mode output voltage with respect to frequency

The lamp is represented by a resistor having a value of 55 kOhms. This value is computed by using the voltage and current measurements. These measured waveforms have been given in section 4.1. According to those results the lamp

current is 10.02 mA and voltage is 554 V. Therefore the resistor is 554/10.02=55.2 kOhms.

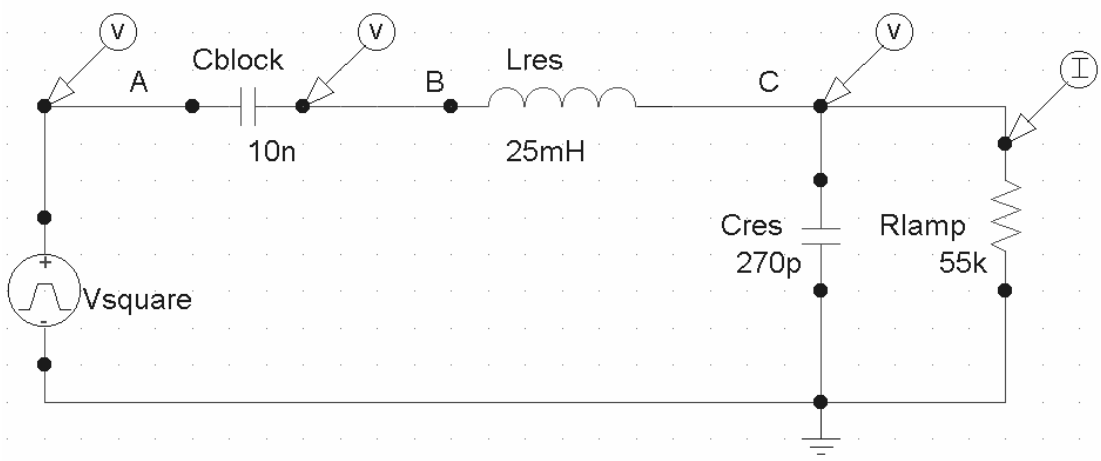

Figure 4.11 PSPICE simulation schematics for run mode analysis.

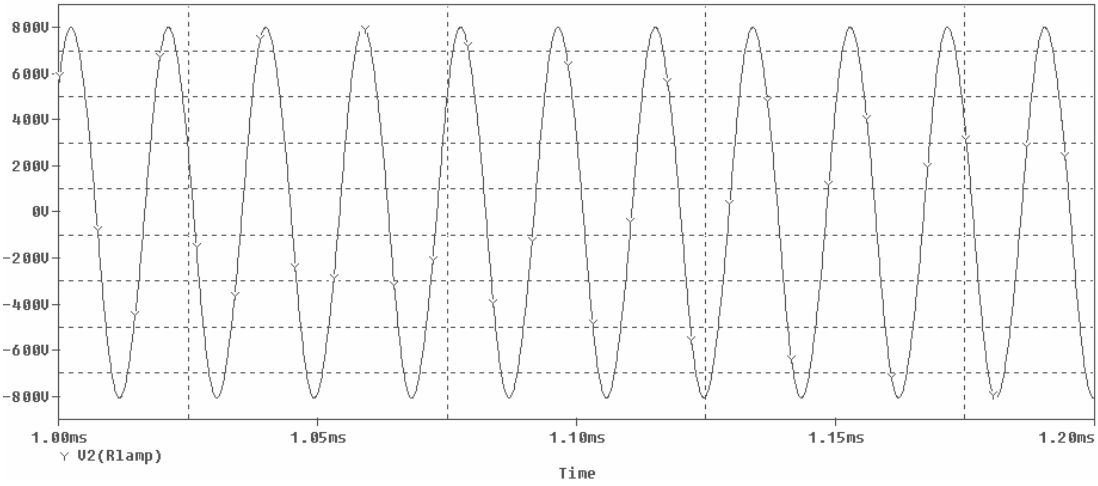

Figure 4.12 Output voltage with respect to time

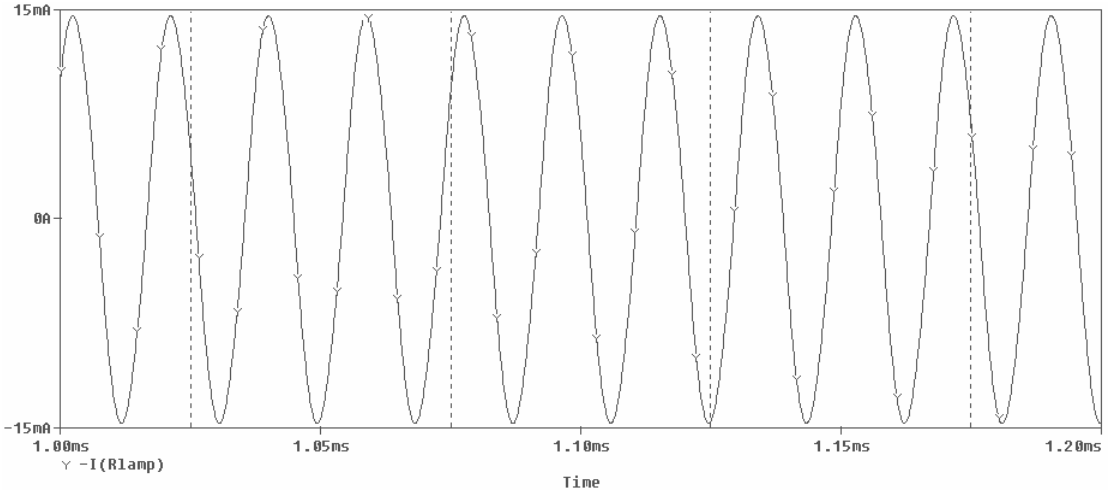

Figure 4.13 Output current with respect to time

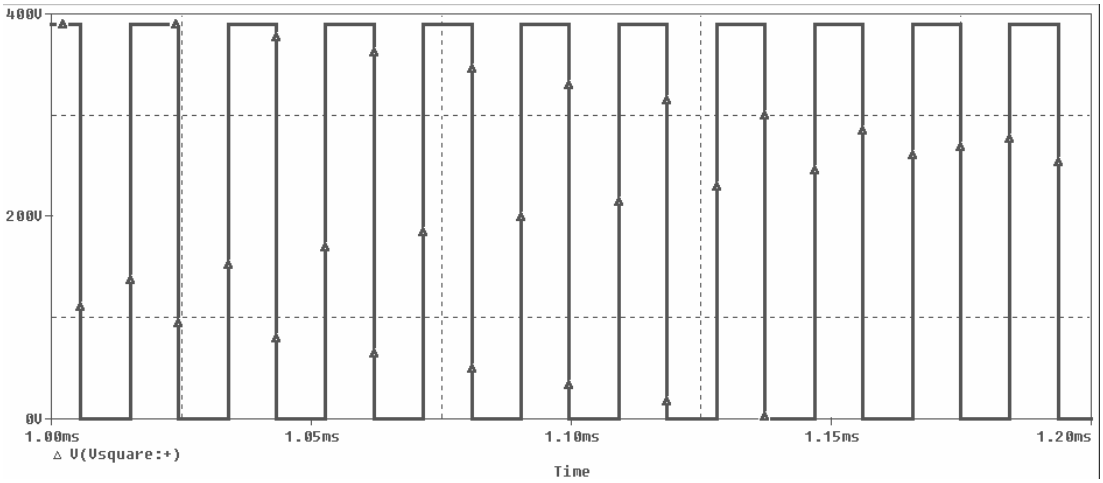

Figure 4.14 Half bridge output voltage

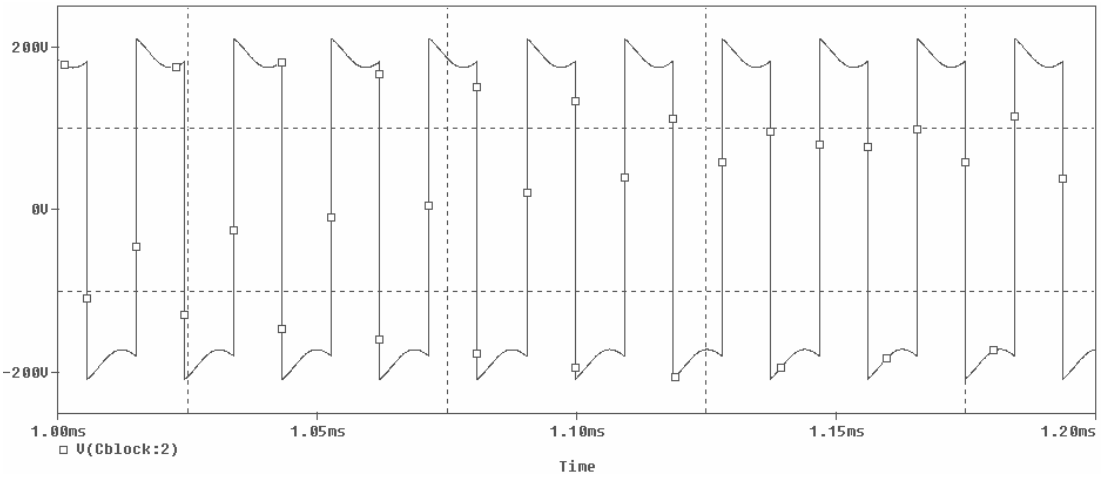

Figure 4.15 Resonant circuit input voltage after than dc blocking capacitor

The operating frequency during preheat is computed with the new circuit parameters as follows;

choosen

L=25e-3

C=270e-12

Vi=390V

$$MVs = \left(\frac{1}{2} \cdot \frac{4}{\Pi} \cdot \frac{1}{\sqrt{2}} \right) = 0.45 \tag{4-20}$$

V=Vi.MVs=175V

Vout=1300V

$$Wph = \sqrt{\frac{(Vout - V)}{Vout} \left(\frac{1}{L \cdot C} \right)} \tag{4-21}$$

Wph=3.5797e+005

fph=56.97kHz

The circuit is also analyzed in PSPICE for preheat mode as shown in Figure 4.16. The variation of voltage across the output capacitor with respect to operating frequency is shown in Figure 4.17. Figure 4.18 shows the zoom in of voltage variation around preheat operating frequency.

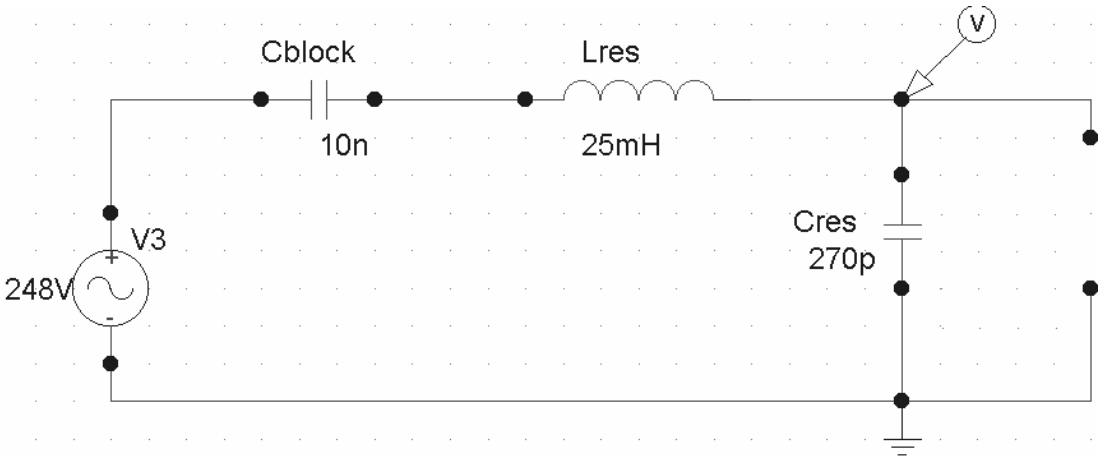

Figure 4.16 PSPICE simulation schematics for preheat mode ac analysis.

As it can be observed from Figure 4.17 the voltage goes to very high values around the resonance frequency. In order to limit this voltage around 1.5 kV, the operating frequency has been selected as 57 kHz for preheat (starting) mode.

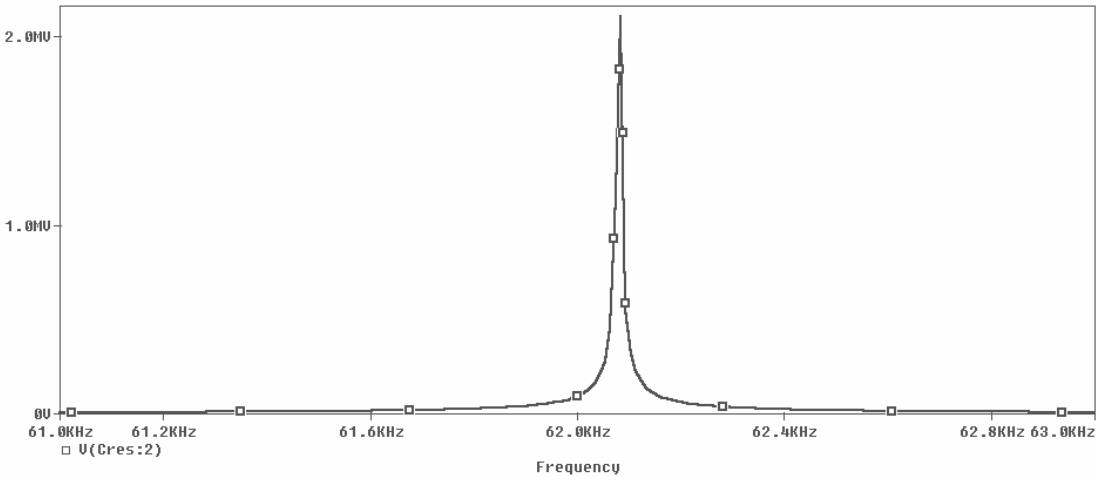

Figure 4.17 Output voltage with respect to frequency for preheat mode

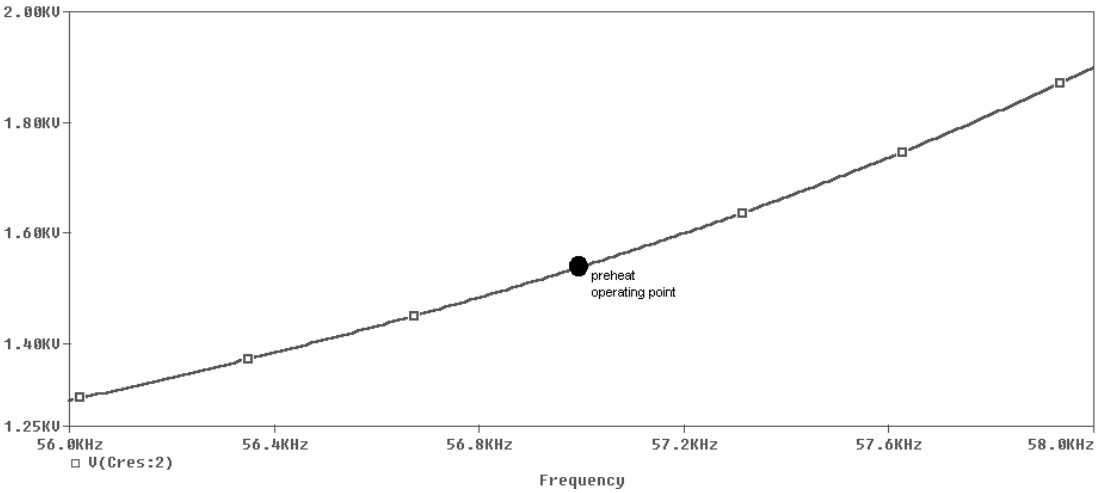

Figure 4.18 Zoom in graphics of output voltage with respect to frequency for preheat mode

4.3 Results of Experimental Work

A photo of the experimental set up and schematic diagram of the circuit are given in Figure 4.19 and 4.20 respectively.

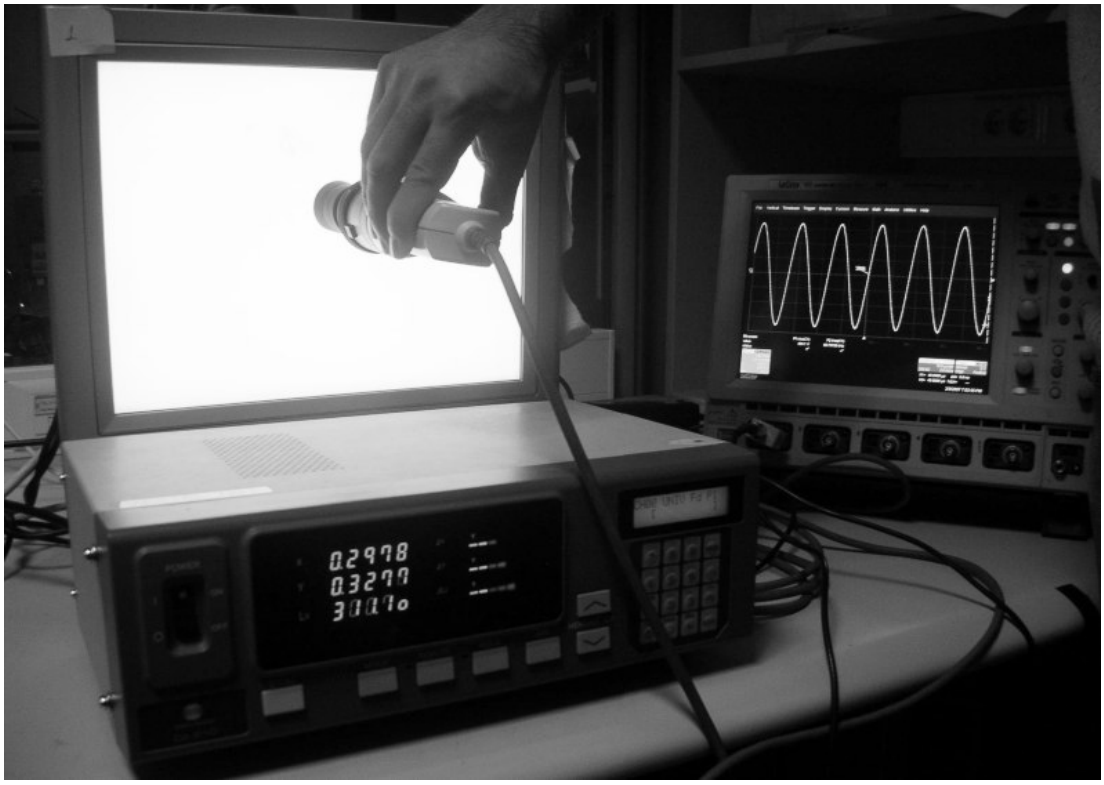

Figure 4.19 Picture of experimental work

An integrated circuit (IC-IR2167) is used to control the resonant inverter. The external components control the preheat and the run mode frequency. These relations are given by the following equations.

$$fph = \frac{1}{2 \cdot \left[\left(\frac{Rt \cdot R1}{Rt + R1} \right) + td \right]} \tag{4-22}$$

$$frun = \frac{1}{2 \cdot [(Rt \cdot C2) + td]} \tag{4-23}$$

where Rt is;

$$Rt = \frac{R2 \cdot VR1}{R2 + VR1} \tag{4-24}$$

and where td is;

$$td = 0.69 \cdot C2 \cdot R4 \tag{4-25}$$

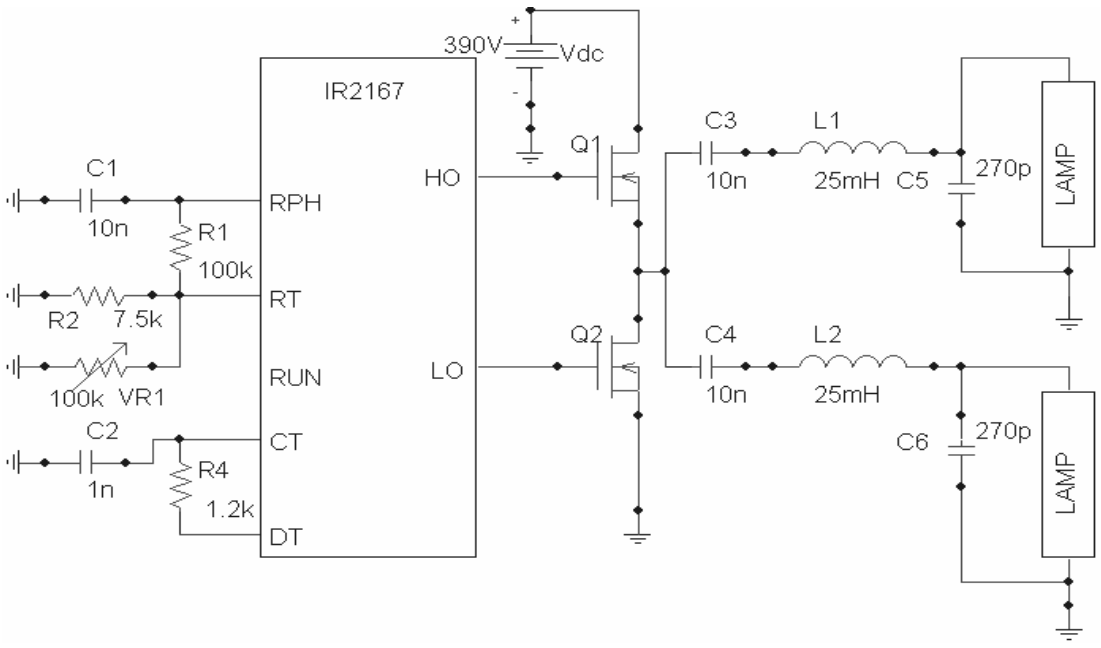

Figure 4.20 Schematic diagram of experimental work.

The measurements are obtained during run mode (steady-state) and preheat mode.

Luminance values are measured from 5 points as mentioned at chapter 4.2. These values are given below for the points L1, L2, L3, L4 and L5 marked in Figure 4.4

L1=262 cd/m^2, L2=255 cd/m^2, L3=317 cd/m^2, L4=271 cd/m^2, L5=285 cd/m^2.

So luminance uniformity is 317/255=1.24 which is better than previous design.

The output voltage of half bridge inverter is recorded and given in Figure 4.21. The peak of voltage is 390 V and the duty cycle is almost %50. The frequency of voltage is almost 54 kHz.

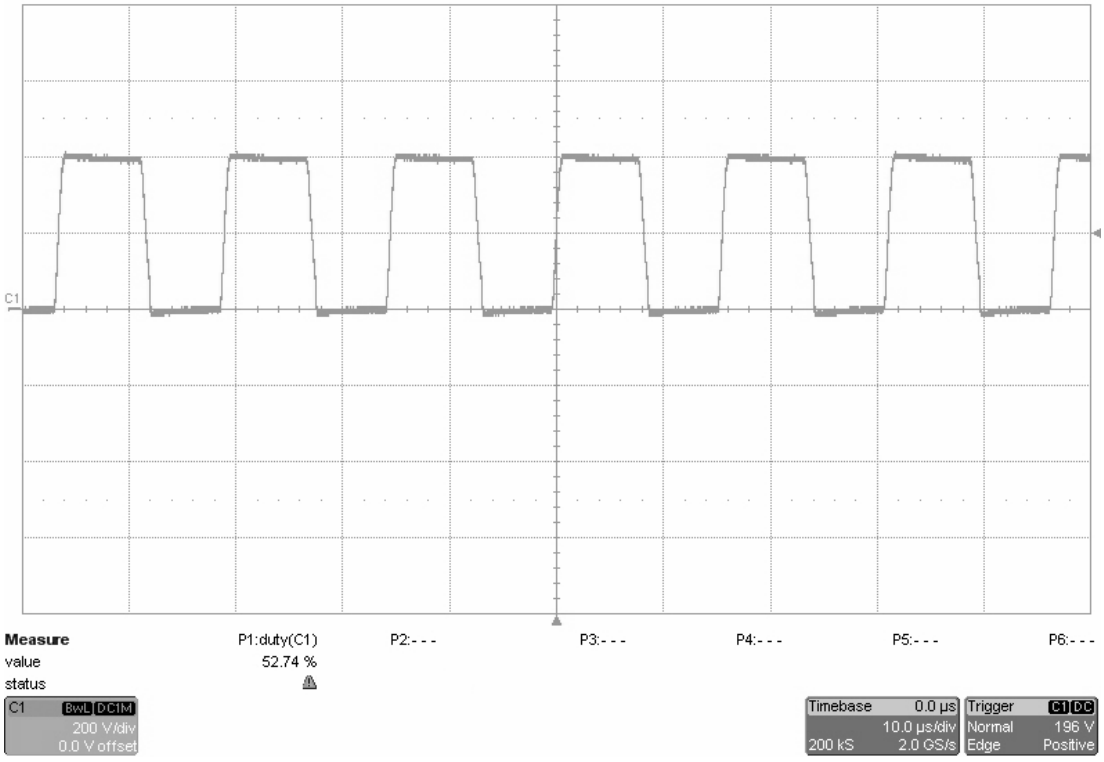

Figure 4.21 Half bridge output voltage

The ac component of bridge inverter output voltage is also recorded. The dc component is blocked by the series capacitor. This waveform is given in Figure 4.22.

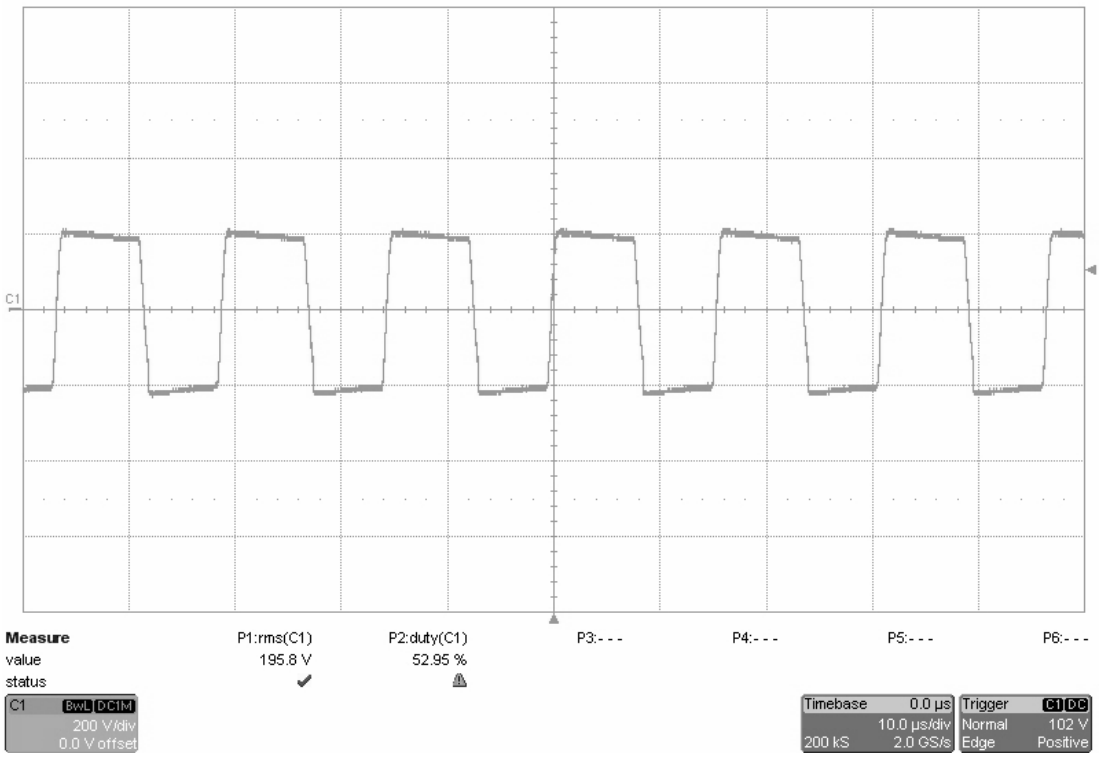

Figure 4.22 Half bridge output voltage after dc blocking capacitor

The voltage across the lamp and current through the lamp are measured and given Figure 4.23. It is obvious that both of them sinusoidal and in phase. The peak value of voltage is 783 V and the peak value of current is 14.17 mA.

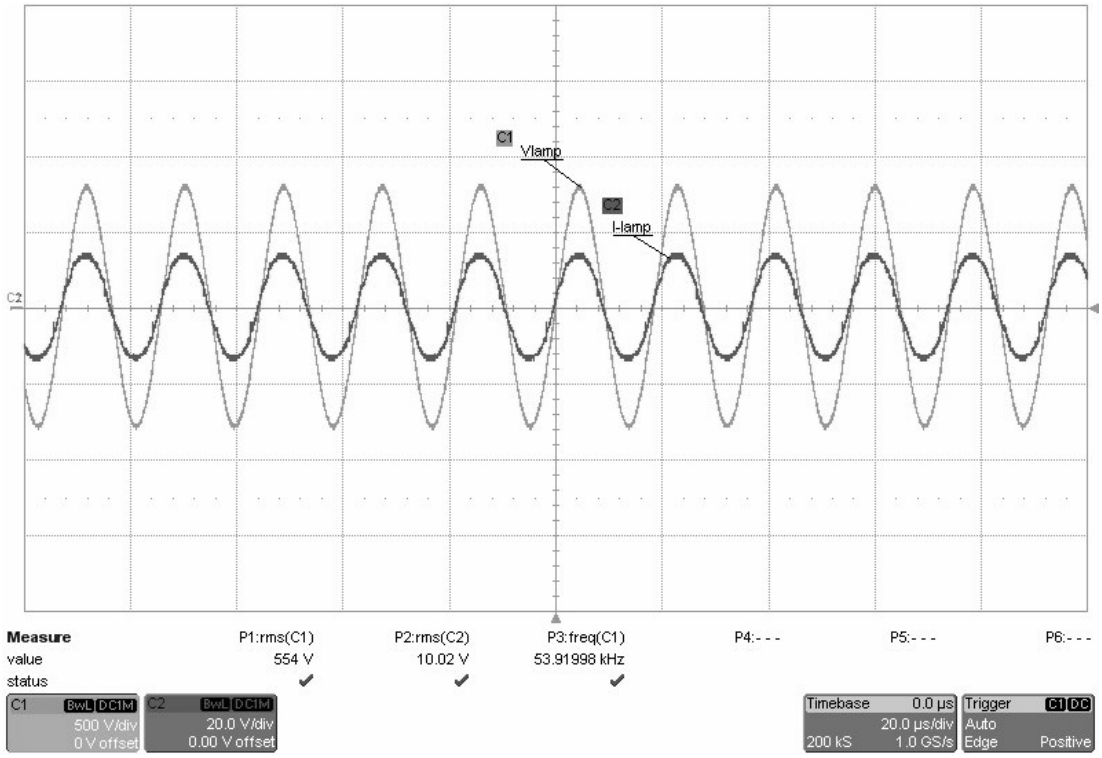

Figure 4.23 Lamp voltage and lamp current

The variation of voltage across the lamp is given in Figure 4.24 for starting (preheat) and running modes. The magnitude of voltage is successfully controlled by the IC. The ionization is started by 1300 V, but that instant is not captured by the recorder. The time adjusted for preheat which is 1.3 seconds, then the run mode frequency takes over the operation. The voltage across the lamp is recorded in zoom in to verify the calculated frequency. This waveform is given in Figure 4.25. Figure 4.26 shows the voltage variation during preheat period while the lamp is removed. The dc level appears on the waveform until the dc blocking capacitor charges up. The frequency is lower than resonance frequency, and its value is measured as 56.7 kHz.

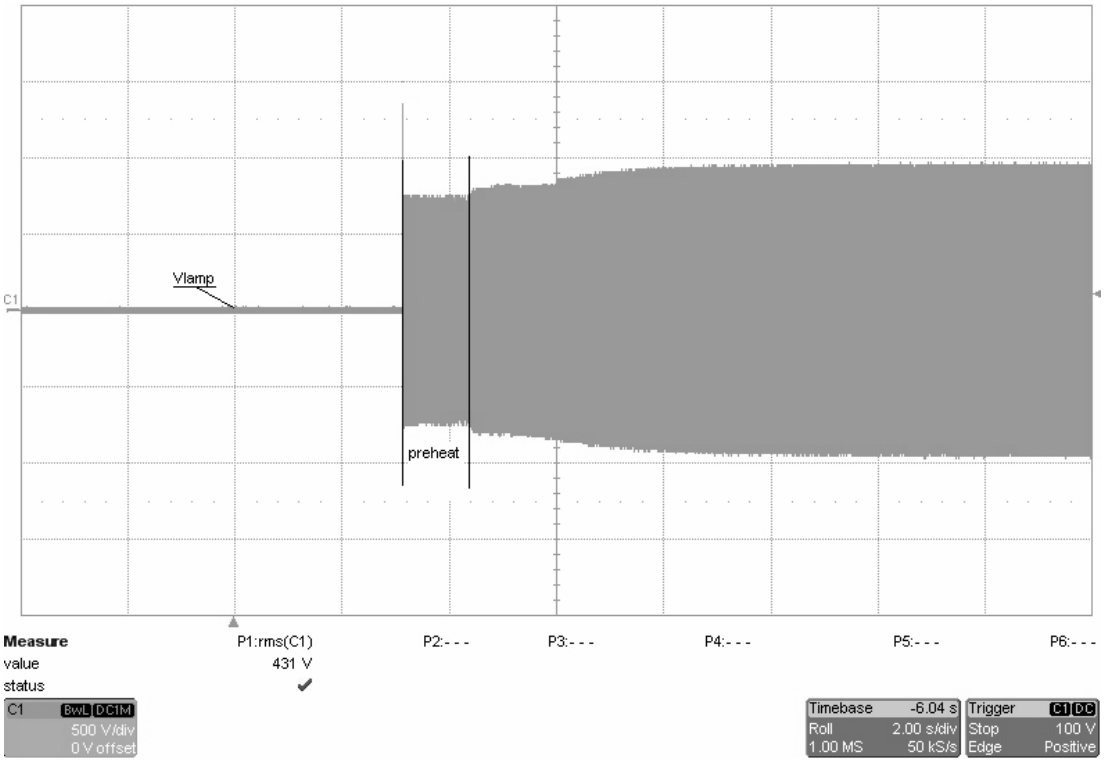

Figure 4.24 Lamp startup voltage

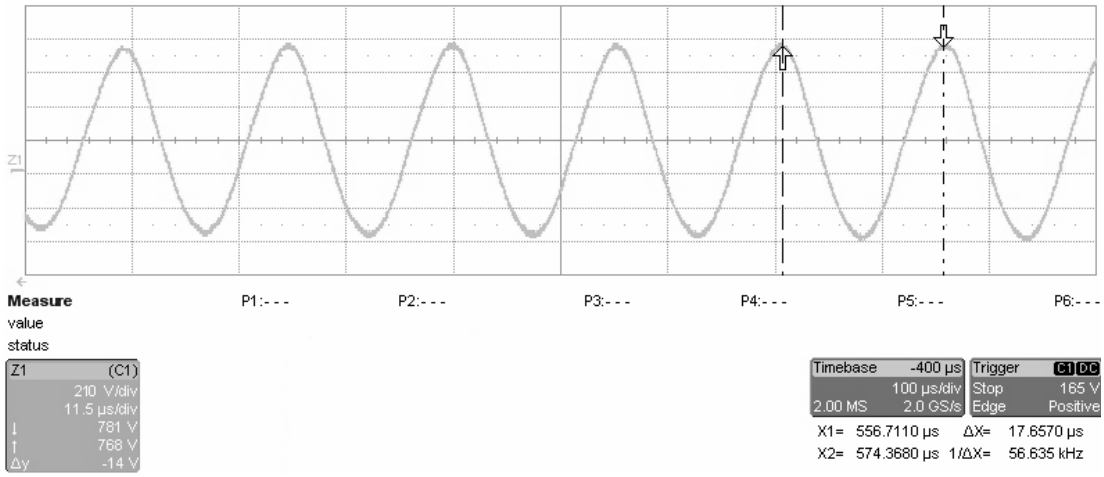

Figure 4.25 Zoom in lamp startup voltage

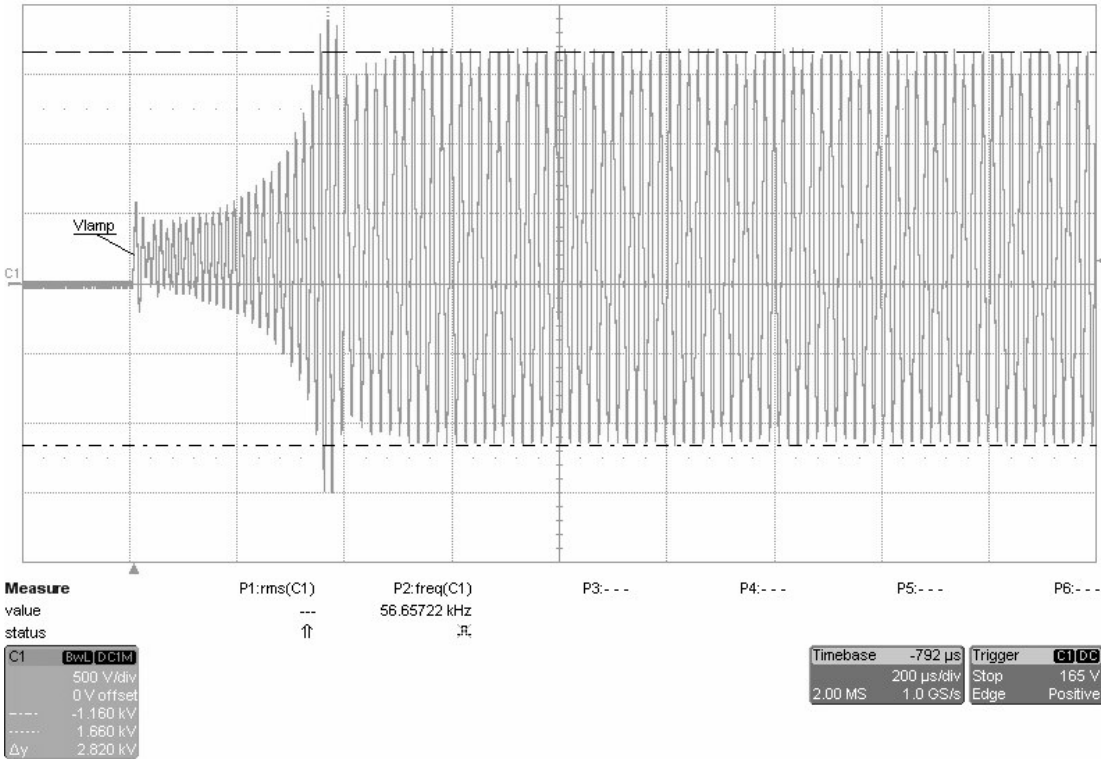

Figure 4.26 Open circuit startup voltage

CHAPTER FIVE
CONCLUSIONS

This thesis introduced a new drive circuit for LCD (Liquid Crystal Display) TVs. In this thesis, the previous inverter designs were examined and the step up transformer is eliminated. The most important difference is that the inverter is supplied from high voltage so, the necessity of transformer is avoided. Also, the detailed design technique and component selection procedure have been given. A single lamp has been driven by the inverter, then the circuit was connected to drive 15'' LCD panel which has two lamps, therefore this purposed design has been modified because of the brightness uniformity problem which is very essential criteria for the end user.

The simulation results were compared to the experimental ones. The simulation results from PSPICE show a good agreement with the experimental measurements except the preheat mode, parasitic capacitance effect and component tolerances.

The efficiency of the circuit is not investigated yet. These cost and efficiency analyses are left as further work.

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APPENDICES

APPENDIX A. PROGRAMS FOR MAXIMUM VOLTAGE FREQUENCY

In this appendix, the lists of MATLAB package programs are given. By using these programs, the frequency corresponding to maximum voltage can be found as follows for series inverter, parallel inverter and series parallel inverter respectively.

For series inverter,

```
syms MVr Q W Wo MVr
MVr=1/sqrt(1+(Q*(W/Wo-Wo/W))^2);
diff(MVr,W)
ans=-1/(1+Q^2*(W/Wo-Wo/W)^2)^(3/2)*Q^2*(W/Wo-
Wo/W)*(1/Wo+Wo/W^2)
```

The frequency corresponding to maximum voltage is solved as follows;

```
S=solve('-1/(1+Q^2*(W/Wo-Wo/W)^2)^(3/2)*Q^2*(W/Wo-
Wo/W)*(1/Wo+Wo/W^2)=0',W)
```

For parallel inverter,

```
syms MVr Q W Wo MVr
MVr=1/sqrt((1-(W/Wo)^2)^2+(1/Q^2)*(W/Wo)^2);
diff(MVr,W)
ans=-1/2/((1-W^2/Wo^2)^2+1/Q^2*W^2/Wo^2)^(3/2)*((-
4+4*W^2/Wo^2)*W/Wo^2+2/Q^2*W/Wo^2)
```

The frequency corresponding to maximum voltage is solved as follows;

```
S=solve('-1/2/((1-W^2/Wo^2)^2+1/Q^2*W^2/Wo^2)^(3/2)*((-
4+4*W^2/Wo^2)*W/Wo^2+2/Q^2*W/Wo^2)=0',W)
```

For series parallel inverter

```
syms MVr Q W Wo MVr A
MVr=1/sqrt((1+A)^2*(1-(W/Wo)^2)^2+(1/Q^2)*((W/Wo)-
(Wo/W)*(A/(A+1)))^2)
diff(MVr,W)
ans=-1/2/((1+A)^2*(1-W^2/Wo^2)^2+1/Q^2*(W/Wo-
Wo/W*A/(1+A))^2)^(3/2)*(-4*(1+A)^2*(1-W^2/Wo^2)*W/Wo^2+2/Q^2*(W/Wo-
Wo/W*A/(1+A))*(1/Wo+Wo/W^2*A/(1+A)))
```

The frequency corresponding to maximum voltage is solved as follows;

```
S=solve('-1/2/((1+A)^2*(1-W^2/Wo^2)^2+1/Q^2*(W/Wo-
Wo/W*A/(1+A))^2)^(3/2)*(-4*(1+A)^2*(1-W^2/Wo^2)*W/Wo^2+2/Q^2*(W/Wo-
Wo/W*A/(1+A))*(1/Wo+Wo/W^2*A/(1+A)))=0',W)
```

So maximum output can be obtained when W is equal to

```
1/6*2^(1/2)*3^(1/2)*(2*(-18*A^2*Q^4+60*A^3*Q^4+42*A^4*Q^4-
1+6*Q^2*A^2+12*Q^2*A+6*Q^2+8*Q^6*A^6+48*Q^6*A^5+120*Q^6*A^4+160
*Q^6*A^3+120*Q^6*A^2+48*Q^6*A+8*Q^6-12*Q^4-
48*Q^4*A+6*3^(1/2)*A*(8*Q^6*A^6+48*Q^6*A^5+15*A^4*Q^4+120*Q^6*A^4
+6*A^3*Q^4+160*Q^6*A^3+6*Q^2*A^2+120*Q^6*A^2-
45*A^2*Q^4+48*Q^6*A+12*Q^2*A-48*Q^4*A+8*Q^6-12*Q^4+6*Q^2-
1)^(1/2)*Q^2+6*3^(1/2)*A^2*(8*Q^6*A^6+48*Q^6*A^5+15*A^4*Q^4+120*Q^6
*A^4+6*A^3*Q^4+160*Q^6*A^3+6*Q^2*A^2+120*Q^6*A^2-
45*A^2*Q^4+48*Q^6*A+12*Q^2*A-48*Q^4*A+8*Q^6-12*Q^4+6*Q^2-
1)^(1/2)*Q^2)^(1/3)*Q^2*A^2+4*(-18*A^2*Q^4+60*A^3*Q^4+42*A^4*Q^4-
1+6*Q^2*A^2+12*Q^2*A+6*Q^2+8*Q^6*A^6+48*Q^6*A^5+120*Q^6*A^4+160
*Q^6*A^3+120*Q^6*A^2+48*Q^6*A+8*Q^6-12*Q^4-
48*Q^4*A+6*3^(1/2)*A*(8*Q^6*A^6+48*Q^6*A^5+15*A^4*Q^4+120*Q^6*A^4
+6*A^3*Q^4+160*Q^6*A^3+6*Q^2*A^2+120*Q^6*A^2-
45*A^2*Q^4+48*Q^6*A+12*Q^2*A-48*Q^4*A+8*Q^6-12*Q^4+6*Q^2-
1)^(1/2)*Q^2+6*3^(1/2)*A^2*(8*Q^6*A^6+48*Q^6*A^5+15*A^4*Q^4+120*Q^6
*A^4+6*A^3*Q^4+160*Q^6*A^3+6*Q^2*A^2+120*Q^6*A^2-
45*A^2*Q^4+48*Q^6*A+12*Q^2*A-48*Q^4*A+8*Q^6-12*Q^4+6*Q^2-
1)^(1/2)*Q^2)^(1/3)*Q^2*A+2*(-18*A^2*Q^4+60*A^3*Q^4+42*A^4*Q^4-
```

```
1+6*Q^2*A^2+12*Q^2*A+6*Q^2+8*Q^6*A^6+48*Q^6*A^5+120*Q^6*A^4+160
*Q^6*A^3+120*Q^6*A^2+48*Q^6*A+8*Q^6-12*Q^4-
48*Q^4*A+6*3^(1/2)*A*(8*Q^6*A^6+48*Q^6*A^5+15*A^4*Q^4+120*Q^6*A^4
+6*A^3*Q^4+160*Q^6*A^3+6*Q^2*A^2+120*Q^6*A^2-
45*A^2*Q^4+48*Q^6*A+12*Q^2*A-48*Q^4*A+8*Q^6-12*Q^4+6*Q^2-
1)^(1/2)*Q^2+6*3^(1/2)*A^2*(8*Q^6*A^6+48*Q^6*A^5+15*A^4*Q^4+120*Q^6
*A^4+6*A^3*Q^4+160*Q^6*A^3+6*Q^2*A^2+120*Q^6*A^2-
45*A^2*Q^4+48*Q^6*A+12*Q^2*A-48*Q^4*A+8*Q^6-12*Q^4+6*Q^2-
1)^(1/2)*Q^2)^(1/3)*Q^2+(-18*A^2*Q^4+60*A^3*Q^4+42*A^4*Q^4-
1+6*Q^2*A^2+12*Q^2*A+6*Q^2+8*Q^6*A^6+48*Q^6*A^5+120*Q^6*A^4+160
*Q^6*A^3+120*Q^6*A^2+48*Q^6*A+8*Q^6-12*Q^4-
48*Q^4*A+6*3^(1/2)*A*(8*Q^6*A^6+48*Q^6*A^5+15*A^4*Q^4+120*Q^6*A^4
+6*A^3*Q^4+160*Q^6*A^3+6*Q^2*A^2+120*Q^6*A^2-
45*A^2*Q^4+48*Q^6*A+12*Q^2*A-48*Q^4*A+8*Q^6-12*Q^4+6*Q^2-
1)^(1/2)*Q^2+6*3^(1/2)*A^2*(8*Q^6*A^6+48*Q^6*A^5+15*A^4*Q^4+120*Q^6
*A^4+6*A^3*Q^4+160*Q^6*A^3+6*Q^2*A^2+120*Q^6*A^2-
45*A^2*Q^4+48*Q^6*A+12*Q^2*A-48*Q^4*A+8*Q^6-12*Q^4+6*Q^2-
1)^(1/2)*Q^2)^(2/3)+4*A^4*Q^4+16*A^3*Q^4+24*A^2*Q^4-
4*Q^2*A^2+16*Q^4*A-8*Q^2*A+4*Q^4-4*Q^2+1-(-
18*A^2*Q^4+60*A^3*Q^4+42*A^4*Q^4-
1+6*Q^2*A^2+12*Q^2*A+6*Q^2+8*Q^6*A^6+48*Q^6*A^5+120*Q^6*A^4+160
*Q^6*A^3+120*Q^6*A^2+48*Q^6*A+8*Q^6-12*Q^4-
48*Q^4*A+6*3^(1/2)*A*(8*Q^6*A^6+48*Q^6*A^5+15*A^4*Q^4+120*Q^6*A^4
+6*A^3*Q^4+160*Q^6*A^3+6*Q^2*A^2+120*Q^6*A^2-
45*A^2*Q^4+48*Q^6*A+12*Q^2*A-48*Q^4*A+8*Q^6-12*Q^4+6*Q^2-
1)^(1/2)*Q^2+6*3^(1/2)*A^2*(8*Q^6*A^6+48*Q^6*A^5+15*A^4*Q^4+120*Q^6
*A^4+6*A^3*Q^4+160*Q^6*A^3+6*Q^2*A^2+120*Q^6*A^2-
45*A^2*Q^4+48*Q^6*A+12*Q^2*A-48*Q^4*A+8*Q^6-12*Q^4+6*Q^2-
1)^(1/2)*Q^2)^(1/3))^(1/2)/(-18*A^2*Q^4+60*A^3*Q^4+42*A^4*Q^4-
1+6*Q^2*A^2+12*Q^2*A+6*Q^2+8*Q^6*A^6+48*Q^6*A^5+120*Q^6*A^4+160
*Q^6*A^3+120*Q^6*A^2+48*Q^6*A+8*Q^6-12*Q^4-
48*Q^4*A+6*3^(1/2)*A*(8*Q^6*A^6+48*Q^6*A^5+15*A^4*Q^4+120*Q^6*A^4
+6*A^3*Q^4+160*Q^6*A^3+6*Q^2*A^2+120*Q^6*A^2-
45*A^2*Q^4+48*Q^6*A+12*Q^2*A-48*Q^4*A+8*Q^6-12*Q^4+6*Q^2-
1)^(1/2)*Q^2+6*3^(1/2)*A^2*(8*Q^6*A^6+48*Q^6*A^5+15*A^4*Q^4+120*Q^6
*A^4+6*A^3*Q^4+160*Q^6*A^3+6*Q^2*A^2+120*Q^6*A^2-
45*A^2*Q^4+48*Q^6*A+12*Q^2*A-48*Q^4*A+8*Q^6-12*Q^4+6*Q^2-
1)^(1/2)*Q^2)^(1/6)*Wo/(1+A)/Q
```

APPENDIX B THD ANALYSIS PROGRAM FOR THD

In this appendix the MATLAB package program is given for THD. By using this program it is possible to see the variation of THD with respect to the quality factor and pulse width.

For series inverter to analyze effect of quality factor, the following commands are used.

```
V=1;Wo=60000;W=60000;
Q=0;B=pi;
THD=zeros(1,10);
while Q<10
  Q=Q+1;
Vi=zeros(1,100);
Vo=zeros(1,100);
%assume that VDC=2(1,-1)
Vi(1)=((2*sqrt(2)*V)/pi)*sin(B/2);
n=2;
while n<101
   Vi(n)=((2*sqrt(2)*V)/(n*pi))*sin((n*B)/2);
   n=n+1;
end
Vi;
n=1;
while n<101
   Vo(n)=Vi(n)*(1/sqrt(1+(Q*((n*W)/Wo-Wo/(n*W)))^2));
   n=n+1;
end
Vor=Vo(1);
Vo(1)=0;
THD(Q)=(sqrt(sum(Vo.*Vo)))/Vor;
```

```
end
plot(THD)
xlabel('quality factor');
ylabel('THD')
title('Q-THD for series inverter')
```

For series inverter to analyze effect of pulse width, the following commands are used.

```
V=1;Wo=60000;W=60000;
Q=5;B=pi;
THD=zeros(1,10);a=0;
while a<100
   a=a+1;
   B=(pi*a)/100;
Vi=zeros(1,100);
Vo=zeros(1,100);
%assume that VDC=2(1,-1)
Vi(1)=((2*sqrt(2)*V)/pi)*sin(B/2);
n=2;
while n<101
   Vi(n)=((2*sqrt(2)*V)/(n*pi))*sin((n*B)/2);
   n=n+1;
end
Vi;
n=1;
while n<101
   Vo(n)=Vi(n)*(1/sqrt(1+(Q*((n*W)/Wo-Wo/(n*W)))^2));
   n=n+1;
end
Vor=Vo(1);
Vo(1)=0;
```

```
THD(a)=(sqrt(sum(Vo.*Vo)))/Vor;
end
n=0.5:0.5:50;
plot(n,THD)
xlabel('Pulse Width(%)');
ylabel('THD')
title('PW-THD for series inverter')
```

For parallel inverter to analyze effect of quality factor, the following commands are used.

```
V=1;Wo=60000;W=60000;
Q=0;B=pi;
THD=zeros(1,10);
while Q<10
  Q=Q+1;

Vi=zeros(1,100);
Vo=zeros(1,100);
%assume that VDC=2(1,-1)
Vi(1)=((2*sqrt(2)*V)/pi)*sin(B/2);
n=2;
while n<101
   Vi(n)=((2*sqrt(2)*V)/(n*pi))*sin((n*B)/2);
   n=n+1;
end
Vi;
n=1;
while n<101
   Vo(n)=Vi(n)*(1/sqrt((1-((n*W)/Wo)^2)^2+(1/Q^2)*((n*W)/Wo)^2));
   n=n+1;
end
```

```
Vor=Vo(1);
Vo(1)=0;
THD(Q)=(sqrt(sum(Vo.*Vo)))/Vor;
end
plot(THD)
xlabel('quality factor');
ylabel('THD')
title('Q-THD for parallel inverter')
```

For parallel inverter to analyze effect of pulse width, the following commands are used.

```
V=1;Wo=60000;W=60000;
Q=5;B=pi;
THD=zeros(1,10);a=0;
while a<100
   a=a+1;
   B=(pi*a)/100;
Vi=zeros(1,100);
Vo=zeros(1,100);
%assume that VDC=2(1,-1)
Vi(1)=((2*sqrt(2)*V)/pi)*sin(B/2);
n=2;
while n<101
   Vi(n)=((2*sqrt(2)*V)/(n*pi))*sin((n*B)/2);
   n=n+1;
end
Vi;
n=1;
while n<101
   Vo(n)=Vi(n)*(1/sqrt((1-((n*W)/Wo)^2)^2+(1/Q^2)*((n*W)/Wo)^2));
```

```
    n=n+1;
end
Vor=Vo(1);
Vo(1)=0;
THD(a)=(sqrt(sum(Vo.*Vo)))/Vor;
end
n=0.5:0.5:50;
plot(n,THD)
xlabel('Pulse Width(%)');
ylabel('THD')
title('PW-THD for parallel inverter')
```

For series parallel inverter to analyze effect of quality factor, the following commands are used.

```
V=1;Wo=60000;W=60000;
Q=0;B=pi;A=1;
THD=zeros(1,10);
while Q<10
  Q=Q+1;

Vi=zeros(1,100);
Vo=zeros(1,100);
%assume that VDC=2(1,-1)
Vi(1)=((2*sqrt(2)*V)/pi)*sin(B/2);
n=2;
while n<101
    Vi(n)=((2*sqrt(2)*V)/(n*pi))*sin((n*B)/2);
    n=n+1;
end
Vi;
n=1;
```

```
while n<101
   Vo(n)=Vi(n)*(1/sqrt((1+A)^2*(1-((n*W)/Wo)^2)^2+(1/Q^2)*(((n*W)/Wo)-
(Wo/(n*W))*(A/(A+1)))^2));
   n=n+1;
end
Vor=Vo(1);
Vo(1)=0;
THD(Q)=(sqrt(sum(Vo.*Vo)))/Vor;
end
plot(THD)
xlabel('quality factor');
ylabel('THD')
title('Q-THD for series_parallel inverter')
```

For series parallel inverter to analyze effect of pulse width, the following commands are used.

```
V=1;Wo=60000;W=60000;
Q=5;B=pi;A=1;
THD=zeros(1,10);a=0;
while a<100
   a=a+1;
   B=(pi*a)/100;
Vi=zeros(1,100);
Vo=zeros(1,100);
%assume that VDC=2(1,-1)
Vi(1)=((2*sqrt(2)*V)/pi)*sin(B/2);
n=2;
while n<101
   Vi(n)=((2*sqrt(2)*V)/(n*pi))*sin((n*B)/2);
   n=n+1;
end
```

```
    Vi;
    n=1;
    while n<101
       Vo(n)=Vi(n)*(1/sqrt((1+A)^2*(1-((n*W)/Wo)^2)^2+(1/Q^2)*(((n*W)/Wo)-
(Wo/(n*W))*(A/(A+1)))^2));
       n=n+1;
    end
    Vor=Vo(1);
    Vo(1)=0;
    THD(a)=(sqrt(sum(Vo.*Vo)))/Vor;
    end
    n=0.5:0.5:50;
    plot(n,THD)
    xlabel('Pulse Width(%)');
    ylabel('THD')
    title('PW-THD for series_parallel inverter')
```