**DOKUZ EYLÜL UNIVERSITY**
**GRADUATE SCHOOL OF NATURAL AND APPLIED SCIENCES**

# LOW NOISE AMPLIFIER DESIGN AND OPTIMIZATION

**by**
**Oral Melih ALPAN**

**March, 2010**
**İZMİR**

# LOW NOISE AMPLIFIER DESIGN AND OPTIMIZATION

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## M.Sc THESIS EXAMINATION RESULT FORM

We have read the thesis entitled **"LOW NOISE AMPLIFIER DESIGN AND OPTIMIZATION"** completed by **ORAL MELİH ALPAN** under supervision of **ASST. PROF. DR. GÜLDEN KÖKTÜRK** and we certify that in our opinion it is fully adequate, in scope and in quality, as a thesis for the degree of Master of Science.

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**LOW NOISE AMPLIFIER**
**DESIGN AND OPTIMIZATION**

## ABSTRACT

Low noise amplifiers are key components in the receiving end of nearly every communication system. These systems require very weak signals at the input. Primary purpose of LNA is to amplify the weak signal while keeping noise as little as possible. Performance of LNA is measured most notably by its gain and noise figure. There are also other performance criteria's such as dynamic range, return loss and stability.

At the beginning of project we aimed to design an amplifier for RF signal of satellite silicone tuners. After some observation we decided to design a LNA which works between 950 MHz to 2.1 GHz with required gain and noise figure. First of all, we selected the required active amplifier component. We chose NXP BFG 425 RF transistor for this purpose. We designed a biasing circuit which works as stable as possible regardless of temperature and other environment effects. We designed matching circuits for both input and output of this transistor. We draw PCB according to RF design requirements. After getting first measurements, we used AWR Microwave office for optimization of circuit to reach target design spec.

**Keywords:** LNA, amplifier, noise, radio frequency

# DÜŞÜK GÜRÜLTÜLÜ GÜÇLENDİRİCİ TASARIM VE OPTİMİZASYONU

## ÖZ

Düşük gürültülü güçlendiriciler birçok iletişim sisteminin girişindeki anahtar elemanlardır.Bu sistemler girişlerinde düşük seviyede sinyaller isterler.Düşük gürültülü güçlendiricilerin asıl amacı gürültüyü mümkün olduğunca düşük tutarak bu sinyalleri güçlendirmektir. Düşük gürültülü güçlendiricilerin performansı en çok kazanç ve gürültü oranları ile ölçülür. Bunların dışında dinamik aralığı , kararlılığı ve dönüş kaybı gibi kriterler de vardır.

Tez başlangıcında silikon tunerlerin girişindeki sinyaller için güçlendirici yapmayı hedefledik.Yaptığımız birkaç araştırmadan sonra 950Mhz ile 2.1Ghz arasında gerekli kazanç ve gürültü oranı ile çalışacak bir düşük gürültülü güçlendirici yapmaya karar verdik.Öncelikle güçlendirici için gerekli olan aktif malzemeyi seçtik.Amacımız için NXP nin BFG425 RF transistörünü seçtik.Sıcaklık ve diğer çevresel etkenlerden etkilenmeden mümkün olduğunca kararlı çalışacak bir tetikleme devresi tasarladık.Transistörün giriş ve çıkışı için eşleştirme devreleri tasarladık.RF dizayn gereksinimlerine göre baskı devre tasarladık.İlk sonuçları aldıktan sonra AWR Microwave office programını kullanarak hedeflediğimiz dizayn özellikleri için devreyi optimize ettik.

**Anahtar sözcükler:** Düşük gürültülü güçlendirici, güçlendirici, gürültü, radyo frekansı

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# CHAPTER ONE
# INTRODUCTION

Due to developing technology the use of Radio Frequency (RF) and microwave receivers has increased in the 21st century. These receivers are for example used in cordless telephones, cellular phones, wireless local area networks (WLAN) and in satellite downlinks. Satellite receivers, is the one of interest in this report. The entire satellite system, as shown in figure 1.1 consist of a satellite dish, an antenna, a low noise block (LNB), a coaxial cable and an integrated receiver decoder (IRD). The LNB is a combination of a block down converter and a low noise amplifier (LNA). The combination of an LNB and a feed horn is referred to as an LNBF.

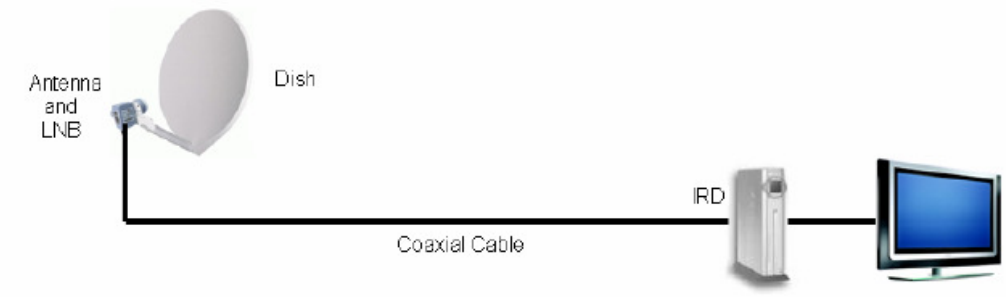


Figure 1.1 Satellite receiver systems

LNA is placed at the front end of a receiver system, following the antenna. Low noise amplifier (LNA) is usually preceded by a band pass filter which filters the out of band signals while allowing the in band signals to pass through. Hence, the LNA forms the first block that amplifies the desired band of signals without adding significant noise to the signal. The LNA receives the entire in band of signals with the out of band signals sufficiently suppressed.

Frequency spectrum for satellite video broadcasting is between 950MHz to 2.15GHz. The signal is subjected to interference from various out of channel signals operating within the band of interest and various out of band signals. Some frequencies within this range correspond with today's communication technologies

such as UMTS. This combined with the numerous other coexisting standards place stringent requirements on the RF receiver front end design. Thus the receiver should be able to sufficiently suppress the interference signals and process the desired channel of interest.

The LNA is a non linear device and generates various frequency components few of which affect the input signal. This nonlinear characteristic results in two important problems namely “Blocking” and “Intermodulation”. A weak input signal accompanied by a strong in band interferer (neighbor channel for instance) tends to reduce the gain of LNA and desensitize the circuit.

Another interesting problem that occurs in nonlinear circuits is “Intermodulation”. When two strong in band interferers appear at the input, the circuit nonlinearities result in intermodulation components which fall on the signal of interest thus corrupting the input signal.

But in today’s video broadcasting environment, due to the problems involving interferers described above, the LNA should also be able to suppress the interferers without which the following mixer block encounters a much larger interferer and thus demanding much higher performance from it in terms of linearity and trading off on its other specifications like conversion gain. Thus an LNA that achieves high levels of linearity and consequently high IIP3 are desired. But the main function of an LNA is to achieve high gain without adding significant noise (less NF) to the signal.

Using an LNA, the noise of all the subsequent stages is reduced by the gain of the LNA, while the noise of the LNA itself is injected directly into the received signal. Thus, it is necessary for an LNA to boost the desired signal power while adding as little noise and distortion as possible so that the retrieval of this signal is possible in the later stages in the system. The low noise amplifier (LNA) is the first gain stage in the receiver path. Therefore, according to Friis’ formula, the noise figure (NF) of this circuit directly adds to that of the overall system. The noise figure is a measure of the

degradation of the signal to noise ratio (SNR) at the output of the LNA compared to that at the input. Another main performance parameter of the LNA is its gain. The signal should be amplified as much as possible with hardly lowering the SNR, while also maintaining linearity. The last performance parameter is therefore represented by IP3. Obviously, the obtained NF, gain and IP3 should be within specification with minimum power consumption. This is the dilemma for an RF designer. The design specifications usually have to be met for a certain source and load impedance, while achieving minimum power consumption (Vaucher & Tang & Leenaerts, 2001).

The objective of this thesis is to design a low noise amplifier working at UMTS frequency that achieves high IIP3 in the order of 20dBm without sacrificing gain and NF. LNA should also cover whole digital video satellite band which is between 950MHz to 2.15GHz.

If there is interference in integrated receiver decoder at UMTS frequency (1900MHz), we should keep our main antenna input signal stronger then interfering signal. By this way, we can decrease and overcome the negative effects of interfering signal.

### 1.1 Literature Review

Jayaraman, K. (2009) designed a 2.4 GHz, reconfigurable RF low loise amplifier (LNA) using on chip peak detection and calibration, to mitigate the deleterious effects of process, voltage and temperature (PVT) variations. The LNA can reconfigure its input impedance matching, as well as its gain. On chip detection of optimal input/output impedance matching is performed using an amplitude peak detector.

Wu, S.C. (2009) researched low noise amplifier of RF front end circuits for Ka band receiver being implemented on TSMC 0.18-μm CMOS technology. The low noise amplifier is implemented by a cascading two stages. The first stage is designed for low noise performance while the second stage is matched for high gain. The

circuit design by adding a series inductor between the CS and CG transistors to improve the transistors' fT for increasing the circuit's overall gain, and reducing the noise figure (NF).

Edwall, M. (2008) studied EISCAT_3D for four years time. The purpose of the study was to investigate the feasibility of a next generation incoherent scatter radar system. He designed a reciever front end, which include an LNA with high performance requirements. For that reason a MATLAB particle swarm optimization implementation was developed to interatively find a solution to optimal component values for a user definable LNA topology.

Aitha, V.R. & Imam, M.K. (2007) researched patch antenna and LNA for a "radio telescope system" working at 1.42 GHz. The main objective of this project is to design a two stage low noise amplifier for a radio telescope system, working at the frequency 1.42 GHz. The aim is to design a two stage LNA, match, connect and test together with patch antenna to reduce the system complexity and signal loss.

Sperling, M. (2003) researched wideband low noise amplifiers. He designed a wide band amplifier with 15dB gain and a 3dB bandwidth of 2.8GHz. This amplifier presented with SiGe Bipolar technology. This design has noise figure less then 4.4dB while dissipating only 16mW from a 2.5V supply.

Lucek, J. & Damen, R. (1999) designed a LNA for CDMA front end working at 1900MHz. They designed an LNA using Philips RF BFG400 series .They achieved low supply voltage ( Vce = 2V ) , low current consumption ( Ic=10mA ) , high gain (15 dB) , low noise figure ( NF = 2dB ) , unconditional stability , 10 dB input return loss, high isolation , small dimension and low cost.

Content of the thesis can be summarized briefly as follows;

Chapter two contains basic radio frequency concept. Reflection, scattering parameters, smith chart and impedance matching methods are explained.

Chapter three describes low noise amplifier design strategies. Target specifications, active device selection, impedance matching and maximum gain theories are explained.

Chapter four consists of design procedures. Initial design, simulation results, optimized circuit and test board measurements are explained. Some constraints we have faced during design are showed. To get rid of these constraints alternative ways are explained. Also, some viable improvements are given to make the design more efficient.

Chapter five concerned with conclusion.

# CHAPTER TWO
# RADIO FREQUENCY CONCEPT

## 2.1 Reflection

As a power wave travels through an impedance discontinuity, a fraction of the wave will be reflected at that junction. By this way the counterpart (the incident wave) will lose some of its magnitude. Naturally, if power conservation is critical this is an undesirable phenomenon. The extent of power loss in incident wave is related to the similarity of the impedances as seen in both directions from the junction. In order to maximize the power transfer, designer should optimize the impedance match. There are number of performance parameters that are related to impedances matching. Firstly, the reflection coefficient, which is the ratio of the reflected wave to the incident wave, but can also, is expressed in terms of impedances. It is a complex entity that describes both the magnitude of the reflection, and the phase shift.

$$\Gamma_L = \frac{\text{ReflectedWave}}{\text{IncidentWave}} = \frac{ZL - ZS}{ZL + ZS} \tag{2.1}$$

This is the load reflection coefficient with respect to the source impedance. It can be also expressed with respect to the characteristic impedance ($Z_0$). When the load is short circuited, maximum negative reflection occurs and the reflection coefficient assumes minus unity. In contrast, when the load is open circuited, maximum positive reflection occurs.

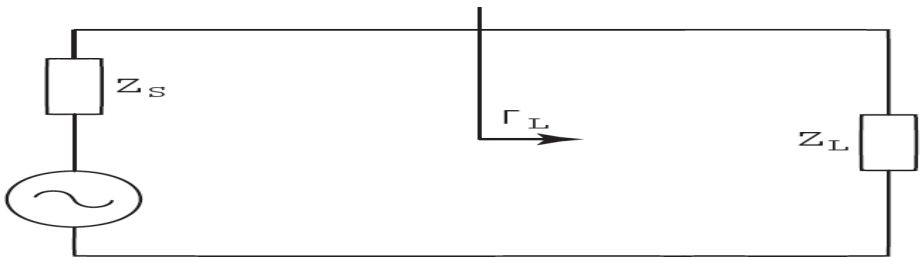


Figure 2.1 Simple circuit showing the impedance discontinuity junction and measurement location of $\Gamma_L$.

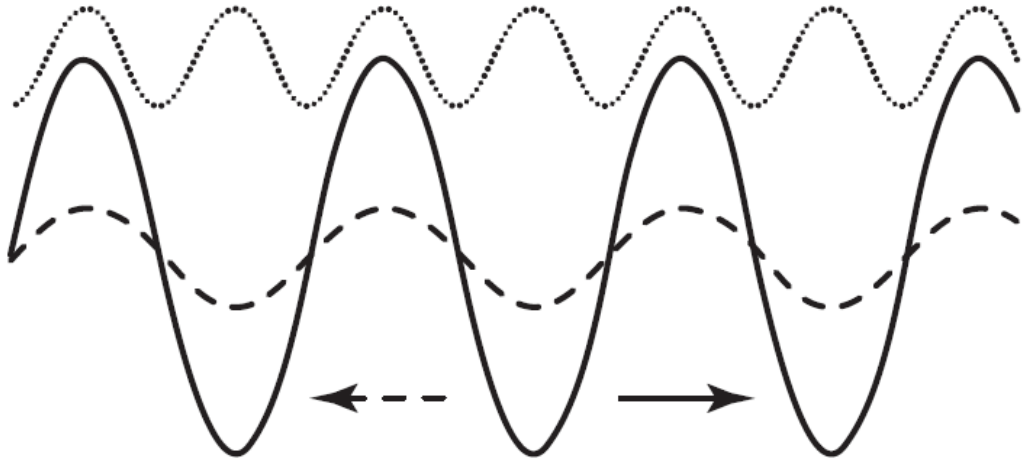

Figure 2.2 Incident wave (solid), reflected wave (dashed) and standing wave (dotted).

Reflection occurs and the reflection coefficient assumes plus unity. In the ideal case, if $Z_L$ is perfectly matched to $Z_S$, there is no reflection and the reflection coefficient is consequently zero.

A closely related parameter is the Voltage Standing Wave Ratio (VSWR). As the incident and reflected wave travel in opposite directions the addition of the two generates a standing wave, see Figure 2.2. The VSWR is defined as the ratio of the maximum voltage to the adjacent minimum voltage of that standing wave .If we know the domain of the reflection coefficient, it follows that when there is no reflection in a perfectly matched system; VSWR assumes its minimum and ideal value of 1.0:1.

$$\text{VSWR} = \frac{|V|\max}{|V|\min} = \frac{1+|\Gamma_L|}{1-|\Gamma_L|} \tag{2.2}$$

The Return Loss ($R_L$) is simply the magnitude of the reflection coefficient in decibels.

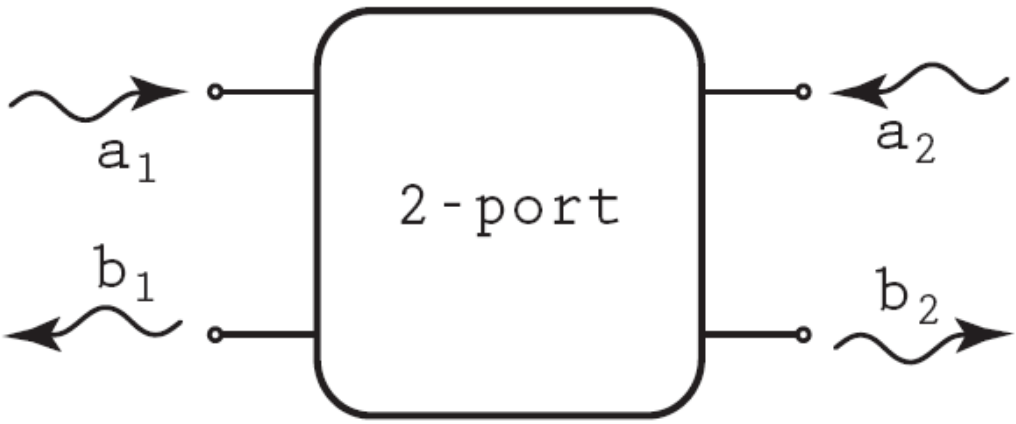


Figure 2.3 A 2-port with incident waves a1 and a2, and reflected waves b1 and b2.

It is specified that the return loss is measured on the input or output side of the Device Under Test (DUT), which corresponds IRL and ORL naming. It should be mentioned that the return loss is occasionally expressed without the leading minus sign ending up with a negative $R_L$. This is incorrect however as $R_L$ should be positive.

$$RL = -20\log|\Gamma L| \tag{2.3}$$

## 2.2 Scattering Parameters

Scattering Parameters or S parameters are complex numbers that help us to know how voltage waves propagate in the radio frequency (RF) environment. They characterize the complete RF behavior of a network in matrix form. At this point it is necessary to introduce the concept of 2 ports. It is fundamental in RF circuit analysis and simulation as it enables representation of networks by a single device. As we can effectively take out physical structure of the circuits from equations, circuit analysis is greatly simplified.

The characteristics of the 2 port is represented by a set of four S parameters: S11, S12, S21 and S22, which correspond to input reflection coefficient, reverse gain

coefficient, forward gain coefficient and output reflection coefficient respectively

There are alternative parameters for 2 ports, such as impedance parameters, admittance parameters, chain parameters and hybrid parameters. These parameters are measured on the basis of short and open circuit tests which are hard to realize at high frequencies. S parameters are measured under matched and mismatched conditions. This is why S parameters are favored in microwave applications. S parameters depend on both frequency and system impedance so although manufacturers typically supply S parameter data with their devices it is not always applicable. Under such circumstances, it becomes necessary to measure the parameters. Measurements are carried out by measuring wave ratios while systematically altering the termination to cancel either forward gain or reverse gain according to the following equations:

$$S_{11} = \frac{b1}{a1}\Bigg|_{a2=0} \tag{2.4}$$

$$S_{12} = \frac{b1}{a2}\Bigg|_{a1=0} \tag{2.5}$$

$$S_{21} = \frac{b2}{a1}\Bigg|_{a2=0} \tag{2.6}$$

$$S_{22} = \frac{b2}{a2}\Bigg|_{a1=0} \tag{2.7}$$

S parameters relate the four waves in the following fashion:

$$b_1 = S_{11}a_1 + S_{12}a_2 \tag{2.8}$$

$$b2 = S_{21}a_1 + S_{22}a_2 \tag{2.9}$$

## 2.3 Smith Chart

Smith Chart is one of the most useful graphical tools available to the rf circuit designer today. The chart was originally conceived back in the Thirties by a Bell Laboratories engineer named Phillip Smith. It is designed to find out an easier method of solving the tedious repetitive equations that often appear in rf theory. His solution, appropriately named the Smith Chart, is still widely in use (Bowick, 1997).

At first glance, the chart appears to be quite complex. Indeed, why would anyone even care to look at such a chart? The answer is really quite simple; once designer understands the chart and its uses, the rf circuit designer's job becomes much less tedious and time consuming. Very complex equations can be solved graphically on the chart in seconds, which lessens the possibility of errors creeping into the calculations.

The Smith Chart is a classic tool in RF engineering that has many uses and remains widely used although computers have become a convenient alternative. It is a fundamental aid in impedance matching network design and it serves as a standard for graphical presentation of impedance, reactance, stability circles, gain circles, noise circles etc.

The chart is made up out of two overlaid grids: the constant resistance circles and the constant reactance circles. The Cartesian coordinate system within the Smith Chart is used to plot the reflection coefficient. As the radius of the chart is unity, it is implied that all plotted values, whether they are impedances or admittances, must be normalized with respect to a reference. This reference is usually the characteristic impedance of the system which usually is 50 (Bowick, 1997).

$$z = \frac{Z}{Zo} \tag{2.10}$$

$$y = \frac{Y}{Yo} \tag{2.11}$$

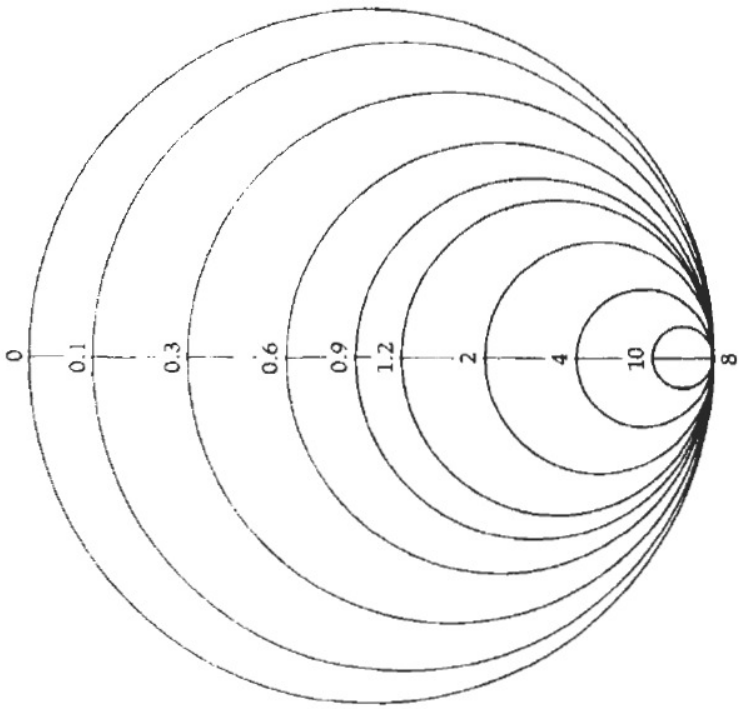


Figure 2.4 Constant resistance circles

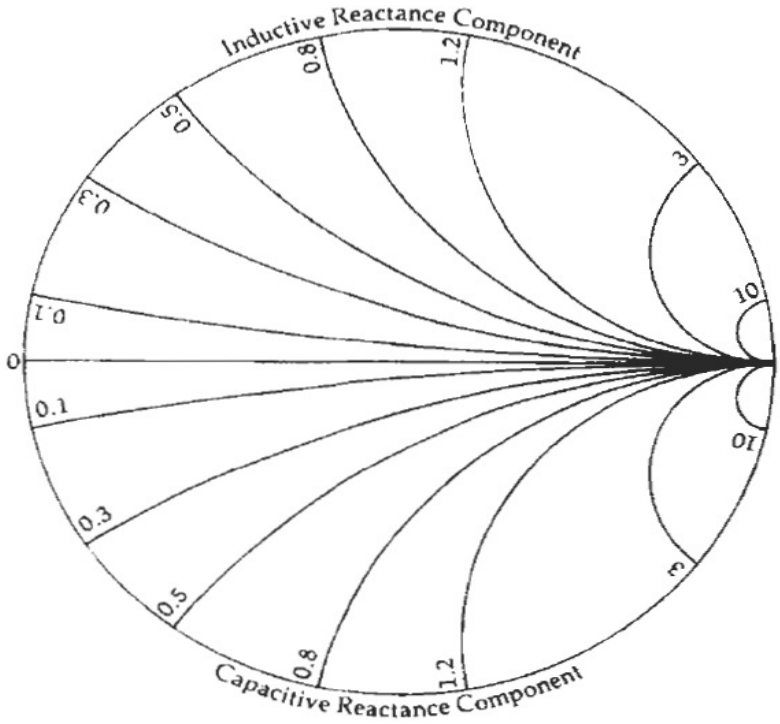


Figure 2.5 Constant reactance circles

Figure 2.5 is known as constant reactance circles, as each point on a circle has the same reactance as any other point on that circle. These circles are centered off of the

chart and, therefore, only a small portion of each is contained within the boundary of the chart. All arcs above the centerline of the chart represent +jX, or inductive reactance, and all arcs below the centerline represent -jX, or capacitive reactance. The centerline must, therefore, represent an axis where X = 0 and is, therefore, called the real axis. Notice in Fig. 2.4 that the "constant resistance =0" circle defines the outer boundary of the chart. As the resistive component increases, the radius of each circle decreases and the center of each circle moves toward the right on the chart. Then, at infinite resistance, you end up with an infinitely small circle that is located at the extreme right-hand side of the chart. A similar thing happens for the constant reactance circles shown in Fig. 2.5. As the magnitude of the reactive component increases ( -jX or +jX), the radius of each circle decreases, and the center of each circle moves closer and closer to the extreme right side of the chart. Infinite resistance and infinite reactance are thus represented by the same point on the chart. Since the outer boundary of the chart is defined as the "R = 0" circle, with higher values of R being contained within the chart, it follows then that any point outside of the chart must contain a negative resistance. The concept of negative resistance is useful in the study of oscillators and it is mentioned here only to state that the concept does exist, and if needed, the Smith Chart can be expanded to deal with it. When the two charts of Fig. 2.4 and 2.5 are incorporated into a single version and a few peripheral scales to aid us in other rf design tasks, such as determining standing wave ratio (SWR), reflection coefficient, and transmission loss along a transmission line.

### 2.3.1 Plotting Impedance Values

Any point on the Smith Chart represents a series combination of resistance and reactance of the form $Z = R \pm jX$ Z. Thus, to locate the impedance $Z = 1 + j1$, you would find the R = 1 constant resistance circle and follow it until it crossed the X = 1 constant reactance circle. The needed impedance value is represented by the junction of these two circles. This particular point, shown in Fig. 2.6, is located in the upper half of the chart because X is a positive reactance or an inductor. On the other hand, the point 1 - j l is located in the lower half of the chart because, in this instance, X is

a negative quantity and represents a capacitor. In general, then, to find any series impedance of the form $R \pm jX$ on a Smith Chart, you simply find the junction of the R = constant and X = constant circles.

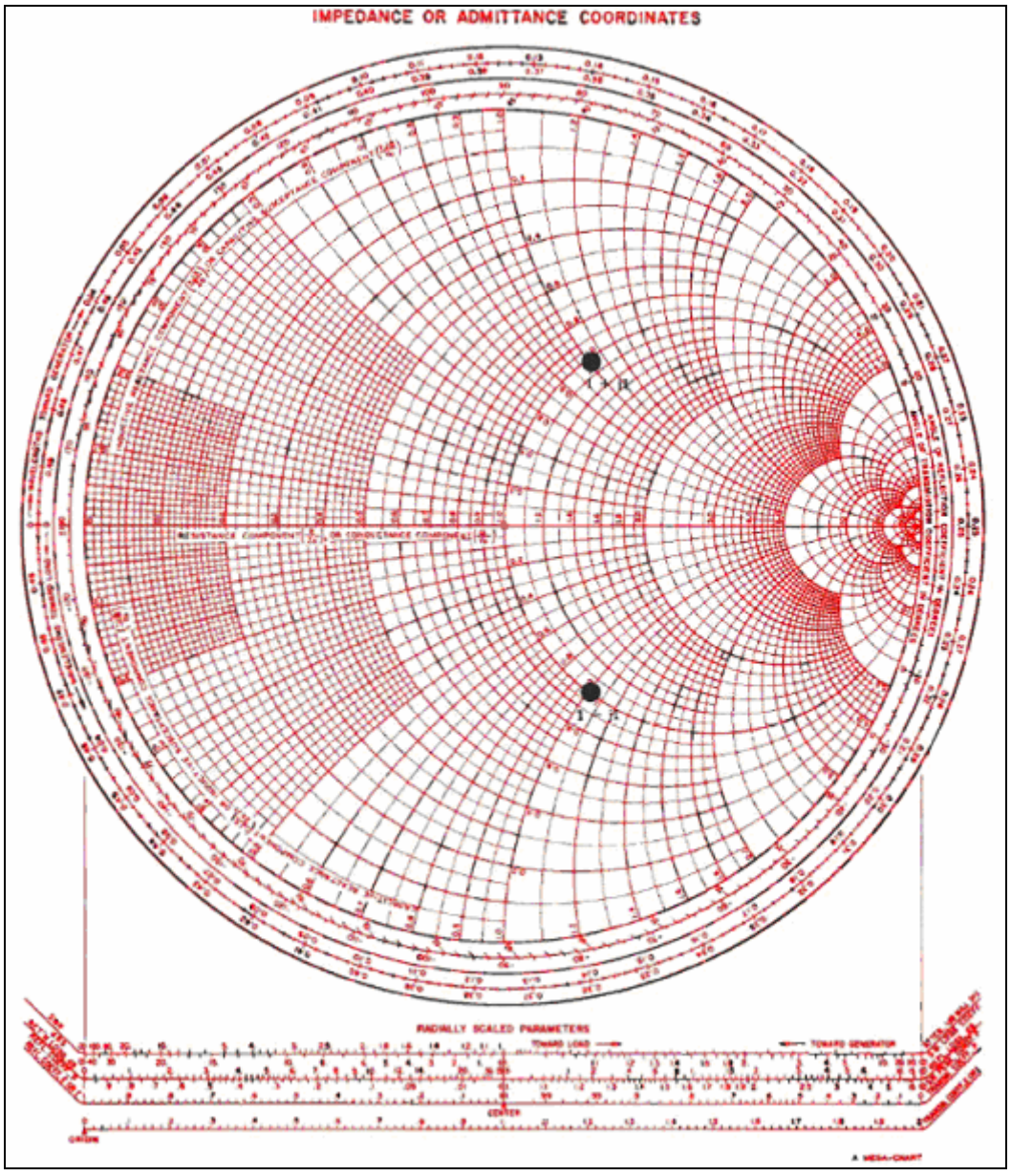


Figure 2.6 Representation of $1 \pm j1$ on the Smith Chart.

Indeed, if you try to plot an impedance of Z = 100 + jl50 ohms, you will not be able to do it accurately because the R = 100 and X = 150 ohm circles would be on the extreme right edge of the chart very close to infinity. In order to facilitate the plotting of larger impedances, normalization must be used. Impedance must be

divided by a convenient number that will place the new normalized impedance near the center of the chart to obtain increased accuracy in plotting. Thus, for the preceding example, where Z = 100 + j150 ohms, it would be convenient to divide Z by 100, which yields the value Z = 1 + j1.5.

### *2.3.2 Impedance Matching On the Smith Chart*

It is easy to add series and shunt components by ladder type arrangements on smith chart while easily keeping track of the impedance as seen at the input terminals of the structure. By this way the chart seems to be an excellent candidate for an impedance matching tool. The idea here is simple. We have a given a load impedance and the impedance that the source would like to see, simply plot the load impedance and, then, begin adding series and shunt elements on the chart until the desired impedance is achieved.

### *2.3.3 Two Element Matching*

It is easy to design two element matching networks mathematically by using formulas. As a Smith Chart user, to make life much easier the following equations may be used.

For a series C component:

$$C = \frac{1}{\omega XN} \tag{2.12}$$

For a series L component:

$$L = \frac{XN}{\omega} \tag{2.13}$$

For a shunt C component:

$$C = \frac{B}{\omega N} \tag{2.14}$$

For a shunt L component:

$$L = \frac{N}{\omega B} \tag{2.15}$$

Where,

w = 2IIf,

X = the reactance as read from the chart,

B = the susceptance as read from the chart,

N = the number used to normalize the original impedances that are to be matched.

## 2.4 The Quality Factor

The Quality Factor (Q) is a descriptive parameter of the rate of energy loss in complete RLC networks. Q is a measurement of how lossy the component is, that is how much parasitic resistance on the design. In applications such as where loss is undesirable, high Q components are advantageous. Additionally the Q factor is directly related to the bandwidth. Higher Q corresponds to narrower bandwidth. The equations for calculating Q are:

$$Q_{RLC} = w\,\frac{Etot}{Pavg} \tag{2.16}$$

$$BW = \frac{w_0}{Q_{RLC}} \tag{2.17}$$

$$Q_L = \frac{X_L}{R} = \frac{wL}{R} \tag{2.18}$$

$$Q_C = \frac{|X_C|}{R} = \frac{1}{wCR} \tag{2.19}$$

## 2.5 Impedance Transformation

There are numerous matching networks that can be employed to facilitate impedance matching and coupling, and supply some filtering (normally of the low-pass variety) between RF stages as well. Matching allows the maximum power transfer and the attenuation of harmonics to be achieved between stages. Using one of the various topologies of LC circuits within a matching network is far less expensive, and can reach far higher frequencies, than the lumped transformer matching that was so popular in the past (Sayre, 2008).

In order to maximize power transfer from source to load, matching impedances is required. In a circuit as seen in Figure 2.8 where the source and load impedances are fixed, the purpose is to design the input matching network so that $Z_S$ matches $Z_1$ and the output matching network so that $Z_L$ matches $Z_2$. In other words $Z_1$ and $Z_2$ are transformed to match the input and output impedances of the transistor. According to the Maximum Power Transfer Theorem, the maximum power transfer will occur when the reactive components of the impedances cancel each other, which means that they are complex conjugates. This method is called conjugate matching.

To match network of passive components, there are primarily three options. First of them is the L match. Its advantage is the simplicity, but that is simultaneously its downside as well because it has only two degrees of freedom. Since there are only two component values to set, the L match is restricted to determining only two out of the three associated parameters: impedance transformation ratio, centre frequency and Q. We have to cascade another L match stage to achieve third degree of freedom. By this way we get another two types of impedance transformation matches: the Π match and the T match in Figure 2.8.

We don't get an additional degree of freedom with T and Π match configurations do not end with an additional degree of freedom but because of their topology they can absorb parasitic reactance present in source or load. Specifically the T match will absorb parasitic inductance whereas the Π match will absorb parasitic capacitance.

We can achieve significantly higher Q compared to an L match configuration. Another noteworthy impedance transformation option is band pass filtering where the port impedances are unequal.

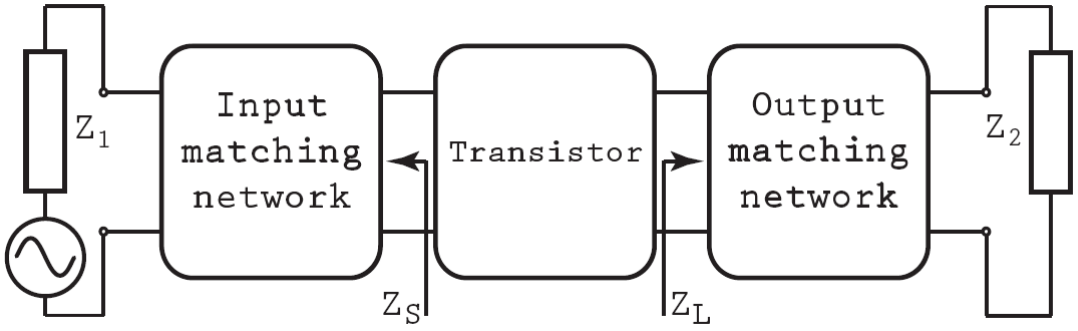


Figure 2.7 Matching networks in a microwave amplifier.

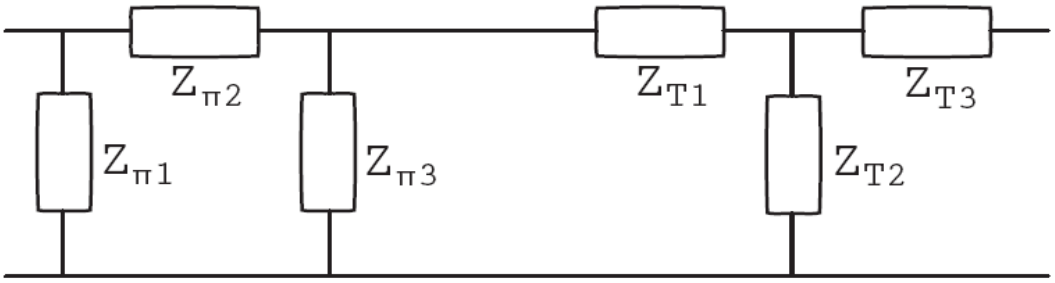


Figure 2.8 Cascaded Π- and T-matching networks

# CHAPTER THREE
# LOW NOISE AMPLIFIER DESIGN STRATEGY

## 3.1 Target Specifications

Small signal amplifiers are required to increase the small signal levels found at the input of a receiver into usable levels for the receiver's detector, or into the proper levels required of the final power amplifier of a transmitter.

A receiver's first RF amplifier has small signal, must have high gain type and must not produce excessive noise. Any noise generated within this first stage will be highly amplified by later stages which decreases the SNR.

As RF amplifiers are operating at high frequencies, they may sometimes be neutralized in order to counteract any possible positive feedback and its resultant self oscillations. Designing a system with a transistor that has unconditional stability at the frequency and impedance of operation is much more prevalent.

Transistors can also be completely characterized by their scattering or S parameters. It is possible to calculate potential instabilities, maximum available gain, input and output impedances, and transducer gain by these parameters. It is also possible to calculate optimum source and load impedances for a specified transducer gain. Firstly, it is better to choose a transistor, select a stable operating point, and determine its S parameters at that operating point by measurement or from a data sheet.

## 3.2 Active Device Selection

Since the data sheet is the dominant source of information circuit designers have for selecting an active device for their own specialized applications, it is especially

important to understand data sheet parameters as they apply to RF transistors (Sayre, 2008)

The properties of the active device are limiting factor for many parameters of the LNA. It is important to select an active device with parameters that correspond to and preferably exceed those of the target specifications. There are various active devices that are well suited for LNA applications. In the interest of limiting the scope of this thesis however, the device of choice is the NXP BFG425 RF Transistor.

### *3.2.1 Description of NXP BFG425 Wideband RF Transistor*

NPN double polysilicon wide band transistor with buried layer for low voltage applications in a plastic, 4-pin dual-emitter SOT343R package.

### *3.2.2 Features of the Transistor*

· Very high power gain
· Low noise figure
· High transition frequency
· Emitter is thermal lead
· Low feedback capacitance.

### *3.2.3 Application Areas of the Transistor*

· RF front end
· Wideband applications, e.g. analog and digital cellular telephones, cordless telephones (PHS, DECT, etc.)
· Radar detectors
· Pagers
· Satellite television tuners (SATV)

· High frequency oscillators.

Quick reference data of BFG425 RF transistor can be found at Appendix A at the end of the thesis.

### 3.3 DC Bias Network Design

In amplifier designs, very little thought is ever given to the design of bias networks for the individual transistors involved. Often, the lack of interest in bias networks may be justified. If the amplifier is to be operated only at room temperature, there would be little need to spend much time developing an extremely temperature stable dc operating point.

When a transistor's bias point changes it affects all of its rf operating characteristics. It only stands to reason, then, that the dc operating point must remain stable under your specified operating conditions. It has been shown that there are two basic internal transistor characteristics that have a profound effect upon the transistor's dc operating point over temperature; they are ΔVBE and Δβ. The object of a good temperature stable bias design is to minimize the effects of these parameters.

The total change in ΔBE for a given temperature change is called ΔVBE**.** The primary external circuit factor that the circuit designer has control over, and which tends to minimize the effects of ΔVBE**,** is the emitter voltage **($V_E$)** of the transistor.
If these observations were put into equation form, we would have:

$$\Delta I_C \approx -\frac{\Delta V_{BE} I_C}{V_E} \tag{3.1}$$

where,

$\Delta I_C$ = the change in collector current,

$\mathbf{I_C}$ = the quiescent collector current,

**ΔVBE** = the change in base-to-emitter voltage,

$\mathbf{V_E}$ = the quiescent emitter voltage.

Thus, if VE were made equal to 20 times ΔVBE**,** the collector current would change only *5%* over temperature due to ΔVBE. It is important to note that it is the value of the emitter voltage ($V_E$) and not the value of the emitter resistor ($R_E$) that is the important bias design criteria.

The change in a transistor's dc current gain, or β**,** over temperature, is also of importance to the circuit designer. Not only does β vary with temperature, but the manufacturing tolerance for β among transistors of the same part number is typically very poor. Thus, a stable operating point with respect to β is difficult to obtain from a production standpoint as well as from a temperature standpoint.

The change in collector current for a corresponding change in β can be approximated as:

$$\Delta I_C = I_{C1}\left(\frac{\Delta\beta}{\beta_1\beta_2}\right)\left(1+\frac{R_B}{R_E}\right) \tag{3.2}$$

Where,

$I_{C1}$ = the collector current at $\beta = \beta_1$,

$\beta_1$ = the lowest value of β ,

$\beta_2$ = the highest value of β ,

$\Delta\beta = \beta_2 - \beta_1$

$R_B$ = the parallel combination of $R_1$ and $R_2$

$R_E$ = the emitter resistor.

This equation indicates that once a transistor is specified, the only control that the designer has over the effect of β changes on collector current is through the resistance ratio $R_B/R_E$. The smaller this ratio, the less the collector current varies. Again, however, some compromise is necessary. As you decrease the ratio $R_B/R_E$**,**

you also produce the undesirable effect of decreasing the current gain of the amplifier. Also, as the ratio approaches unity, the improvement in operating point stability rapidly decreases. As a practical rule of thumb for stable designs, the ratio $R_B/R_E$, should be less than 10.

Similar bias arrangements and design procedures for a field-effect transistor (FET).These are based on the well-known formula:

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2 \tag{3.3}$$

Where,

$I_D$ = the drain current

$I_{DSS}$ = the drain current with VGS = 0,

$V_{GS}$ = the gate to source voltage,

$V_P$ = the pinch – off voltage

$I_D$ is usually a value chosen by the user as part of the bias specifications, and $I_{DSS}$ and $V_P$, can be found on the data sheet for the transistor. Once these three values are known, equation below can be used to solve for $V_{GS}$, and a suitable bias circuit can then be found.

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2 \tag{3.4}$$

### 3.4 Matching Network Design

As we find a suitable stable transistor, and its gain capabilities have been found to match our requirements, we can proceed with the design. This design procedure will result in load and source reflection coefficients which will provide a conjugate match for the actual output and input impedances of the transistor. The actual output impedance of a transistor is dependent upon the source impedance that the transistor sees. The actual input impedance of the transistor is dependent upon the load

impedance that the transistor sees. This dependency is directly related to reverse gain of the transistor ($S_{12}$). If $S_{12}$ equals to zero, then, the load and source impedances have no effect on the transistor‘s input and output impedances.

### *3.4.1 Determining ΓL*

Perform the following calculations to find the desired load reflection coefficient for a conjugate match:

$$C_2 = S_{22} - ( D_S S_{11}^{\circ} ) \tag{3.5}$$

Where, the asterisk indicates the complex conjugate of $S_{11}$ (same magnitude, but angle has the opposite sign). The quantity $D_S$ is the intermediate quantity. Next, calculate $B_2$.

$$B_2 = 1 + |S_{22}|^2 - |S_{11}|^2 - |D_S|^2 \tag{3.6}$$

The magnitude of the reflection coefficient is then found from the equation:

$$|\Gamma_L| = \frac{B_2 \pm \sqrt{B_2^{\,2} - 4|C_2|^2}}{2|C_2|} \tag{3.7}$$

The sign preceding the radical is the opposite of the sign of $B_2$. The angle of the load reflection coefficient is simply the negative of the angle of $C_2$.

### *3.4.2 Determining ΓS*

As we find the desired load reflection coefficient, it can be plotted on a Smith Chart, and the corresponding load impedance can be found directly. Or we can substitute $\Gamma_L$, into equation and solve for $Z_L$, mathematically. With the calculated load reflection coefficient we can now find the source reflection coefficient that is needed to properly terminate the transistor's input.

$$\Gamma_S = \left[ S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1-(\Gamma_L \bullet S_{22})} \right]^* \tag{3.8}$$

The asterisk again indicates that we should take the conjugate of the quantity in brackets (same magnitude, but opposite sign for the angle). As we complete the calculation, the magnitude of the result will be correct, but the angle will have the wrong sign. Simply change the sign of the angle. As $\Gamma_S$ is found, it can either be plotted on a Smith Chart or substituted into equation to find the corresponding source impedance.

## 3.5 Gain

### *3.5.1 P1dB and IP3*

In a no signal DC condition or under a maximum signal situation. Obviously, the transistor's *fT,* P1dB, and *GA* (MAX) (maximum available gain) and, for low-noise amplifier (LNA) applications, the NF, are all vital specifications. The near maximum output power possible in an amplifier is the 1-dB compression point (P1dB). This is the area where a linear amplifier begins to run out of room for its maximum output voltage swing. Any amplifier will have what is generally considered as a linear *P*OUT until it reaches this P1dB point, which occurs when a high enough input signal is injected into the amplifier's input. At P1dB, the gain of the amplifier will depart from the gain displayed at lower input powers, and for every decibel placed at the amplifier's input; no longer will there be a linear amplification of the signal. The output gain slope flattens, and soon no significant increase in output power is possible.

When an amplifier is below its P1dB, then for every 1-dB increase in fundamental power into the amplifier, the output second-order products will increase by 2 dB, while the output third-order products will increase by 3 dB. The reverse is also true. For every 1 dB decrease in the fundamental input power, the second and third orders

decrease in power by 2 and 3 dB, respectively. However, by increasing the desired input signals, there will reach some point where the third-order products must be (theoretically) equal to the fundamental outputs. This is the third-order intercept point (TOIP). The third-order intercept point is approximately 10 to 15 dB above the P1dB compression point. The TOIP is the point where, when two different (but closely spaced in frequency) input signals are placed at the amplifier's input port, the undesired output third-order products will be at the same amplitude as the desired two-tone fundamental input signals. However, the output TOIP itself can never actually be reached. This is because the amplifier will go into saturation before this amplitude is ever truly attained. Even though Fig. 3.1 does not show it, the third-order product's output power will gain-limit, just as the fundamental signal must, when the amplifier goes into saturation.

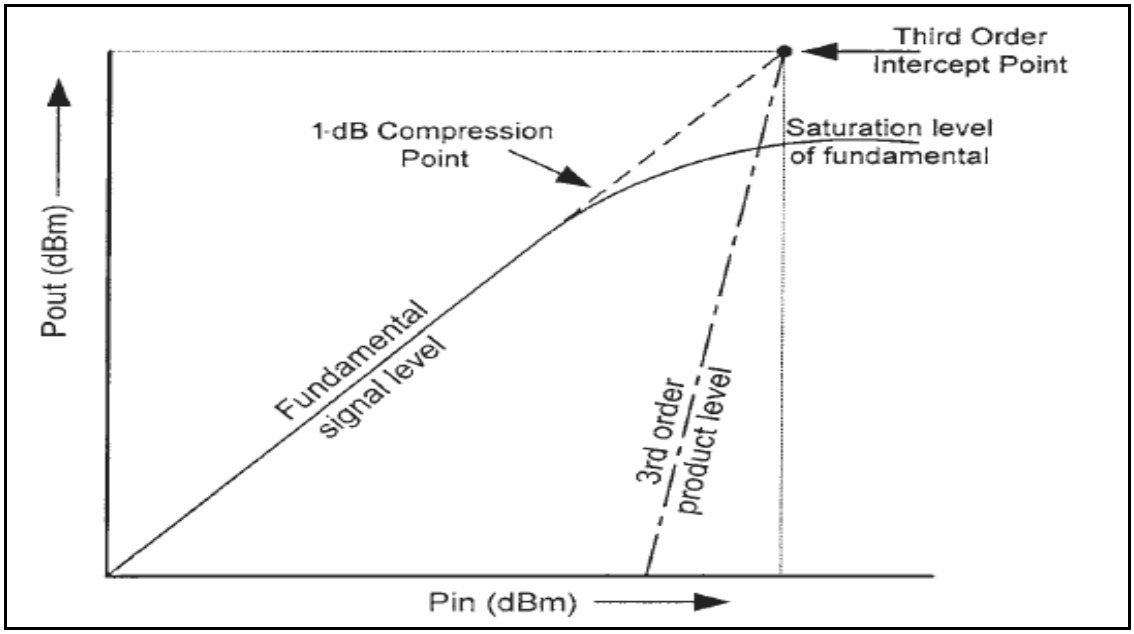


Figure 3.1 The third order intercept and 1dB compression points.

### *3.5.2 Maximum Available Gain*

A transistor amplifier provides the maximum available power gain, when both ports are conjugately matched. This condition can be written as: (Lehto & Raisanen, 2003).

$$q_{in} = q_s{}^{*} \text{ and } q_{out} = q_L{}^{*} \tag{3.9}$$

The maximum gain we can achieve from a transistor under conjugate matched conditions is called the Maximum Available Gain (MAG). To calculate MAG, first calculate the intermediate quantity $B_1$:

$$B_1 = 1 + |S_{11}|^2 - |S_{22}|^2 - |D_S|^2 \tag{3.10}$$

The MAG is then calculated:

$$MAG = 10\log\frac{|S_{21}|}{|S_{12}|} + 10\log\left|K \pm \sqrt{K^2 - 1}\right| \tag{3.11}$$

MAG is in dB, K is the stability factor. The reason $B_1$ had to be calculated first is because its polarity determines sign. If $B_1$ is negative, use the plus sign. If $B_{1,}$ is positive, use the minus sign. K must be greater than 1 for unconditional stability. If K is less than 1, the radical in the equation will produce an imaginary number and the MAG calculation is no longer valid. MAG is undefined for unstable transistors.

### *3.5.3 Transducer Gain*

The transducer gain is the actual gain of an amplifier stage including the effects of input and output matching and device gain. It does not include losses attributed to power dissipation in imperfect components.

Transducer gain is found by

$$G_T = \frac{|S_{21}|^2\left(1 - |\Gamma_S|^2\right)\left(1 - |\Gamma_L|^2\right)}{\left|(1 - S_{11}\Gamma_S)(1 - S_{22}\Gamma_L) - S_{12}S_{21}\Gamma_L\Gamma_S\right|^2} \tag{3.12}$$

Where, $\Gamma_S$ and $\Gamma_L$ are the source and load reflection coefficients, respectively. Calculation of $G_T$ is a useful method of checking the power gain of an amplifier before it is built.

### 3.6 Noise Performance

The noise figure of any two port network is the measurement of the amount of noise that is added to a signal while transmitting through the network. For any practical circuit, the signal to noise ratio at its output will be worse than that at its input. In most of the applications, it is possible to minimize the noise contribution of each two port network through a judicious choice of operating point and source resistance. For each transistor, there exists an optimum source resistance necessary to establish a minimum noise figure. Many manufacturers specify an optimum source resistance on the data sheet.

In a microwave amplifier, even when there is no input signal, a small output voltage can be measured. We refer to this small output power as the amplifier noise power. The total noise output power is composed of the amplifier noise input power plus the noise output power produced by the amplifier. (Gonzalez, 1996)

Others will specify an optimum source reflection coefficient. There is just not enough space in a typical data book to provide the user with all of the information that he needs in order to design amplifiers at every possible frequency and bias point. The datasheet is meant only as a starting point in any design.

Designer should make many of his own measurements on a device before it becomes a part of the design. In the data sheet, you will find a set of curves labeled “Typical Optimum N.F. vs. Collector Current.” Designing amplifiers for a minimum noise figure depends on determining, experimentally or from the data sheet, the source resistance and the bias point that produce the minimum noise figure for the device.

Once determined, the actual source impedance is simply forced to look like the optimum value. Of course, we still have to apply all stability considerations. If the Rollett stability factor (K) calculates to be less than l, then you must be careful in your choice of source and load reflection coefficients.

First, draw the stability circles for an accurate graphical indication of where the unstable regions lie. After providing the transistor with its optimum source impedance, then determine the optimum load reflection coefficient needed to properly terminate the transistor's output. This is given by:

$$\Gamma_L = \left[ S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S} \right]^* \tag{3.13}$$

Where,

**Γs** is the source-reflection coefficient for minimum noise figure.

### 3.7 Stability

Unconditional stability of the amplifier circuit is the goal of the LNA designer. Unconditional stability means that with any load presented to the input or output of the device, the circuit will not become unstable, will not oscillate.

Unstable conditions are caused by three phenomena: internal feedback of the transistor, external feedback around the transistor caused by external circuit, or excess of gain at frequencies outside of the band of operation. For stability analysis of the transistor, S parameters provided by the manufacturer of the transistor should be checked.

There are two main methods for S parameter stability analysis: numerical and graphical. Numerical analysis consists of calculating a term called Rollett Stability Factor K. An intermitted quantity called delta (Δ) should be calculated first in order to simplify the final equation for the K factor.

$$\Delta = S_{11} * S_{22} - S_{21} * S_{12} \tag{3.14}$$

Then

$$K = \frac{1 + |\Delta|^2 - |S_{11}|^2 - |S_{22}|^2}{2 * |S_{21}| * |S_{12}|} \tag{3.15}$$

When the K factor is greater than unity, the circuit will be unconditionally stable for any combination of source and load impedance. When K is less than unity, the circuit is potentially unstable and oscillation may occur with a certain combination of source and/or load impedance presented to the transistor. The K factor is a key point for checking stability at given frequency and given bias condition. A sweep of the K factor over frequency for a given biasing point must be calculated to assure unconditional stability outside of the band of operation. The designer's aim is to design a LNA circuit that is unconditionally stable for the operating band where the device has a substantial gain.

We should also note that K is a pessimistic measure of stability for it allows arbitrary variations in the source and load impedances by the circuit. On the other hand, if the load impedance of an LNA is well defined, in a homodyne or image reject architecture, then stability is achieved by simply ensuring that the real part of the input impedance remains positive at all frequencies.(Razavi, 1998)

There are five common methods for designers to stabilize LNA circuit. The first one consists of resistive loading of the input. By this method, we improve the stability of the circuit but degrade the noise of the LNA and it is almost never used. Output resistive loading is another preferred method for circuit stabilization. This method should be carefully used because unexpected gain and P1dB point can be achieved. The third method uses collector to base R-L-C (resistor-inductor-capacitor) feedback in order to lower the gain at the lower frequencies and hence improve the stability of the circuit. The forth method consist of filter matching, usually used at the output of the transistor, in order to decrease the gain at a specific narrow bandwidth frequency. This method is used for eliminating gain at high frequencies,

which are above the band of operation. Short circuit quarter wave lines design for problematic frequencies or simple capacitors with the same resonant frequency as the frequency of oscillation can be employed to stabilize the circuit. The final stabilization method can be realized with a simple emitter feedback inductor. A small emitter inductor can make the circuit more stable at higher frequencies for flat gain.

## 3.8 Center Frequency and Bandwidth

S-parameters of a transistor are dependent on frequency. Typically $S_{21}$ decreases at a rate of 20dB/decade as frequency increase and $S_{12}$ increases at the same rate with frequency.

$S_{11}$ and $S_{22}$ are also frequency dependent, this affect input and output matching. There is a degradation of noise figure and VSWR in some frequency range of the amplifier.

Basically the design of a constant gain amplifier over a broad frequency range is a matter of properly designing the matching networks, or feedback network to compensate for the variation of S parameters with frequency.

There are three common methods for this issue:

- (1) The use of compensated impedance matching networks.
- (2) The use of negative feedback.
- (3) Combining either (1) or (2) with the balanced design approach.

### *3.8.1 Compensated Impedance Matching*

A strategy of designing wideband amplifier using compensated impedance matching approach is to examine the expression for the transducer power gain.

$$G_T = \frac{\left(1-|\Gamma_L|^2|S_{21}|^2\left(1-|\Gamma_S|^2\right)\right)}{|1-S_{22}\Gamma_L|^2|1-\Gamma_L\Gamma_S|^2} \tag{3.16}$$

If we enforce Γs = 0 (i.e. make Zs = Zo), then

$$G_{TL} = \frac{\left(1-|\Gamma_L|^2|S_{21}|^2\right)}{|1-S_{22}\Gamma_L|^2} \tag{3.17}$$

A wideband impedance transformation network can then be designed to transform the load impedance $Z_L$ so that ΓL fulfills within the operating frequency band. For a fixed GT, the values of ΓL which fulfills a circle on the Smith chart. First we write:

$$\frac{G_{TL}\left(1-|S_{22}|^2\right)}{|S_{21}|^2} = g_L = \frac{\left(1-|\Gamma_L|^2\right)\left(1-|S_{22}|^2\right)}{|1-S_{22}\Gamma_L|^2} \tag{3.18}$$

$$|\Gamma_S - T_{GTL}|^2 = {R_{GTL}}^2 \tag{3.19}$$

$$T_{GTL} = \frac{g_L \,\mathrm{Re}(S_{22}*)}{1-(1-g_L)|S22|^2} + J\frac{g_L \,\mathrm{Im}(S_{22}*)}{1-(1-g_L)|S_{22}|^2} \tag{3.20}$$

$$R_{GTL} = \frac{\sqrt{1-g_L}\left(1-|S_{22}|^2\right)}{1-(1-g_L)|S_{22}|^2} \tag{3.21}$$

A few constant $G_{TL}$ circles will be plotted on the Smith chart for $\Gamma_L$ at different frequencies.

From these circles, suitable values of $Z_L$ will be identified at each frequency and a wideband impedance transformation network is designed to transform the actual load impedance at the designated frequency.

*3.8.1.1 Drawbacks of this Approach*

This method is limited to bandwidth of one decade. Considerable ripple is present within the operating bandwidth. The design of the required impedance transformation network is more of an art, largely a hit or miss affair. Power gain is not optimized. There is large amount of mismatch at the input and output. Power gain is sacrificed at the expense of wideband operation.

### *3.8.2 Negative Feedback*

Negative feedback is widely used in amplifier design for the following reasons:

– Negative feedback stabilizes the gain of the amplifier against parameter changes in the active device due to voltage variation, temperature drift or device aging.
– To increase the bandwidth of the amplifier (at the expense of maximum gain).

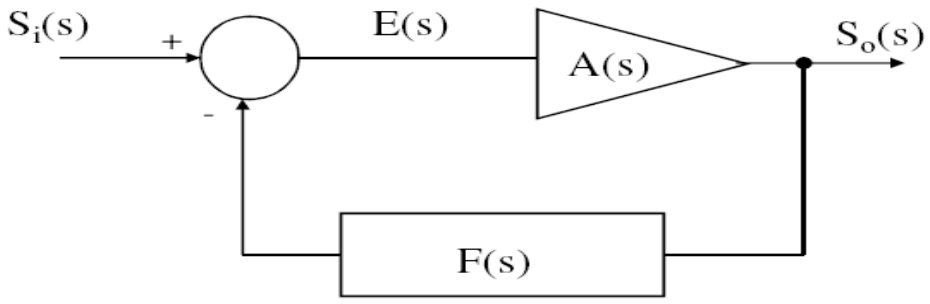


Figure 3.2 Negative feedback

$$\frac{S_0}{S_i}(S) = G(S) = \frac{A(S)}{1 + A(S)F(S)} \tag{3.22}$$

Closed Loop Gain

$$T(S) = A(S)F(S) \tag{3.23}$$

Loop Gain

**Properties of G(s):**

$$\frac{\Delta G(s)}{G(s)} = \frac{\frac{\Delta A(s)}{A(s)}}{1+T(s)}$$

Stabilization of gain against parameter variation

(3.24)

**If T(s)>>1** $\Longrightarrow$ $\frac{S_0}{S_i}(s) \cong \frac{1}{F(s)}$ (3.25)

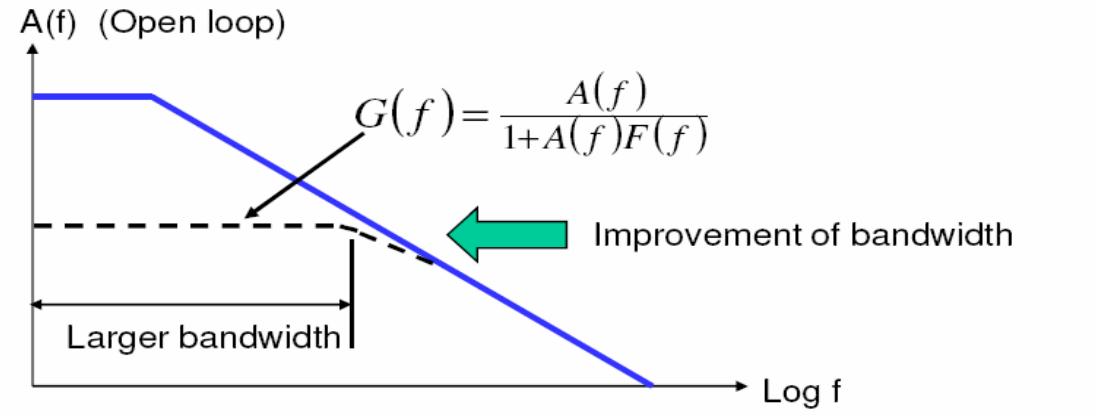


Figure 3.3 Gain versus Frequency

4 basic configurations of feedback system:

– Shunt-shunt feedback.

– Shunt-series feedback.

– Series-shunt feedback.

– Series-series feedback.

*3.8.2.1 Implementing Local Negative Feedback on Transistor and FET*

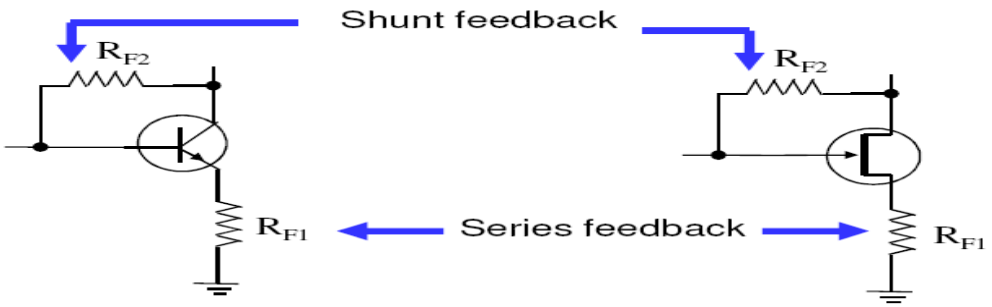


Figure 3.4 The shunt and series feedback can be implemented separately or together.

### 3.9 Inductive Source Degeneration

The purpose of degeneration is to provide a means to transform the real part of the impedance seen looking into the base to a higher impedance for matching purposes. This inductor also trades gain for linearity as the inductor is increased in size (Rogers & Plett, 2003).

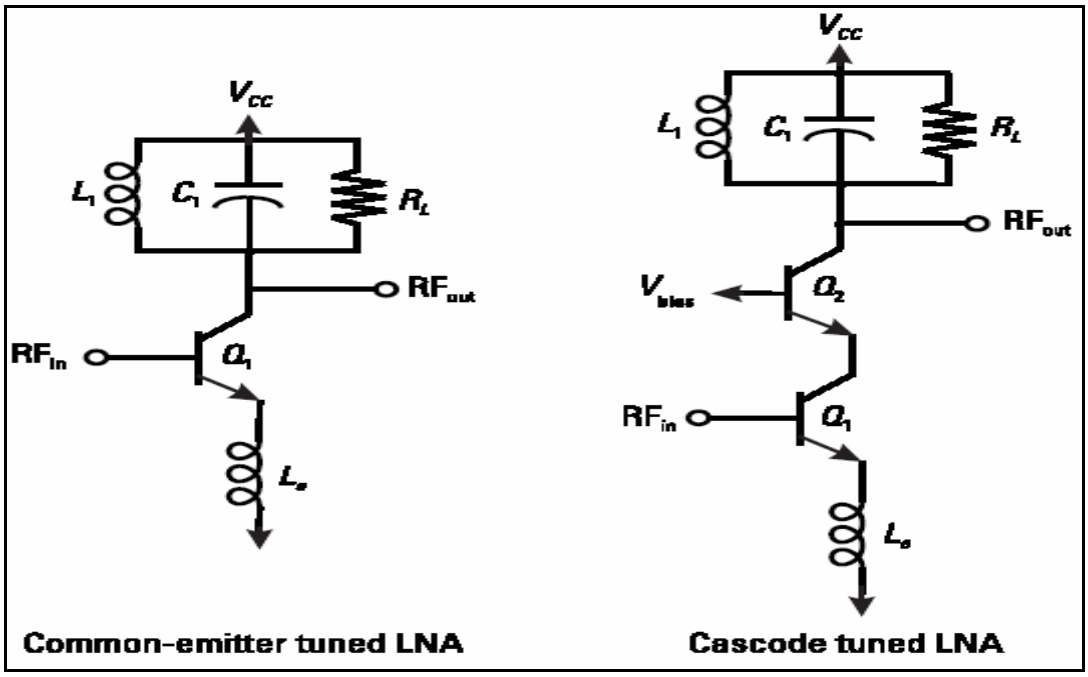


Figure 3.5 Narrowband common-emitter and cascade LNAs with inductive degeneration.

The gain of either amplifier at the resonance frequency of the tank in the collector, ignoring the effect of C m, is given by

$$\frac{v_{\text{out}}}{v_{\text{in}}} = \frac{-g_m R_L}{\left(1 + \frac{Z_E}{Z_\pi} + g_m Z_E\right)} \approx -\frac{R_L}{Z_E} \tag{3.26}$$

where ZE is the impedance of the emitter degeneration. Here it is assumed that the impedance in the emitter is complex impedance. Thus, as the degeneration becomes larger, the gain ceases to depend on the transistor parameters and becomes solely dependent on the ratio of the two impedances. This is, of course, one of the

advantages of this type of feedback. This means that the circuit becomes less sensitive to temperature and process variations.

If the input impedance is matched to RS (which would require an input series inductor), then the gain can be written out in terms of source resistance and fT . Vout in terms of can be given by

$$V_{out} = -g_m v_{\prod} R_L = -g_m i_x Z_{\prod} R_L \tag{3.27}$$

Noting that ix can also be equated to the source resistance RS as ix = v in /Rs:

$$\frac{v_{out}}{v_{in}} = \frac{-g_m Z_\pi R_L}{R_S} \tag{3.28}$$

Assuming that Z p is primarily capacitive at the frequency of interest:

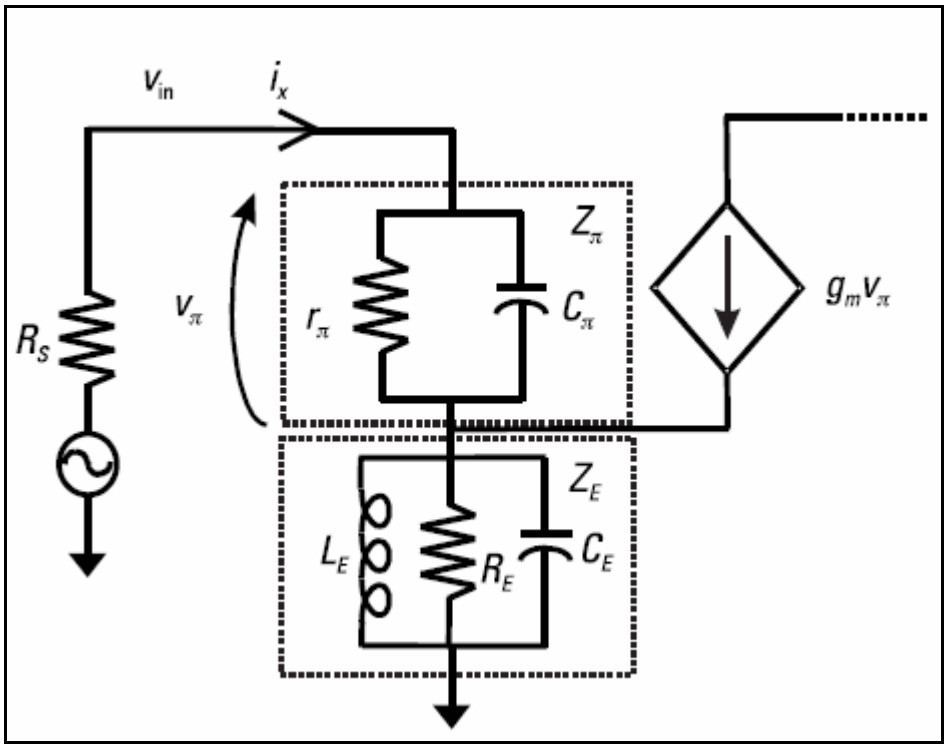


Figure 3.6 Small-signal model used to find the input impedance and gain.

$$\left|\frac{v_{\text{out}}}{v_{\text{in}}}\right| = \frac{g_m R_L}{R_S \omega_o C_\pi} = \frac{R_L \omega_T}{R_S \omega_o} \tag{3.29}$$

where vo is the frequency of interest. The input impedance has the same form as the common-collector amplifier and is also given by

$$Z_{\text{in}} = Z_\pi + Z_E(1 + g_m Z_\pi) \tag{3.30}$$

Of particular interest is the product of ZE and Z p. If the emitter impedance is inductive, then when this is reflected into the base, it will become a real resistance. Thus, placing an inductor in the emitter tends to raise the input impedance of the circuit, so it is very useful for matching purposes (Rogers & Plett, 2003). (Conversely, placing a capacitor in the emitter will tend to reduce the input impedance of the circuit and can even make it negative.)

# CHAPTER FOUR
# APPLICATION AND OPTIMIZATION

## 4.1 Circuit Design

As LNA has complex design, it is mostly time challenging to find a suitable design topology. This topology should comply with required performance criteria's. In this chapter a single transistor LNA was built for the required purpose and then it is evaluated using optimization features of AWR Microwave office.

In this chapter, I will explain the procedure that we followed during our design period. I will describe the design from transistor selection to measuring test board step by step.

Firstly, we examined datasheet to evaluate transistor for LNA design. The transistor's S parameters are published at different collector, emitter voltages and different current levels for frequencies ranging from low to high values. The datasheet also contains noise parameters, which are helpful for low noise design. Spice models for the transistor are also useful for IP3 and P1dB simulations.

We first look at three main design parameters: noise, gain and IP3, and decide what Vce and Ic levels will produce optimal performance. A closer examination of NF vs. collector current, shown in Figure 4.1, indicates that the minimum noise figure can be achieved at around 4 mA at both 900 MHz and 1.9 GHz. Gain available from the transistor vs. collector current is shown in Figure 4.2 and reveals another important aspect in LNA design: the forward transducer power gain of 18 dB remains constant at 1.9 GHz for current levels above 10 mA (24 dB for 900 MHz). Small gain degradation is expected at low current operation, below 10 mA.

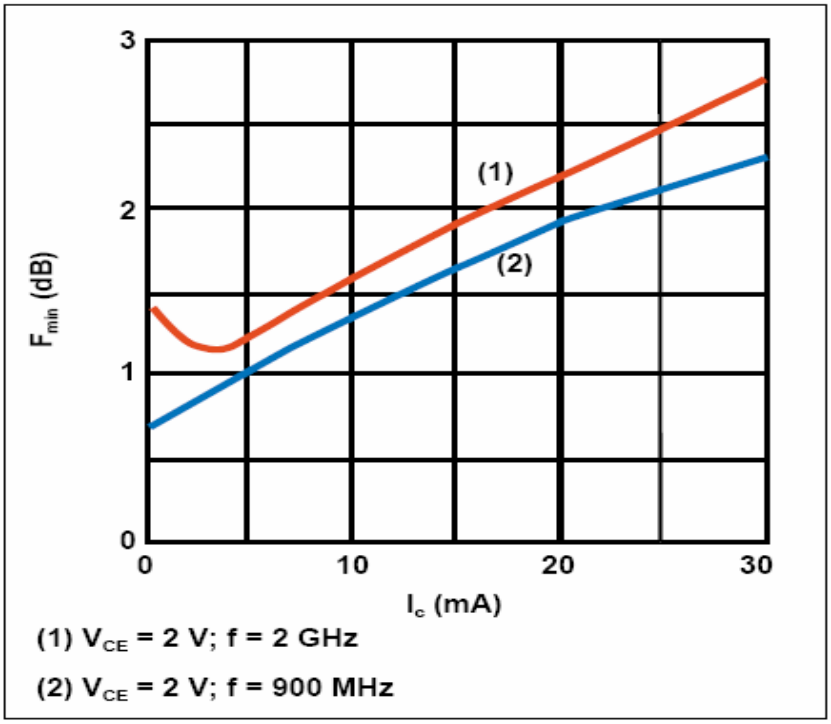


Figure 4.1 BFG425W minimum noise figure as a function of the collector current.

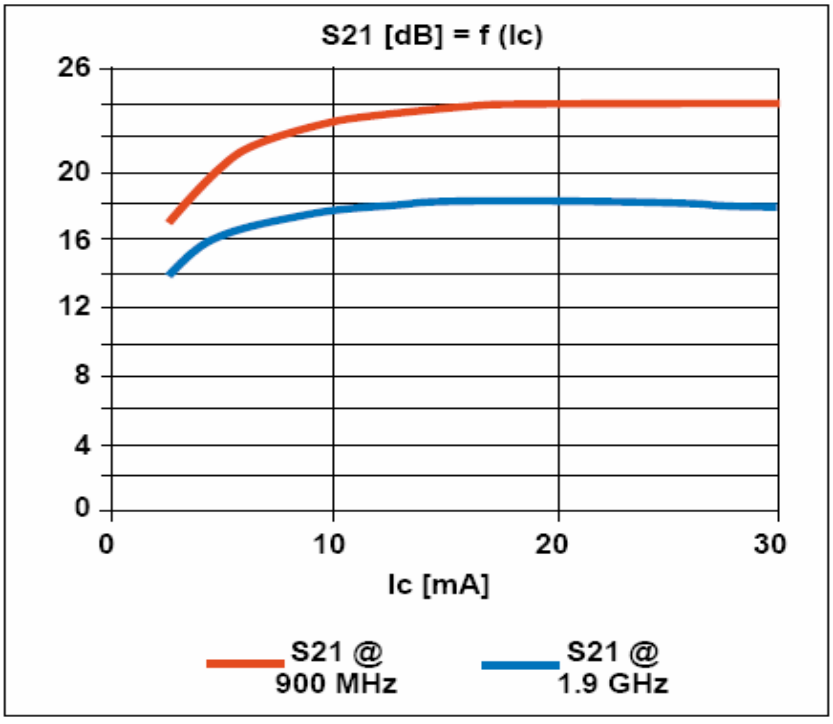


Figure 4.2 Forward transducer power gain.

The forward transducer power gain represents the gain from the transistor itself with its input and output presented with 50 Ω impedance. The $S_{21}$ values are provided by the manufacturer of the transistor at multiple frequencies and different Vce and current levels. Additional gain can be obtained from source and load matching circuits. Maximum stable gain (MSG) and maximum power gain (Gmax) are good indicators of additional obtainable gain from the LNA circuit. LNA linearity is another important parameter. A figure of merit for linearity is the IP3. A two tone test is used for derivation of IP3. As a rule of thumb for bipolar junction transistors (BJT), the output IP3 can be estimated from the following formula:

$$OIP3 = 10\log( V_{CE} * I_C * 5 ) \quad [dBm] \quad (4.1)$$

The graph of OIP3 vs. collector current can be derived. Figure 4.3 shows the result. The relation between IIP3 and OIP3 is defined as:

$$IIP3=OIP3 - Gain\ [dBm] \quad (4.2)$$

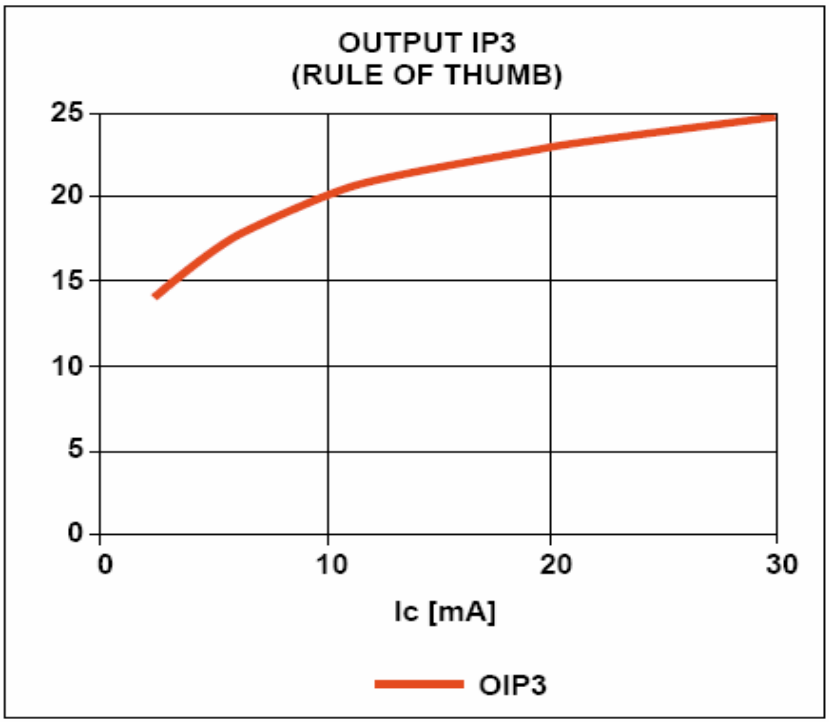


Figure 4.3 OIP3 vs. collector current.

We have 15 dB gain target and by examining the graph of Figure 4.3, one can determine that the transistor will need to be operated at at least 10 mA to produce a 5 dBm of IIP3 without any margins. Vce = 2 V and Ic of 10 mA is the point where the transistor will produce an acceptable gain of at least 15 dB with a noise figure below 2 dB at both 900 MHz and 1.9 GHz. IIP3 will also be above 5 dBm with a collector current level of 10 mA.

By evaluating first step, examining datasheet, we decided to use our rf transistor at $V_{CE}$=2V and $I_C$=10mA. We obtained required S parameters from manufacturer. Our main purpose is designing a LNA working at 1900MHz .We should also guarantee that design has no negative effect between 900MHz to 2.15GHz. We determined S parameters as a good starting point of theoretical calculations.

S parameters for BFG425 with VCE=2V and Ic = 10mA
V1=8.464E-001V, V2=2.000E+000V, I1=1.354E-004A, I2=9.990E-003A

| | S11 | | S21 | | S12 | | S22 | |
|---|---|---|---|---|---|---|---|---|
| Freq(GHz) | Mag | Ang | Mag | Ang | Mag | Ang | Mag | Ang |
| 0.800 | 0.425 | -87.225 | 15.319 | 113.159 | 0.031 | 54.730 | 0.663 | -42.816 |
| 0.900 | 0.401 | -94.933 | 14.228 | 107.957 | 0.033 | 52.973 | 0.627 | -45.635 |
| 1.000 | 0.380 | -102.247 | 13.234 | 103.181 | 0.035 | 51.492 | 0.595 | -48.126 |
| 1.100 | 0.362 | -109.145 | 12.347 | 98.795 | 0.038 | 50.239 | 0.567 | -50.401 |
| 1.200 | 0.347 | -115.750 | 11.551 | 94.701 | 0.039 | 49.235 | 0.542 | -52.518 |
| 1.300 | 0.334 | -121.928 | 10.835 | 90.876 | 0.041 | 48.350 | 0.518 | -54.459 |
| 1.400 | 0.323 | -127.972 | 10.199 | 87.304 | 0.043 | 47.448 | 0.496 | -56.265 |
| 1.500 | 0.314 | -133.805 | 9.622 | 83.881 | 0.045 | 46.698 | 0.478 | -57.977 |
| 1.600 | 0.306 | -139.489 | 9.100 | 80.598 | 0.047 | 45.938 | 0.460 | -59.689 |
| 1.700 | 0.300 | -144.862 | 8.626 | 77.494 | 0.049 | 45.231 | 0.444 | -61.352 |
| 1.800 | 0.295 | -150.093 | 8.196 | 74.493 | 0.051 | 44.478 | 0.429 | -62.992 |
| 1.900 | 0.291 | -155.020 | 7.803 | 71.594 | 0.053 | 43.695 | 0.416 | -64.705 |
| 2.000 | 0.288 | -159.893 | 7.444 | 68.765 | 0.055 | 42.878 | 0.402 | -66.400 |
| 2.200 | 0.285 | -169.312 | 6.812 | 63.355 | 0.059 | 41.222 | 0.378 | -69.781 |

S parameters of Philips BFG425 rf transistor at 1900MHz with $V_{CE}$=2V and $I_C$=10mA is:

$S_{11} = 0.291 \angle -155.020$ $S_{12} = 0.053 \angle 43.695$

$S_{22} = 0.416 \angle -64.705$ $S_{22} = 7.803 \angle 71.594$

Unconditional stability of the circuit is the goal of the LNA designer. Unconditional stability means that with any load presented to the input or output of the device, the circuit will not become unstable or will not oscillate. S parameters provided by the manufacturer of the transistor will aid in stability analysis of the LNA circuit. We can determine stability condition of LNA by numerical analysis consists of calculating a term called Rollett Stability Factor K. An intermitted quantity called delta (Δ) should be calculated first to simplify the final equation for the K factor. When the K factor is greater than unity, the circuit will be unconditionally stable for any combination of source and load impedance.

We calculate the stability factor of LNA at 1900MHz from equation 3.13 and 3.14:

$D_S = S_{11}S_{22} - S_{12}S_{21}$

$= 0.45873 \angle 79.526$

$$K = \frac{1+|D_s|^2-|S_{11}|^2-|S_{22}|^2}{2|S_{21}|\,|S_{12}|} = 1.05 > 1$$

System is unconditionally stable for any combination of source and load impedance at this frequency. As we have gain target of 15dB, we should check maximum available gain at this frequency. Maximum available gain:

$B_1 = 1+|S_{11}|^2-|S_{22}|^2-|D_S|$

$= 1 + 0.084681 - 0.173056 - 0.2104 = 0.701225$

$$\text{MAG} = 10\log\frac{|S_{21}|}{|S_{12}|} + 10\log\left|K \pm \sqrt{K^2 - 1}\right|$$

$$= 10 \log (147.22) + 10 \log (0.5713)$$

$$= 19.24 \text{ dB}$$

We theoretically achieved required stability and gain targets. We should realize these targets. First of all, we should match our circuit input and output ports to attached systems. We will connect our LNA circuit to external equipments with 50ohm impedance values. We have to determine load and source impedance values and calculate matching circuits.

We have to calculate $R_L$ and $R_S$ to determine matching circuits. First of all we calculate $R_L$ by using equations 3.5, 3.6 and 3.7.

$C_2 = S_{22} - ( D_S S_{11}^{\circ} ) = 0.416 \angle -64.705 ((\ 0.45873 \angle 79.526\ )(0.291 \angle 155.020))$

$C_2 = 0.0554728 \angle 169.841$

$B_2 = 1 + |S_{22}|^2 - |S_{11}|^2 - |D_S|^2$

$B_2 = 1 + 0.173056 - 0.084681 - 0.21043 = 0.877945$

$$|\Gamma_L| = \frac{B_2 \pm \sqrt{B_2^{\,2} - 4|C_2|^2}}{2|C_2|} = -0.473181 \angle -169.841$$

(The angle of the load reflection coefficient is simply equal to the negative of the angle of $C_2$ )

After calculating $R_L$, we also have to calculate $R_S$. We use equation 3.8 to find out $R_S$.

$$\Gamma_S = \left[ S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - (\Gamma_L \bullet S_{22})} \right]^{*} = 0.30488 \angle -198.35$$

Once the desired $R_S$ and $R_L$ are known, all that remains is to surround the transistor with components that provide it with source and load impedances which look like $R_S$ and $R_L$.

By using Smith chart we determine 33nH input inductor and 6.8pF input capacitance port matching. For output port matching we should use 3.3nH inductor and 1.5pF capacitor as seen in figure 4.4

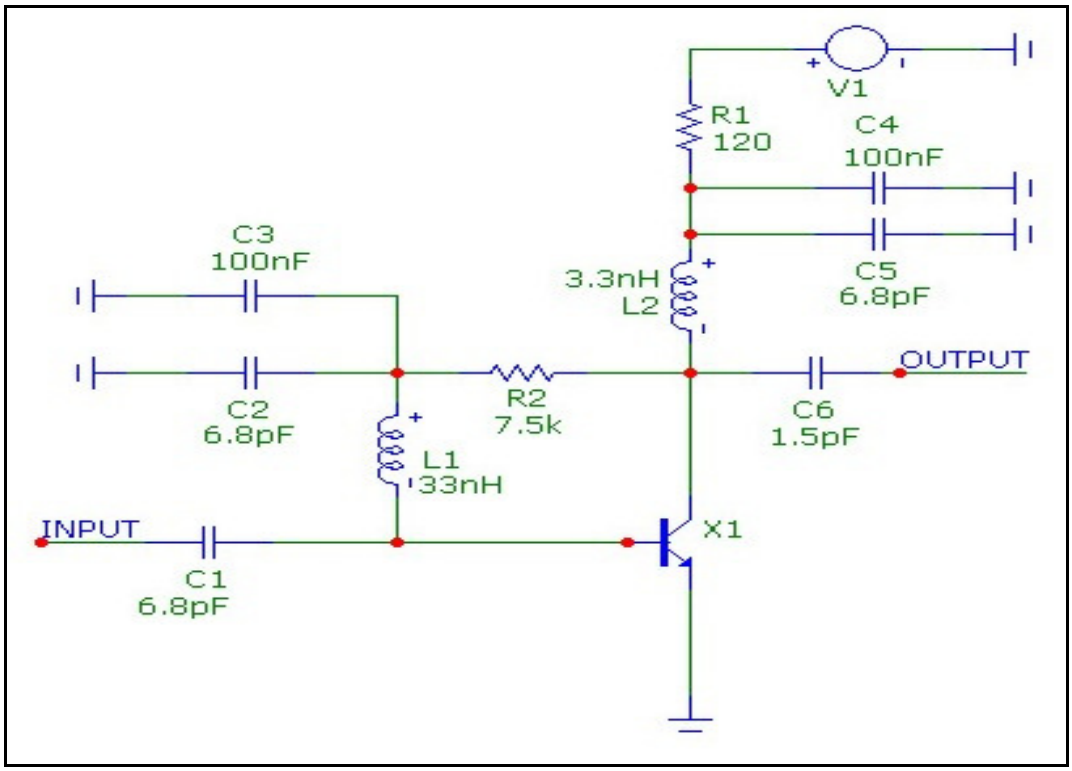


Figure 4.4. Original circuit for 1.9 GHz LNA with BFG425

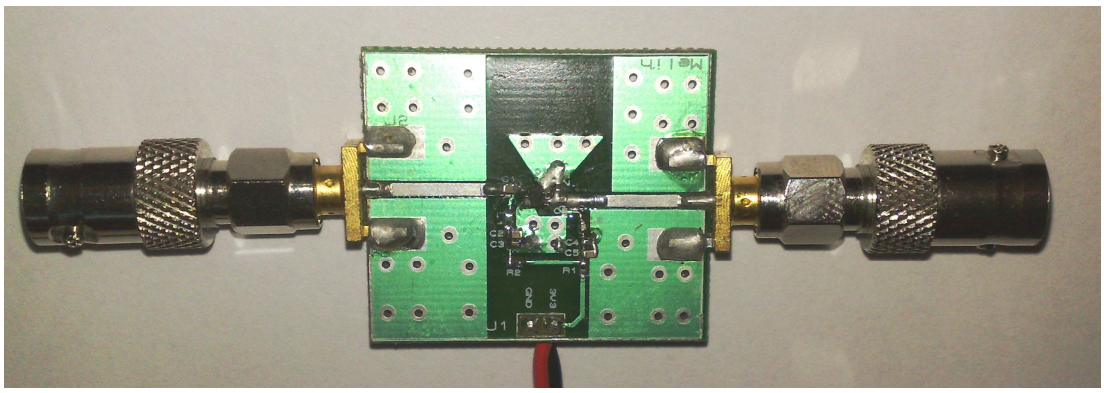

Figure 4.5 Photograph of the test board

Test board is designed to work with 50ohm connectors. Er, thickness of pcb and copper layer are learned from manufacturer. Input output transmission lines are designed to have 50 ohm resistance for perfect matching and eliminating reflections from connections by using this data.

## 4.2 Simulation Results

### *4.2.1 Original Circuit*

LNA circuit in figure 4.4 is designed especially for 1.9GHz. We both simulated and measured the circuit parameters between 800MHz to 2200MHz.

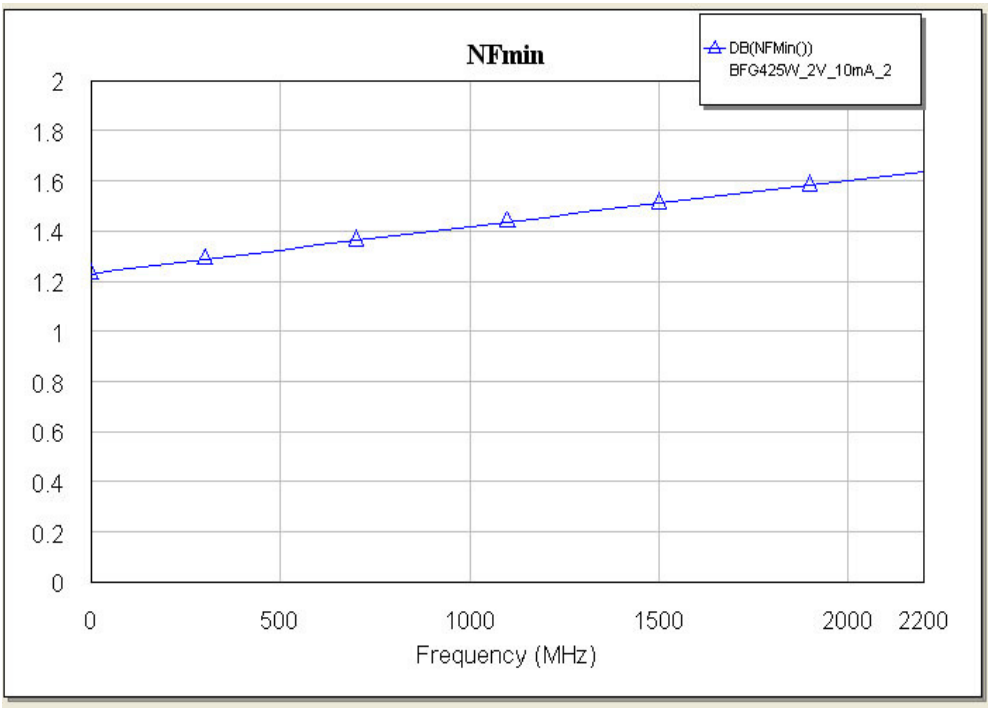


Figure 4.6. Simulation result for noise figure of the LNA

The circuit simulation values for BFG425 show that circuit has great noise figure capabilities. When we set $V_{CE}$ = 2V and $I_C$=10 mA, we achieve very low noise figures at required operating frequency band.

As we mentioned before we have stability and gain targets. We should analysis these values by simulation then we have to confirm by measuring the test board. We imported s parameters into the AWR Microwave Office and analyzed stability factor from 900MHz to 2.2GHz. (Figure 4.4) At and above operating frequency, Rollette Stability factor has values greater then 1. This shows that below 1.9GHz, we should check risk of oscillation.

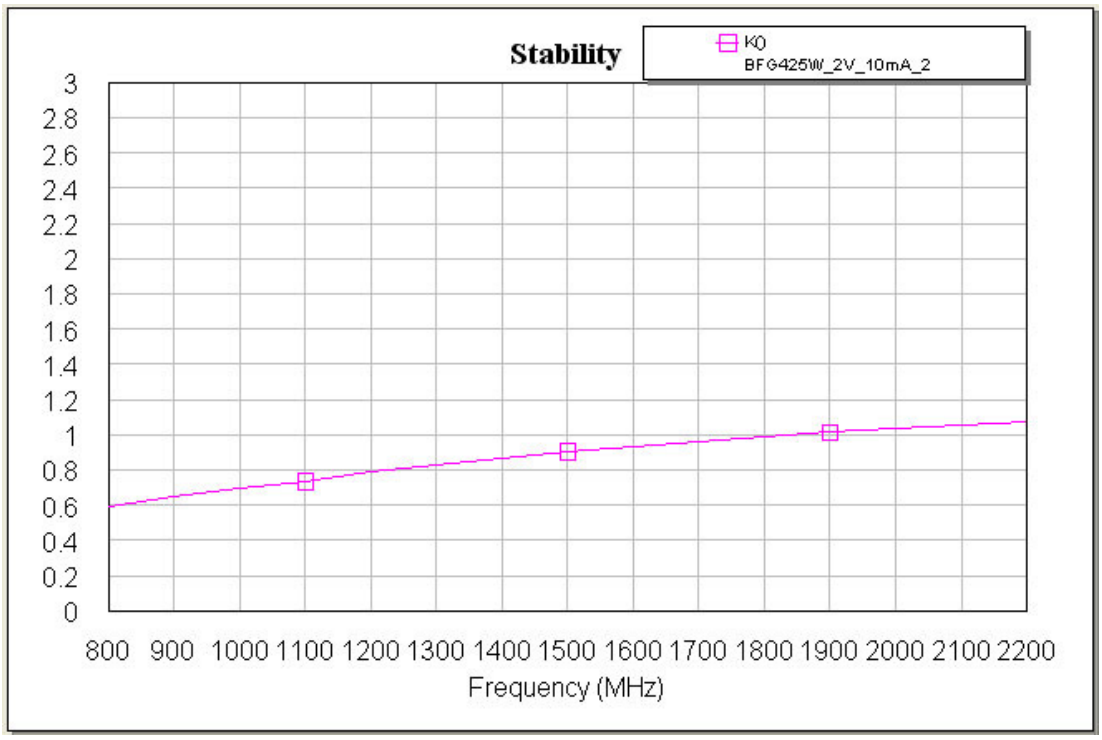


Figure 4.7. Simulation result for stability factor of the rf transistor

As I explained above, transistor has stability factor greater then 1 above 1.85GHz. Below this frequency circuit can oscillate with regards to input and output matching circuits, load and source conditions.

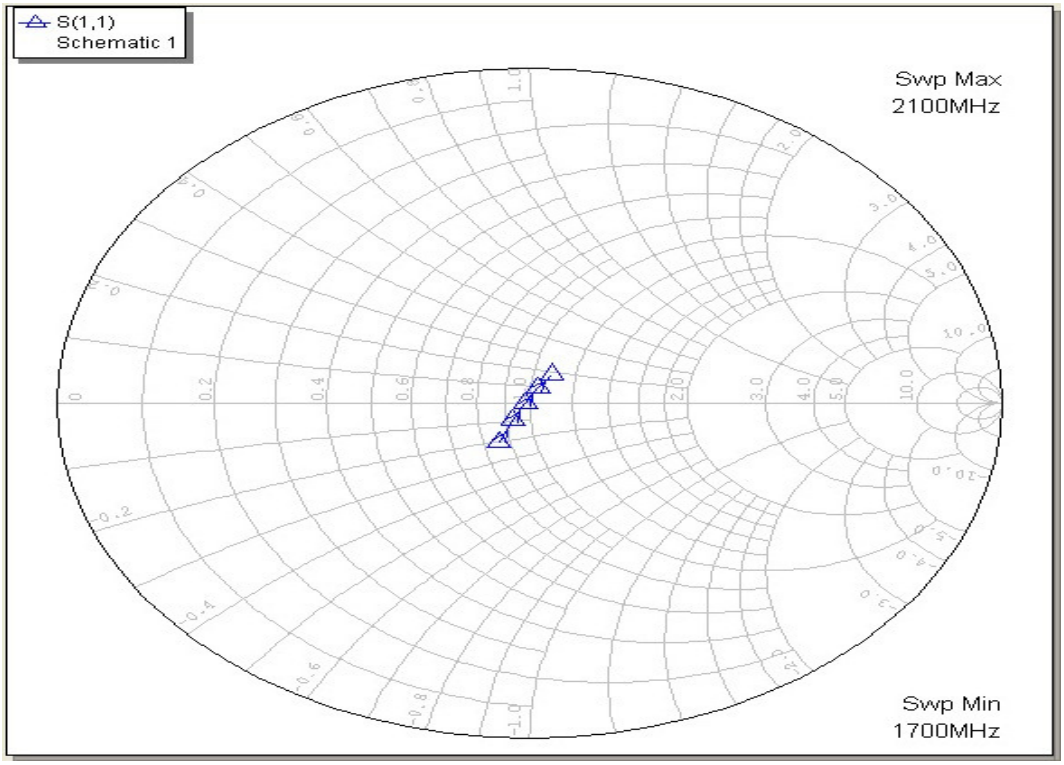


Figure 4.8. Smith chart representation for S11 of original circuit

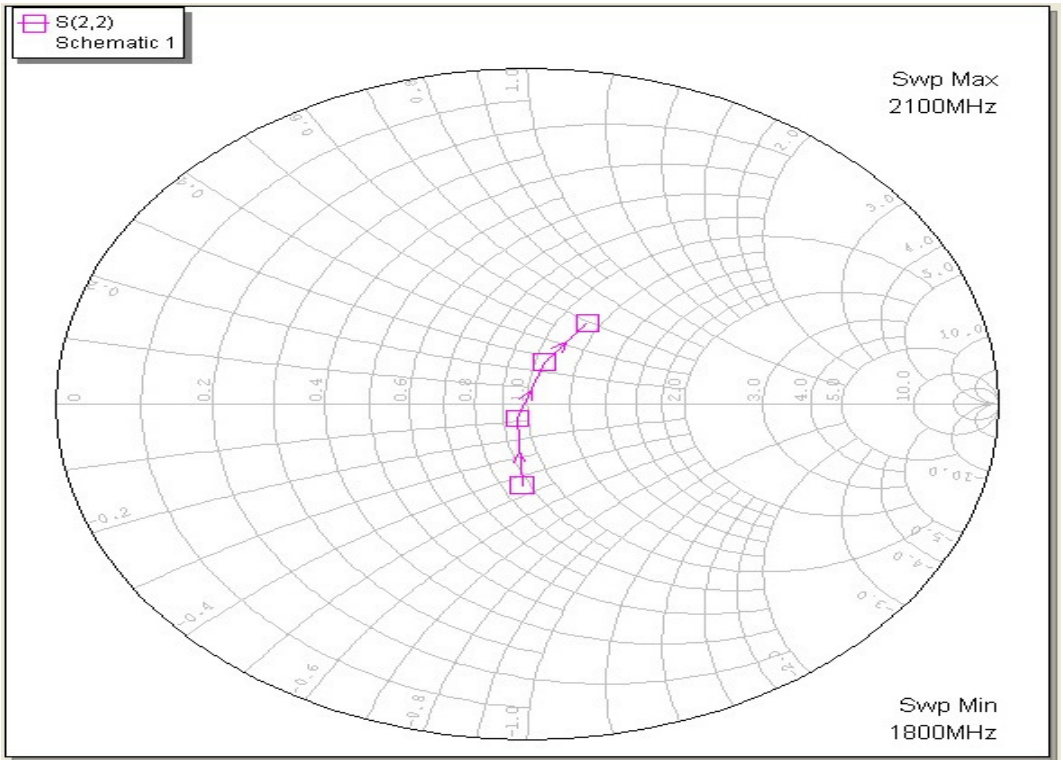


Figure 4.9. Smith chart representation for S22 of original circuit

According to smith chart representations of S11 and S22, we can say that circuit has great matching at 1.9GHz. S11 and S22 lines passes at R=1, X=0 point at 1.9GHz.

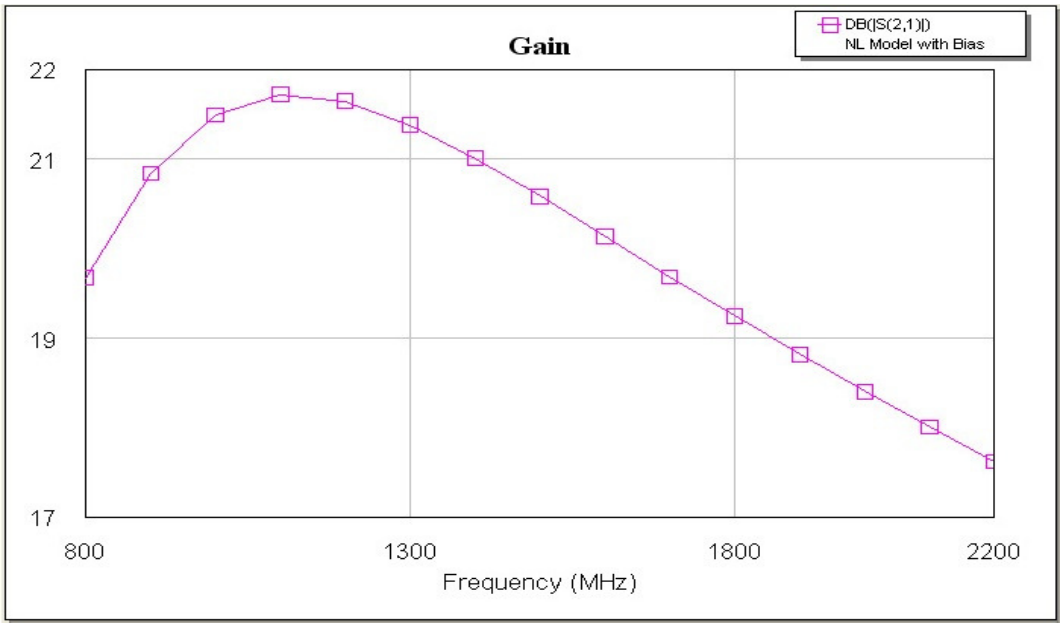


Figure 4.10. Gain result for original circuit

The graph shows us that; amplifier has gain above 15dB within 0.8-2.15GHz band. This nonlinear gain is not suitable for broadband applications. We prefer linear gain within whole band. System reaches our target criteria's at 1.9GHz but requires some optimization for a better whole band performance.

### *4.2.2 Optimized Matching Circuit*

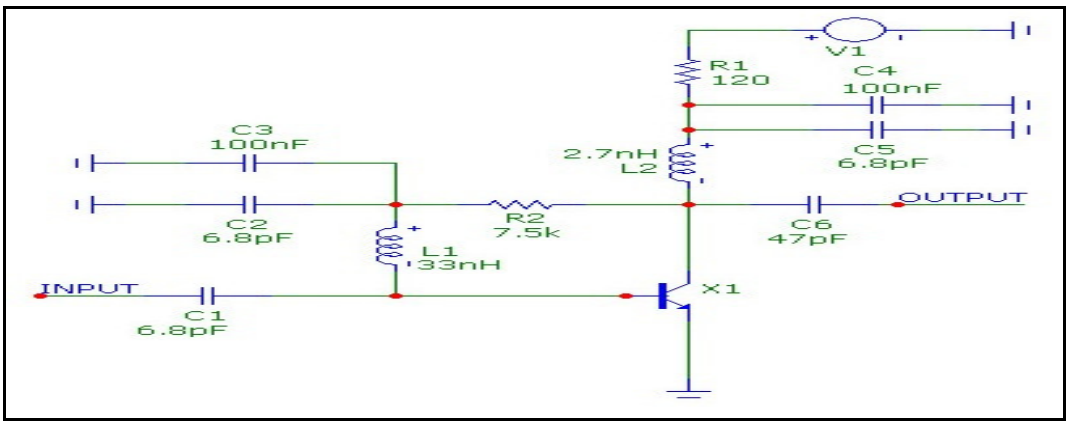


Figure 4.11. Gain result for optimized matching circuit

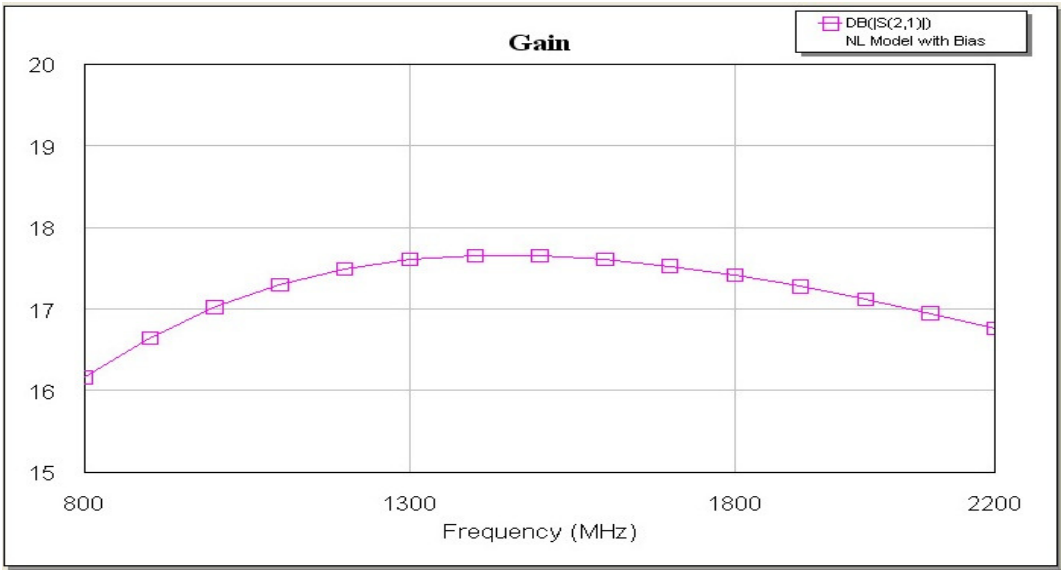


Figure 4.12. Gain graph of LNA with optimized matching circuit

Although system has good matching performance at 1.9GHz, it is not always best solution for the designer. Practical applications show us that it is better to create some mismatch to have a flat gain within whole band application. To achieve our goal, we made some adjustment at output L matching network. C6 and L2 have been replaced with 47pF and 2.7nH components by the help of AWR simulation "tune" module. After optimizing output L matching circuit we lost gain at lower frequencies. We achieved our gain target but we couldn't get a flat gain graph.

### *4.2.3 Inductive Source Degeneration Application*

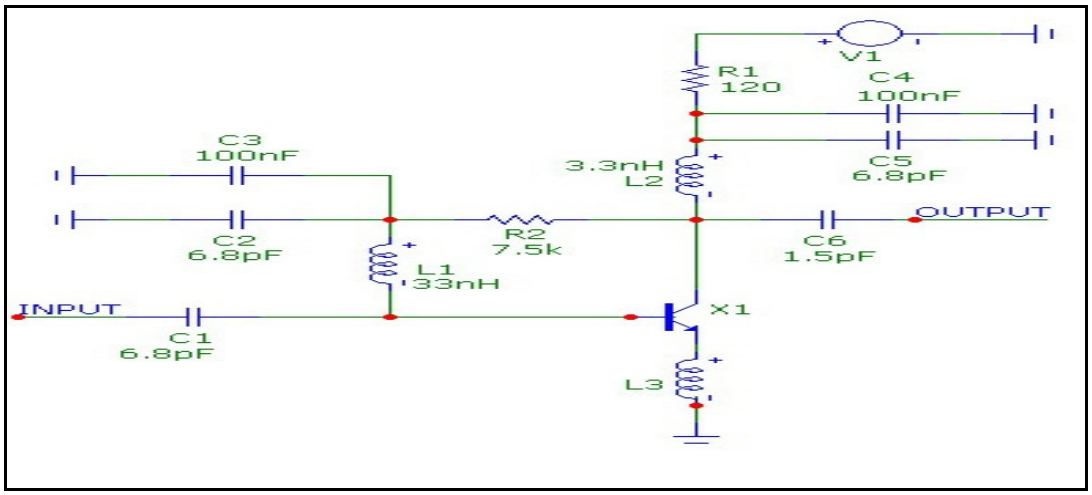


Figure 4.13. Gain graph of LNA with inductive source degeneration

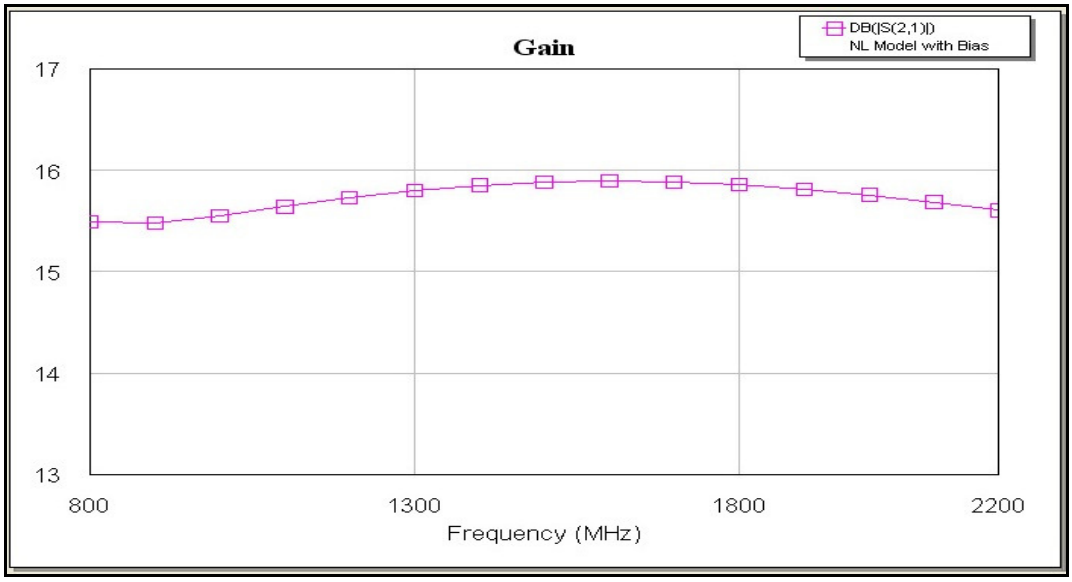


Figure 4.14. Gain graph of LNA with inductive source degeneration

Matching circuit optimization wasn't enough to flatten gain graph so we applied inductive source degeneration method as an alternative solution. Inductive source degeneration causes gain loss at lower frequencies but system has flat enough gain within whole band. We achieved our gain target and also there is less then 1 dB gain difference between highest and lowest gain points on the graph.

## 4.3 Measurement Results

### *4.3.1 Original Circuit*

Table 4.1 1.9GHz LNA measurement results

| Parameters | Units | Measured Performance |
|---|---|---|
| Vce | Volts | 2 |
| Ic | mA | 10.2 |
| Vsupply | Volts | 3.3 |
| Gain | dB | 17.4 |
| NF | dB | 1.9 |
| IRL | dB | 13 |
| ORL | dB | 11 |

We tested our test board with a modern Tektronix network analyzer which has built in s parameter analysis modules. We first tested our test setup by short circuiting source and load. We calculated the cable and connector losses. Then we gave input signal between 800MHz to 2.2GHz. We tested our board with signals with various frequency and power.

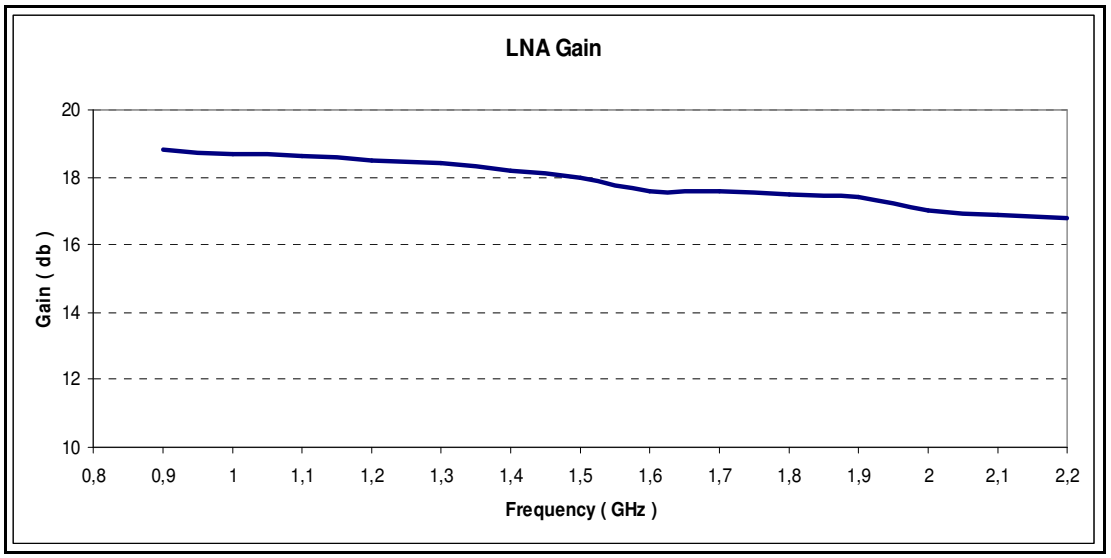


Figure 4.15 LNA gain measurement between 0.8GHz to 2.2GHz

From the measurement results we achieved our gain and noise figure targets at 1.9GHz. We also checked the system performance through whole band. We observed that at small frequencies system has higher gain which corresponds with our datasheet evaluation results. We wanted to have a more flat gain and we searched for a solution and decided to use a simulation program as optimization assistance.

### 4.3.2 Optimized Circuit

We implemented series feedback on circuit in figure 4.4 in order to lower the gain at the lower frequencies and hence improve the stability of the circuit. We increased the feedback resistor to decrease current and improve noise performance. We also calculated input and output matching circuit values for smaller frequencies such as 900MHz. We tried new matching circuit and feedback values through whole band. We also added series resistor between emitter to ground for decreasing gain at lower

frequencies to make gain graph flatter. We prepared another test board with the circuit components as shown in Figure 4.9.

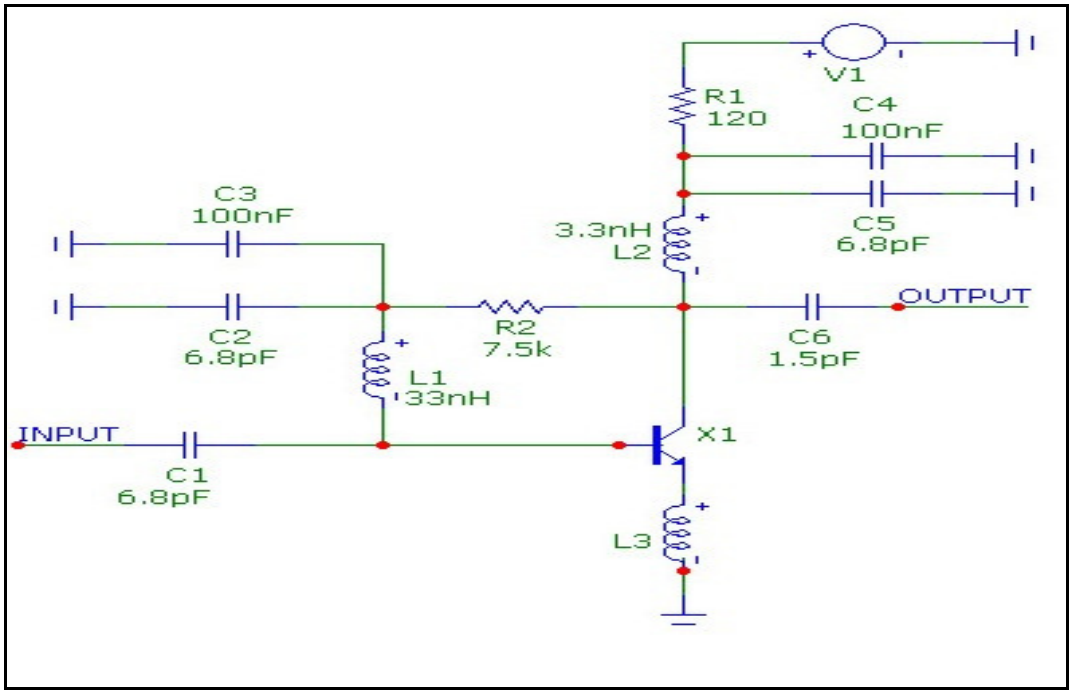


Figure 4.16 Optimized amplifier circuit

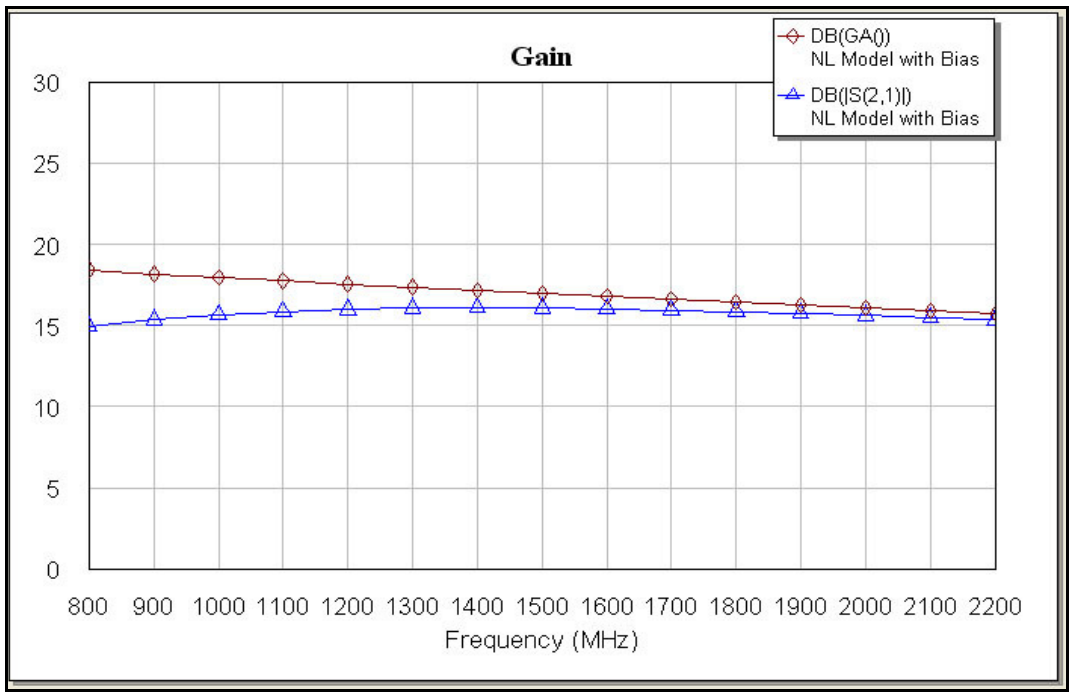


Figure 4.17 Simulation result of the optimized circuit

Implementing series feedback and optimizing circuit with AWR gives us a more flat but decreased gain graph. We achieved a good gain result within the whole band of satellite application. Adding series feedback between emitter to ground decreased gain at lower frequencies as expected.

Rollette stability factor is smaller then one below at 1.9GHz so we increased value of $R_3$ and checked S parameters and stability factor. There is no oscillation problem with the new setup.

Table 4.2 Optimized LNA measurement results

| **Parameters** | **Units** | **Measured Performance** |
|---|---|---|
| Vce | Volts | 2 |
| Ic | mA | 8 |
| Vsupply | Volts | 3.3 |
| Gain | dB | 15.78 |
| NF | dB | 1.7 |
| IRL | dB | 13 |
| ORL | dB | 11 |
| IIP3 | dBm | 5 |

If we analyze the measurement results, we have loss of 1.6dB gain and improvement of 0.2dB noise figure values with the new setup. This result shows us that conjugate matching for input and output impedances is not always best solution. We sometimes require some mismatch to achieve flat gain through a wide frequency band.

# CHAPTER FIVE
# CONCLUSION

The main goal of this thesis was to design a low noise amplifier for digital video broadcasting satellite, which is working between 950MHz to 2150MHz frequency to extract and amplify the received signals coming from satellites. Beside that LNA was especially designed for 1.9GHz interference problems which correspond to UMTS frequency.

We know that as long as main signal power is greater then interferer we can overcome interference and mosaic problems in tuner applications. To overcome this problem, low noise amplifier is designed especially for 1.9GHz but whole frequency band was checked during simulations and measurements. We wanted to be sure that LNA does not have negative effect on other frequencies within the band.

Satellites are generally using integrated amplifier solutions at tuner front ends. This is an expensive solution and also takes bigger space on pcb and has less flexibility. Finally the designed LNA is used with current satellite tuner applications to reduce the system components, signal loss and create design flexibility.

We first designed our circuit for 1.9GHz and we tried to match input and output ports for maximum gain. We achieved our 15dB gain target. Then we checked whole satellite band and observed that gain is not flat enough. We have higher gain values at lower frequencies.

From evaluation of transistor datasheet, we know that transistor has higher gain at lower frequencies with the selected biasing values.

At this point computer aid given by AWR Microwave Office is an invaluable asset. With given LNA topology, AWR gives circuit outputs and helps optimization

of circuit parameters for high overall performance.

As our objective was to find an LNA topology which fulfills satellite RF front end requirements, it was natural to use an optimizer to see how slight changes affect performance. Initial design showed that circuit has good gain but not flat enough within the whole band although it satisfied us with good noise figure and stability. It showed us that we require series feedback. This method provide much more flat gain graph with decreasing noise figure. This method should be carefully used not to lower gain and P1dB point critically.

To achieve our target we applied series feedback between emitter and ground. The process of intentionally inserting additional inductance between device emitter connections and RF ground is a commonly employed method used for influencing device input output match, noise match, stability and linearity. This additional inductance provides series series negative feedback, improving amplifier $3^{rd}$ order intercept and gain compression points at the cost of reduced gain.

We know that our system has stability factor less then one for frequencies below 1.85GHz. The use of inductive emitter degeneration for the purposes of linearity improvement also had a major impact on the stability of the amplifier. In brief: a small amount of emitter degeneration improves stability at lower frequencies, but as the amount of emitter inductance is increased, stability at higher frequencies, e.g. in the range of 5 to 10GHz is compromised. Additional emitter inductance helped to bring K to a value greater then 1, particularly in the range of 800 -2200 MHz.

As expected this circuit showed lower but flat gain and met stability requirements. Last optimized circuit led to an approximate 1.5 to 2 dB gain decrease and 0.2dB noise figure reduction. The computed values are almost same with the measured values on test board except connector and cable losses.

After that the designed LNA can connect, match and test together with satellite tuners. During this time, we feel that we have gathered and studied enormous

information on how digital video broadcasting and low noise amplifiers (LNA) works. For simulation, AWR Microwave software was used .We learnt a lot of new tools from this software and used them in our design process. The best thing about this work has been our experience in doing a lot of practical work.

It requires solid understanding of underlying principles to design a low noise amplifier with traditional methods. It is clear that we require some degree of compromising as one performance parameter is affected negatively by the optimization of another parameter. We require high overall performance requirements so little freedom for compromising is available. This compromising makes design more complex.

For future work it is strongly recommended that special care is to be taken while connecting wires between components on the board and the voltage supply. Also effort to reduce the complexity of the circuit with fewer components would help. Another important point is tried to redesign the stability circuits at lower frequencies to make the circuits much more stable at lower frequencies.

**REFERENCES**

Aitha, V.R. & Imam, M.K. (2007). *Low noise amplifier for radio telescope at 1.42GHz*. Retrieved October, 2007, from http://hh.diva-portal.org/smash/record.jsf?searchId=1&pid=diva2:238215.

Bowick, C. (1997). *RF circuit design* (n.d.). USA: Newnes Press.

Edwall, M. (2008). *Low noise amplifier design and optimization*. Retrieved November, 2008, from http://epubl.luth.se/1402-1617/2008/230/LTU-EX-08230-SE.pdf

Gonzalez, G. (1996). *Microwave transistor amplifiers analysis and design* (2nd ed.). USA: Prentice-Hall, Inc.

Jayaraman, K. (2009). *Self-calibrated, reconfigurable RF LNA*. Retrieved December 17, 2009, from http://ir.library.oregonstate.edu/

Lehto, A. & Raisanen, A.V. (2003). *Radio engineering for wireless communication and sensor applications* (n.d.). Boston: Artech House, Inc.

Lucek, J. & Damen, R. (1999). *Designing an LNA for a CDMA frontend*. Retrieved February, 1999, from http://www.nxp.com/document/application_note/LNA97.pdf

Razavi, B. (1998). *RF microelectronics* (n.d.). USA: Prentice Hall, Inc.

Rogers, J. & Plett, K. (2003). *Radio frequency integrated circuit design* (n.d.) USA: Artech House, Inc.

Sayre, C.W. (2008). *Complete wireless design* (2nd edition). USA: McGraw-Hill International, Inc.

Sperling, M. (2003). *SiGe BiCMOS RF wideband lna example*. Retrieved August 19, 2003, from http://www.ece.cmu.edu/research/publications/2003/CMU-ECE-2003- 034.pdf

Vaucher, C. & van der Tang, J. & Leenaerts, D. (2001). *Circuit design for RF tranceivers* (n.d.). Boston, London: Kluwer Academic Publisher.

Wu, S.C. (2009). *Design and implementation of Ka-Band low power consumption low noise amplifier*. Retrieved December 25, 2009, from http://thesis.lib.ncu.edu.tw/ETD-db/ETD-search/view_etd?URN=965201033

# APPENDIX A

## A.1 Quick Reference Data of NXP BFG425 RF Transistor

Table A.1.1 Reference parameters of NXP BFG425 transistor

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $V_{CBO}$ | collector-base voltage | open emitter | – | – | 10 | V |
| $V_{CEO}$ | collector-emitter voltage | open base | – | – | 4.5 | V |
| $I_C$ | collector current (DC) | | – | 25 | 30 | mA |
| $P_{tot}$ | total power dissipation | $T_s \leq 103$ °C | – | – | 135 | mW |
| $h_{FE}$ | DC current gain | $I_C$ = 25 mA; $V_{CE}$ = 2 V; $T_j$ = 25 °C | 50 | 80 | 120 | |
| $C_{re}$ | feedback capacitance | $I_C$ = 0; $V_{CB}$ = 2 V; f = 1 MHz | – | 95 | – | fF |
| $f_T$ | transition frequency | $I_C$ = 25 mA; $V_{CE}$ = 2 V; f = 2 GHz; $T_{amb}$ = 25 °C | – | 25 | – | GHz |
| $G_{max}$ | maximum power gain | $I_C$ = 25 mA; $V_{CE}$ = 2 V; f = 2 GHz; $T_{amb}$ = 25 °C | – | 20 | – | dB |
| F | noise figure | $I_C$ = 2 mA; $V_{CE}$ = 2 V; f = 2 GHz; $\Gamma_S = \Gamma_{opt}$ | – | 1.2 | – | dB |

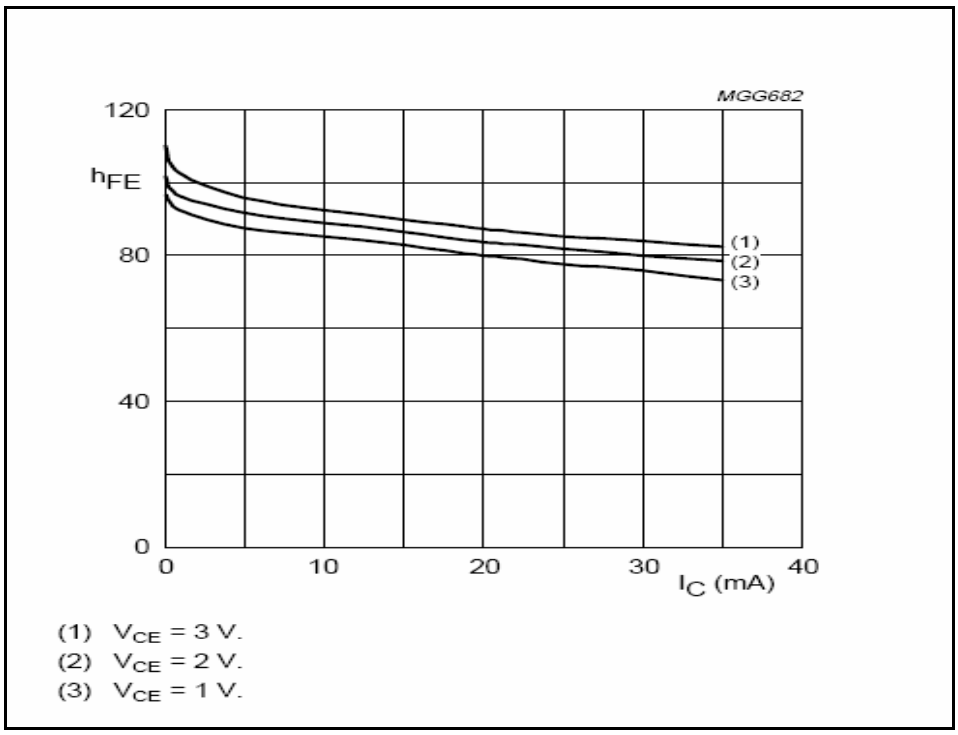


Figure A.1.1 current gain as a function of collector current

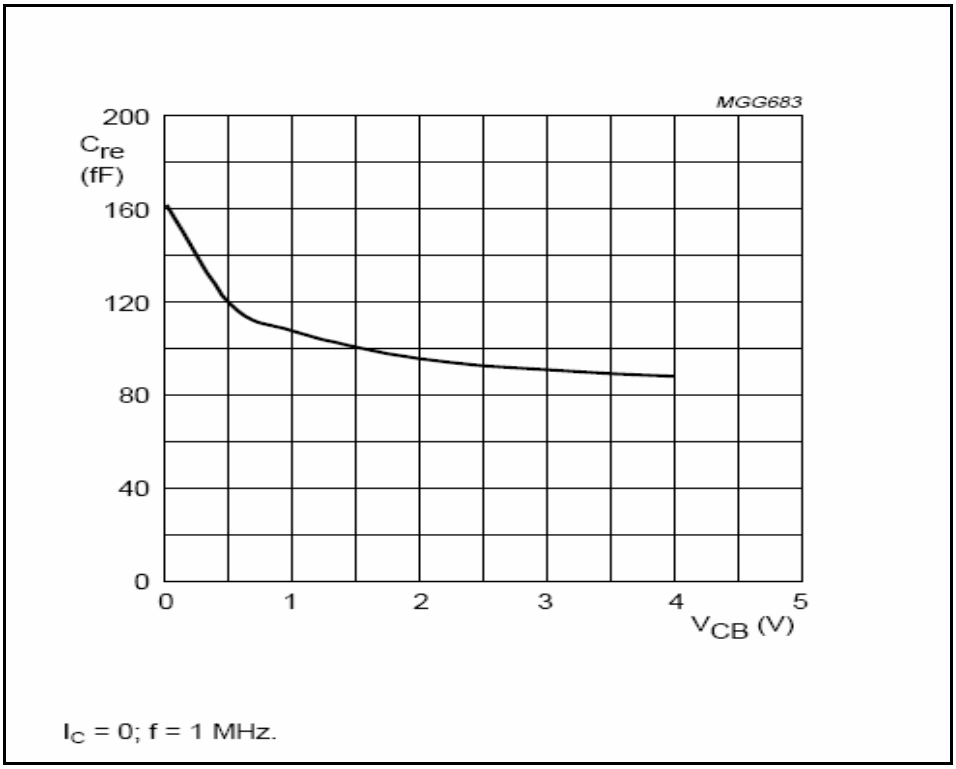


Figure A.1.2 Feedback capacitance as a function of collector base voltage

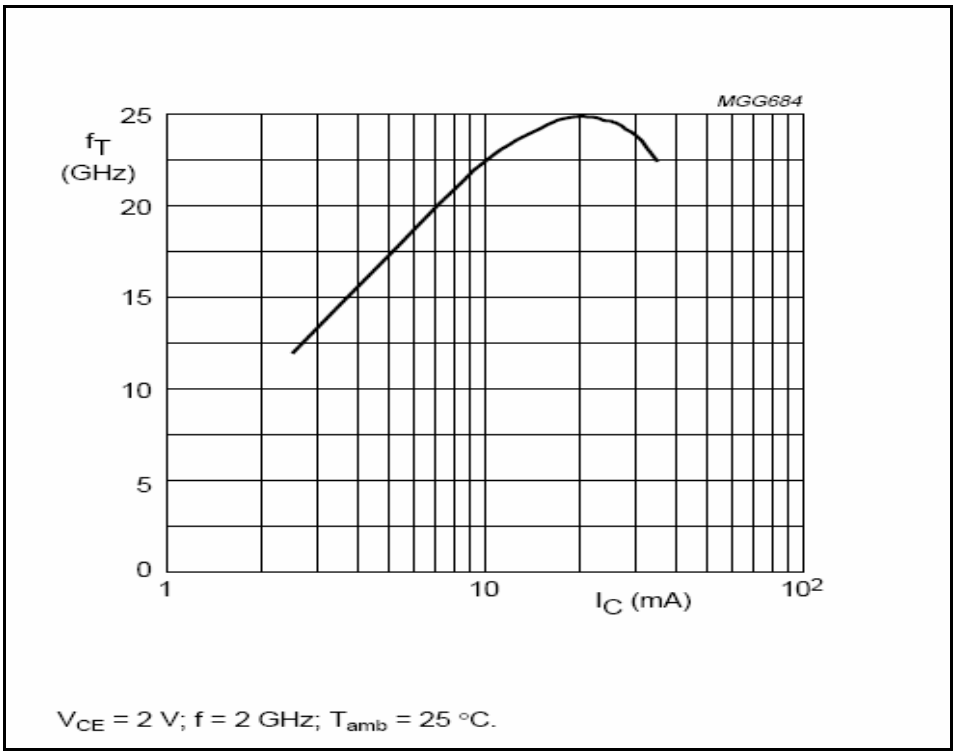


Figure A.1.3 Transition frequency as a function as collector current; typical values.

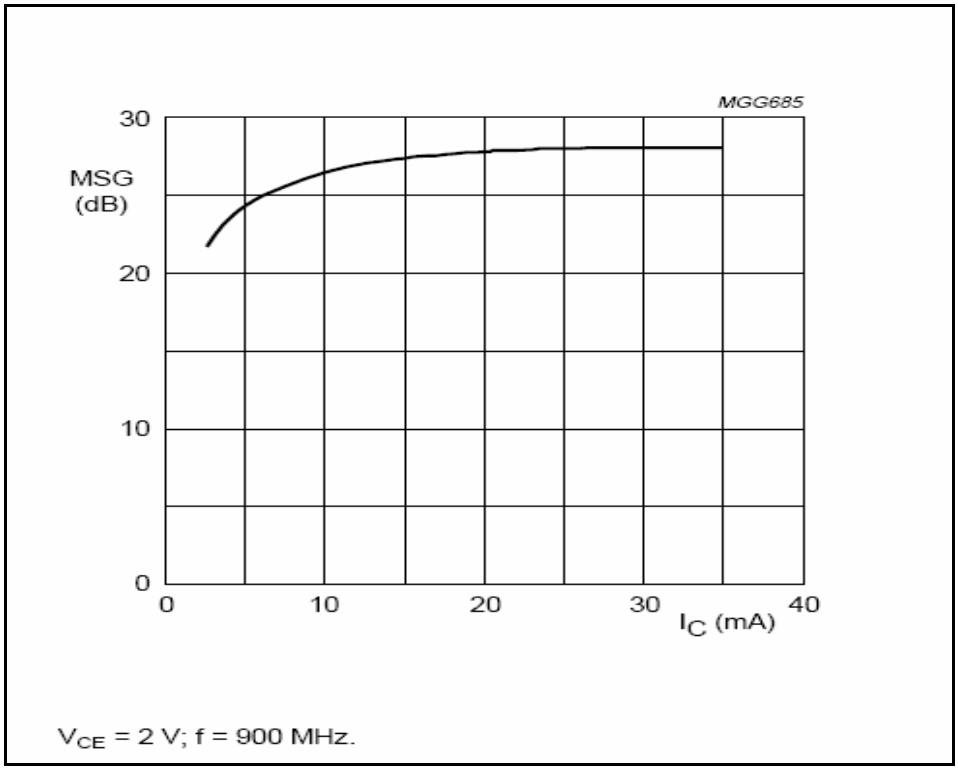


Figure A.1.4 Maximum stable gain as a function of collector current; typical values.

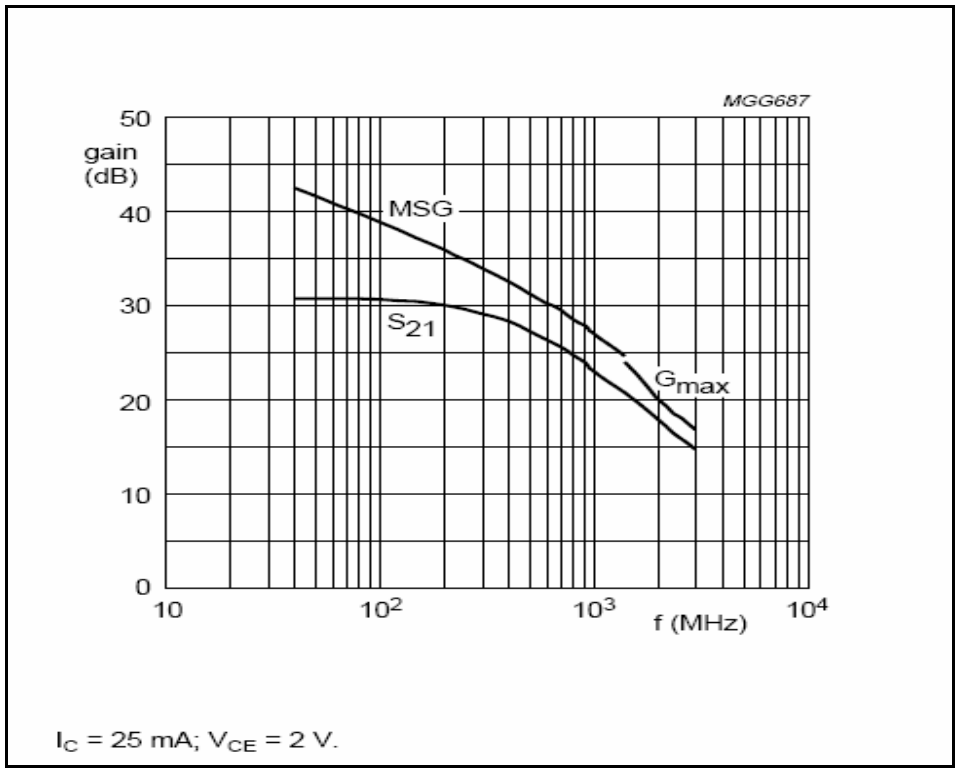


Figure A.1.5 Gain as a function of frequency; typical values.

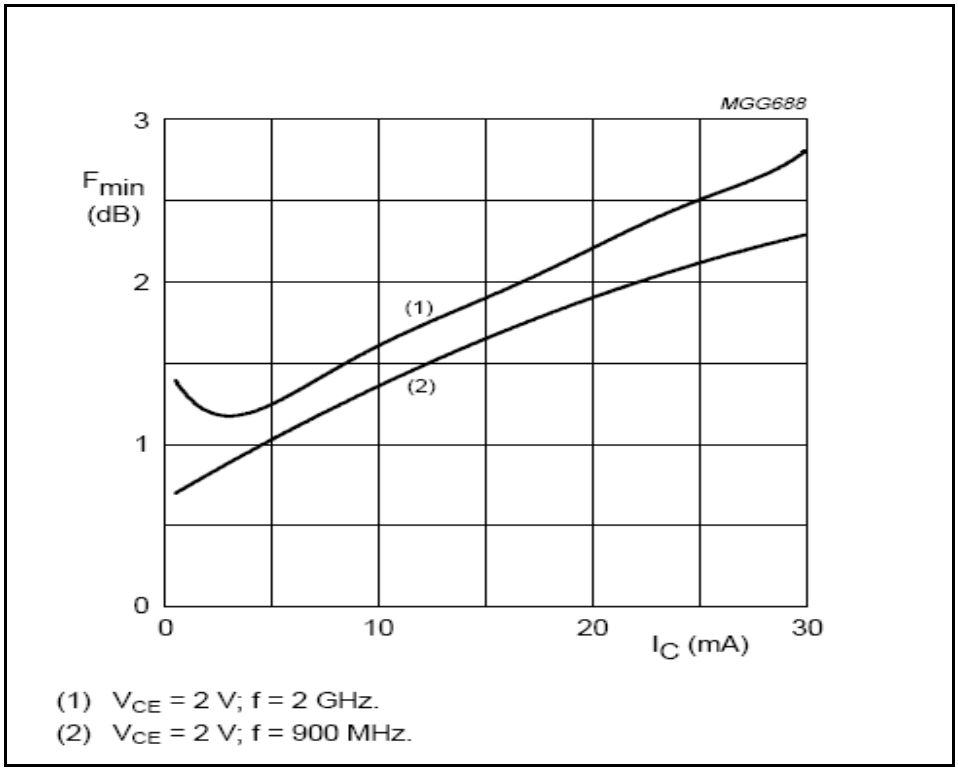


Figure A.1.6 Minimum noise figure as a function of the collector current; typical values.