DOKUZ EYLÜL UNIVERSITY
GRADUATE SCHOOL OF NATURAL AND APPLIED SCIENCES

NOVEL POSSIBILITIES IN SQUARE-ROOT DOMAIN CIRCUIT DESIGN

by
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October, 2011
İZMİR

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Ph.D. THESIS EXAMINATION RESULT FORM

We have read the thesis entitled **"NOVEL POSSIBILITIES OF SQUARE-ROOT DOMAIN CIRCUIT DESIGN"** completed by **SİNEM ÖLMEZ** under supervision of **PROF.DR. UĞUR ÇAM** and we certify that in our opinion it is fully adequate, in scope and in quality, as a thesis for the degree of Doctor of Philosophy.

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Sinem ÖLMEZ

NOVEL POSSIBILITIES IN SQUARE-ROOT DOMAIN CIRCUIT DESIGN

ABSTRACT

Square root domain circuits are a subclass of the companding circuits propound large dynamic range under low-voltage/low power, operating in high frequencies, and electronically tuneablity using DC current sources. Due to these advantages, companding circuits are compatible with CMOS VLSI technology. Since digital circuits are implemented in this technology, design of companding circuits has received great attention.

In this thesis, first order lowpass, second order lowpass, second order bandpass filter and an oscillator designed in square root domain are presented. Lossless integrator, first order highpass, allpass filters; second order highpass, notch with regular, highpass and lowpass cases, allpass filters; Kerwin-Huelsman-Newcomb biquad filter; Tow-Thomas biquad filter; fifth order Butterworth lowpass filter and quadrature oscillator are proposed as novel in the literature. All square root domain circuits are designed by using state space synthesis method. The cut-off frequency and the quality factor of filters are electronically tuneable by changing external currents and dimensions of MOS transistors, respectively. At the same time, oscillation frequency and oscillation condition of oscillators are adjustable by external currents. Only MOS transistors and grounded capacitors are used with single power supply. The proposed filters have low THD values, low power consumption, large dynamic range due to having externally linear internally nonlinear structures.

Keywords: square root domain circuits, state-space synthesis method, companding circuits, analog circuit design

KAREKÖK DOMENİNDE DEVRE TASARIMINDA YENİ OLANAKLAR

ÖZ

Karekök ortamı devreler, düşük gerilim/düşük güç altında geniş dinamik alana sahip olma, yüksek frekanslarda çalışma, doğru akım kaynakları ile elektronik olarak ayarlanabilme özelliklerini sergileyen sıkıştırma-genişletme devrelerinin bir alt kümesidir. Bu sözü edilen özelliklerinden dolayı, sıkıştırma-genişletme devreleri CMOS çok geniş çapta tümleştirme teknolojisi ile uyumludur. Aynı zamanda sayısal devreler CMOS teknolojisi ile gerçekleştirildiğinden bu tip devreler büyük ilgi görmektedir.

Bu tezde; karekök ortamında tasarlanmış birinci derece alçak geçiren, ikinci derece alçak geçiren, ikinci derece bant geçiren filtre ve osilatör devreleri sunulmuş olup, kayıpsız integral alıcı, birinci derece yüksek geçiren; ikinci derece yüksek geçiren, tüm geçiren, bant süzen filtrenin düzenli, yüksek geçiren ve alçak geçiren durumları; Kerwin-Huelsman-Newcomb filtre; Tow-Thomas filtre; beşinci derece Butterworth alçak geçiren filtre ile dördün osilatör literatüre yenilik olarak önerilmiştir. Tüm karekök ortamı devreler durum-uzay sentez metodu kullanılarak tasarlanmıştır. Filterlerin kesim frekansları harici akım kaynakları ile, kalite faktörü ise MOS transistörlerin boyutları değiştirilerek elektronik olarak ayarlanabilir. Aynı zamanda, osilatörlerin osilasyon frekansı ve osilasyon koşulu harici akım kaynakları ile değiştirilebilir. Tüm önerilen devreler, tek güç kaynağı ile MOS transistörler ve topraklanmış kapasitelerden oluşturulmuş olup harici doğrusal dahili doğrusal olmayan yapıya sahip olmalarından dolayı düşük THD değeri, düşük güç tüketimi, geniş dinamik çalışma alanı özelliklerine sahiptir.

Anahtar sözcükler: karekök domeni devreler, durum-uzay sentez metodu, sıkıştırma-genişletme devreleri, analog devre tasarımı

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CHAPTER ONE
INTRODUCTION

The fabrication technology of integration of analog and digital circuits on a single chip is optimized for digital processing because of limitation of digital circuitry area. So, there is a growing interest to design analog interface circuits that are compatible the CMOS VLSI technology in which digital circuits are fabricated (Eskiyerli & Payne, 2000).

Companding (compressing and expanding) circuits are very useful for low voltage, low power consumption, and high frequency analog systems. These circuits are realized based on translinear principle and quadratic current-voltage characteristic of MOS (Metal-Oxide Semiconductor) transistors or exponential current-voltage characteristic of BJTs (bipolar junction transistors). In recent years, there is a growing interest in the area of companding circuits. The main advantages of these circuits can be ordered as having large dynamic range under low voltage and also low power consumption, electronically tenability through applied bias currents and being designed in current mode with usage in high frequencies (Tvisidis and others, 1990; Seevinck,1990; Vlassis & Psychalinos, 2002).

The companding circuits are classified in two main types, which are log-domain circuits and square-root domain circuits. Log-domain circuits are based on the exponential relationship between base-emitter voltage (V_{BE}) and collector current (I_C) of BJTs and translinear principle. In 1979, for the first time, the low-pass filter introduced by R. W. Adams is a nonlinear (exponential) mapping on the state variables of a state space description of a linear transfer function. Seevinck proposed a class AB translinear integrator which is a special type of log-domain circuits (1990). Frey offered the complete theory of the log-domain filters in 1993. Toumazou and others presented log domain filters in terms of MOSFET circuits that operate in weak inversion in 1994. The main disadvantages of these circuits are limited operation frequency and drawback caused of transistor mismatches. Whereupon, filters and integrators designed with MOSFETs operated in saturation

region were introduced by Eskiyerli and others in 1996. These circuits are based on the quadratic relationship between drain current (I_D) and gate-source voltage (V_{GS}) and on the MOS translinear principle. By design topology, these circuits are called square-root domain circuits. In square-root domain circuits, two main operators are used, which are taking square of voltage and taking square-root of current (Psychalinos, 2008). If a current source is applied to drain of MOS transistor, its gate-source voltage is expressed by square-root of applied current source; this circuit is called compressor. If a voltage is applied across gate to source of MOS transistor, drain current is expressed by square of applied gate- source voltage; this circuit is called expander.

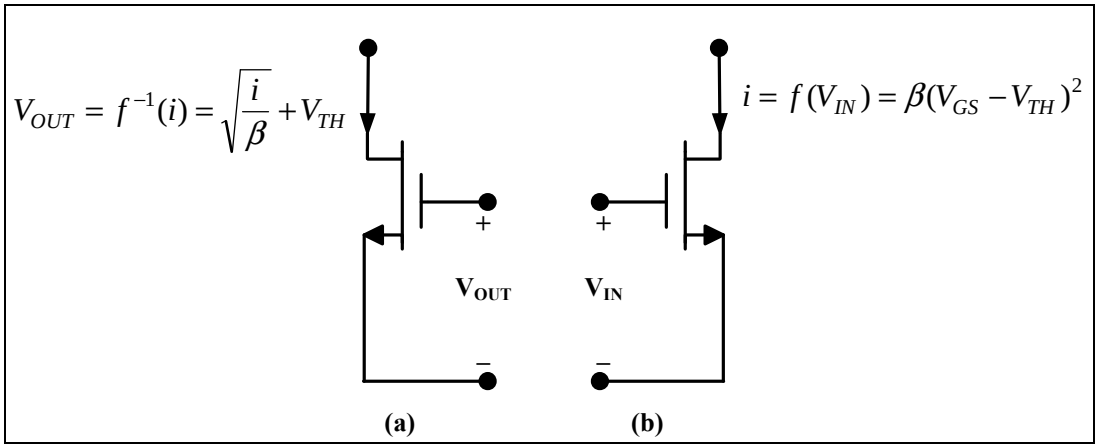

Figure 1. 1 (a) Compressor, (b) Expander

Square root domain circuits, which are externally linear internally nonlinear (ELIN) circuits, mainly exhibits following features; high speed due to designable in current mode, tunability due to applied bias current, high linearity, needing only capacitors and transistors during the design, low-voltage/low power consumption, large dynamic range, and low fabrication cost.

Synthesis methods for square root domain circuits can be arranged as state space synthesis, signal flow graph synthesis, and the substitution of the LC ladder of the corresponding prototype by their square root domain equivalents in the literature (Eskiyerli &Payne, 2000; Psychalinos, 2008; Vlassis & Psychalinos, 2002; Tsividis, 1990). In this dissertation, the state space synthesis method, in which the state space

description of the transfer function is mapped on the state variables was used. This method is also very powerful and efficient approach for externally linear internally nonlinear circuits like square root domain circuits (Kırçay & Çam, 2008)

In this dissertation, it is aimed to propose new square-root domain filters and oscillators designed by using state space synthesis method. In this direction, this thesis is organized as follows.

In Chapter 2, general knowledge about MOS transistors, MOS translinear principle with its topologies as stacked and up-down, state space synthesis method with its derivations are given. Geometric mean circuit that is a basic block of square root domain circuits is also given and simulated in this chapter.

In Chapter 3, first order lowpass filter is presented. This filter also exists in the literature but the presented has simpler structure. In this chapter, lossless integrator, first order highpass and allpass filters are proposed for the first time in the literature.

In Chapter 4, second order lowpass and second order bandpass filters are introduced in simpler structures than these reported in the literature. Second order highpass, second order notch, second order allpass, KHN biquad, and Tow-Thomas biquad filter are proposed as bringing novelty into the literature.

In Chapter 5, 5^{th} order Butterworth lowpass filter, which is appropriate to be used in Wi-Fi and Bluetooth receivers and quadrature oscillator are proposed for the first time in the literature. And also an oscillator designed by using state space synthesis method is presented. All circuits are simulated in many analyses types as frequency, transient, Monte Carlo. Finally, in Chapter 6, the conclusion and future work are given.

CHAPTER TWO
BACKGROUND FOR THE DESIGN OF SQUARE ROOT DOMAIN CIRCUITS

Square root domain circuits are based on the quadratic relationship between drain current and gate-source voltage of MOSFET (metal oxide semiconductor field effect transistor) operated in saturation region and MOS translinear principle. In this regard, operating regions of MOS transistors and MOS translinear principle and state space synthesis method are explained in this chapter. Besides, geometric mean circuit is a basic block for square root domain circuits. Geometric mean circuit, which is used in all designs in the thesis, is presented and simulated in this chapter.

2.1 Operating Regions of Metal Oxide Semiconductor Field Effect Transistor

MOSFET is the most prominent type of field effect transistors. Due to relatively simple manufacturing process, requiring quite small silicon area on the IC chip in consequence of low cost, compatibility with popular CMOS VLSI technology, low power dissipation, MOSFETs have become prevailing in the area of both analog integrated and digital integrated circuit design. There are several circuit design methods according to operating region of MOSFETs. They have three operating regions;

1. weak inversion
2. ohmic/triode region (linear region)
3. Pinch-off region (saturation region)

When the gate-source voltage, V_{GS}, is less than the threshold voltage, V_{TH}, the MOS transistor operates in weak inversion. In this region, n-channel MOS transistor behaves as an npn bipolar transistor, where the source acts as a emitter, the substrate as the base, the drain as the collector (Gray, Hurts, Lewis, and Meyer, 2001). The drain current of MOS transistor in weak inversion is

$$I_D = \frac{W}{L} I_T e^{\left(\frac{V_{GS}-V_{TH}}{nV_{TH}}\right)} \left[1 - e^{\left(-\frac{V_{DS}}{V_{TH}}\right)}\right] \tag{2.1}$$

where

W : transistor width,

L : transistor length,

I_T : drain current when $V_{GS} = V_{TH}$,

n : $1 + \frac{C_{JS}}{C_{OX}}$, where C_{JS} , C_{OX} are depletion-region capacitance, oxide capacitance per unit area, respectively,

V_{DS} : drain-source voltage.

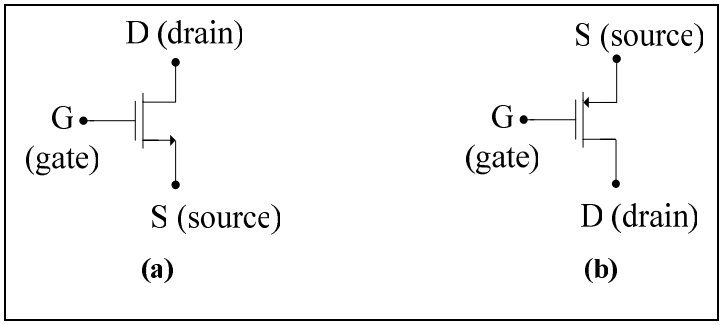

Figure 2. 1 (a) N-channel MOS (NMOS) transistor, (b) P-channel MOS (PMOS) transistor

When V_{DS} is less than $V_{GS} - V_{TH}$, the device operates in the ohmic region. In this region, the transistor can be modeled as a nonlinear voltage-controlled resistor connected between the drain and source. The drain current of MOS transistor in ohmic region is;

$$I_D = \frac{\mu C_{OX}}{2} \frac{W}{L} \left[2(V_{GS} - V_{TH}) V_{DS} - V_{DS}^2 \right] \tag{2.2}$$

Since V_{DS} is small, V_{DS}^2 is also small, so the drain current equation becomes a linear equation, hence that's why this region is sometimes called linear region.

The MOS transistor operates in the pinch-off region, known as saturation region, when V_{DS} is greater than $V_{GS} - V_{TH}$. In the saturation region, the drain current is

$$I_D = \frac{\mu C_{OX}}{2} \frac{W}{L} (V_{GS} - V_{TH})^2 = \beta (V_{GS} - V_{TH})^2 \tag{2.3}$$

where $\beta = \frac{\mu C_{OX}}{2}\frac{W}{L}$ is called transconductance parameter. The drain current equation in (2.3) known as MOS square law is legitimate for ideal case, second order effects like the body effect, mobility reduction, channel length modulation are neglected. The MOS square law paves the way for designing of square root domain circuits.

2.2 The MOS Translinear Principle

The translinear circuit principle was originally formulated by Gilbert in 1975 as meaning of implementing nonlinear signal processing functions by bipolar transistor circuits. The translinear circuit, namely transconductance linear, is based on exponential relation between voltage and current property of bipolar transistor. By trending the CMOS analog circuit techniques, this circuit principle was applied to MOS transistors in weak inversion by accepting exponential voltage-current characteristics (Vittoz & Fellrath, 1977). Because of low dynamic range and low speed for general application due to the limitations of MOS transistor in weak inversion, the translinear principle was applied to MOS transistors operating in saturation region (Bult and Wallinga, 1987). In consequence of these developments, the translinear principle was generalized as applying to devices having transconductance linear with electrical variable such as current or voltage by Seevinck and Wiegerink in 1991. Translinear circuits containing bipolar transistors are called bipolar translinear (BTL), and translinear circuits containing MOS transistors are called MOS translinear (MTL) circuits (Wiegerink,1993).

MTL circuits are based on loop containing equal numbers of one type (n-type or p-type) transistors arranged clockwise (CW) and counterclockwise (CCW). Figure 2.2 shows NMOS translinear circuit containing four identical NMOS transistors.

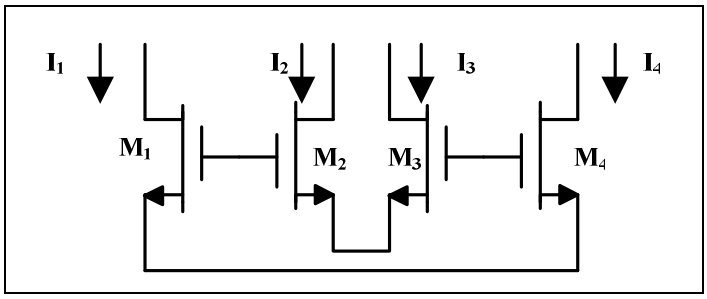

Figure 2. 2 Four transistor NMOS translinear circuit

By using Kirchhoff's voltage law, the equation of gate-source voltages in the counter clock-wise direction as;

$$V_{GS1} - V_{GS4} + V_{GS3} - V_{GS2} = 0 \tag{2.4}$$

The gate-source voltage (V_{GS}) is obtained by arranging the Equation (2.3)

$$V_{GS} = \sqrt{\frac{I}{\beta}} + V_{TH} \tag{2.5}$$

By substituting V_{GS} equation into Equation (2.5), result is

$$V_{TH1} + \sqrt{\frac{I_{D1}}{\beta_1}} + V_{TH3} + \sqrt{\frac{I_{D3}}{\beta_3}} = V_{TH2} + \sqrt{\frac{I_{D2}}{\beta_2}} + V_{TH4} + \sqrt{\frac{I_{D4}}{\beta_4}} \tag{2.6}$$

Due to cancellation of threshold voltage terms in both sides, the MLT principle can be stated as; the sum of the square roots of the drain currents divided by the transconductance parameters in the clock-wise direction is equal to the sum of the square roots of the drain current divided by the transconductance parameters in the counter clock-wise direction.

A simple linear transconductor circuit proposed by Bult and Wallingra in 1987 is shown in Figure 2.3. If it is considered that all transistors are identical and operating in saturation region, drain current of M_2 is;

$$I_{D2} = \beta(V_{GS2} - V_{TH})^2 \tag{2.7}$$

and drain current of M_3 is;

$$I_{D3} = \beta(V_{IN} - V_{TH})^2 \tag{2.8}$$

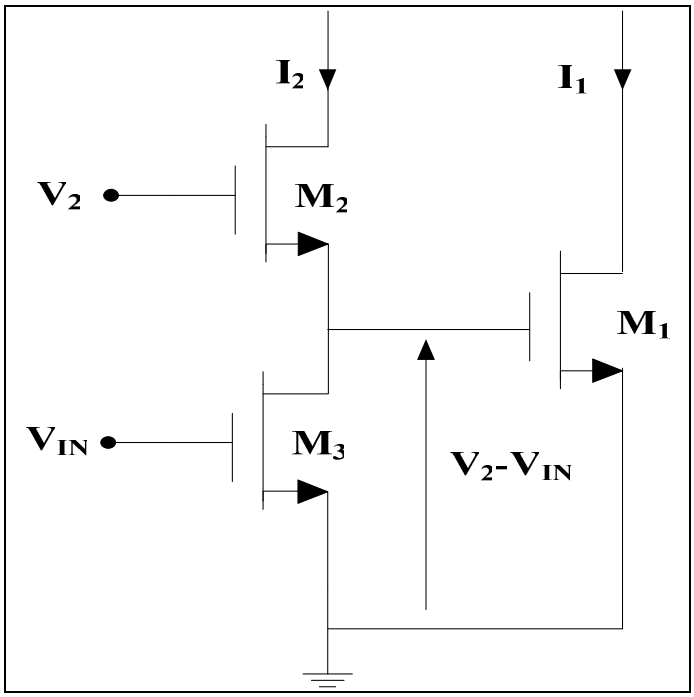

Figure 2. 3 A linear transconductor circuit

Furthermore, because both of these two currents equal to each other equality of these gate-source voltages of M_2 and M_3 are the same. So V_{IN} is equal to V_{GS2}. Consequently, output current;

$$I_1 - I_2 = \beta(V_2 - 2V_{TH}).(V_2 - 2V_{IN}) \tag{2.9}$$

The circuit in Figure 2.3 is presented as linear V-I converter by Bult and Walling in 1987, due to the linear relationship between output current and input voltage. Also this linear transconductor is very common useful structure for square-root domain circuits to take difference between voltages.

MOS translinear circuits have two practical translinear loop topologies: stacked and up-down (Wiegerink, 1993). These topologies for a loop of four transistors are indicated in Figure 2.4. Both topologies in this figure realize the same equation:

$$\sqrt{\frac{I_1}{\beta_1}} + \sqrt{\frac{I_2}{\beta_2}} = \sqrt{\frac{I_3}{\beta_3}} + \sqrt{\frac{I_4}{\beta_4}} \tag{2.10}$$

Although both loop topologies shows same results in ideal case, considering the second order effects, they exhibit worthy of notice differences. Body effect is more

influential in stacked loop topology. According to circuit complexity, the stacked one result in compact circuits and any loop equation can be easily implemented in such a topology. On the other hand, some extra circuitry is needed into the up-down to loop to force the desired currents.

MOS translinear topologies are used in squarer/divider, multiplier, geometric mean circuits.

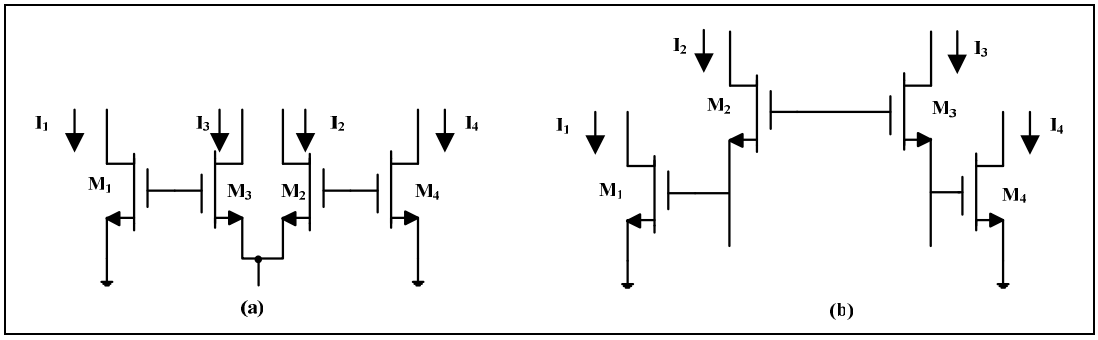

Figure 2. 4 (a) Stacked translinear loop, (b) Up-down translinear loop

2.3 Geometric Mean Circuit

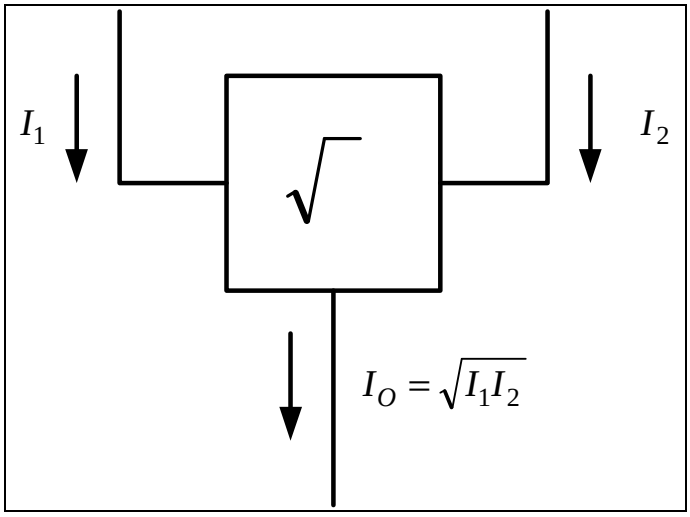

Figure 2. 5 Geometric mean circuit symbol

In implementation of square root domain circuits, two different nonlinear functions, geometric mean and current squarer/divider, are required (Eskiyerli & Payne, 2000). In this thesis, according to the design procedure of square root domain circuit, geometric mean circuit was used.

The geometric mean circuits can be implemented by using stacked and up-down topologies. The basic geometric mean circuit with stacked MOS translinear topology (Wiegerink, 1993) is shown in Figure 2.6.

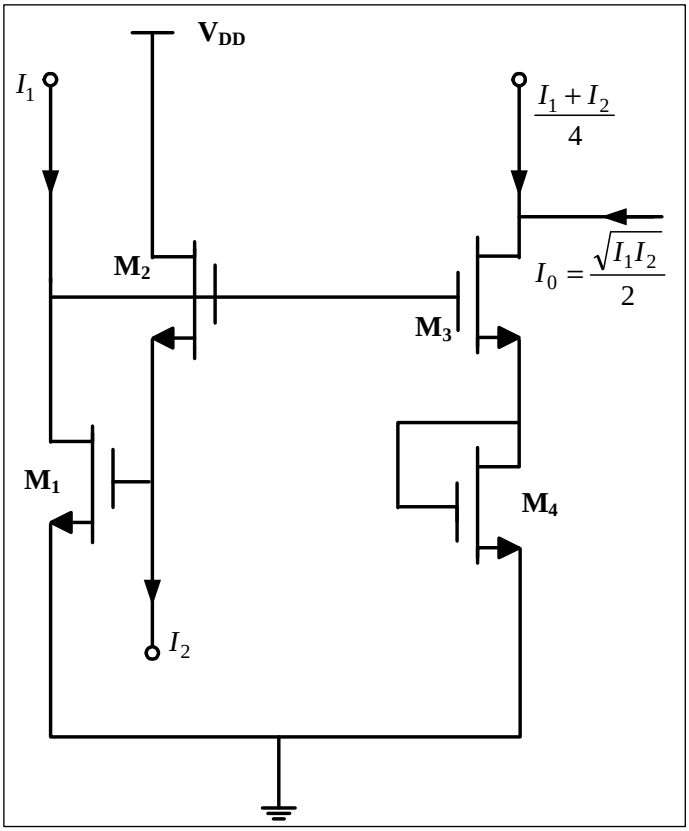

Figure 2. 6 The basic geometric mean circuit

If it is assumed that all transistors in Figure 2.6 are identical, transconductance parameters β and threshold voltage V_{TH} are the same. The relationship between currents is;

$$\sqrt{I_{D1}} + \sqrt{I_{D2}} = \sqrt{I_{D3}} + \sqrt{I_{D4}} \tag{2.11}$$

By substituting external current sources in Equation (2.8);

$$\sqrt{I_1}+\sqrt{I_2}=2.\sqrt{\frac{I_1+I_2}{4}+I_0} \tag{2.12}$$

After some arrangements the output current I_0 is obtained

$$I_0=\frac{\sqrt{I_1 I_2}}{2} \tag{2.13}$$

If transconductance parameters of M_3 and M_4 are taken as two times of transconductance of M_1 and M_2, and drain current of M_3 is assumed as $I_0+\frac{I_1+I_2}{2}$, the output current becomes as

$$I_0=\sqrt{I_1 I_2} \tag{2.14}$$

The geometric mean circuit which is used by Yu and others in 2005, is more complicated than the basic configuration and has advantage when the half value of currents does not applied externally. M_{17} and M_{18} transistors in the circuit are connected to change the direction of the geometric mean of the currents; if these transistors are placed in the schematic the output current direction is outward, if these transistors are disconnected; output current is drain current of M_{16} transistor, the output current direction is inward.

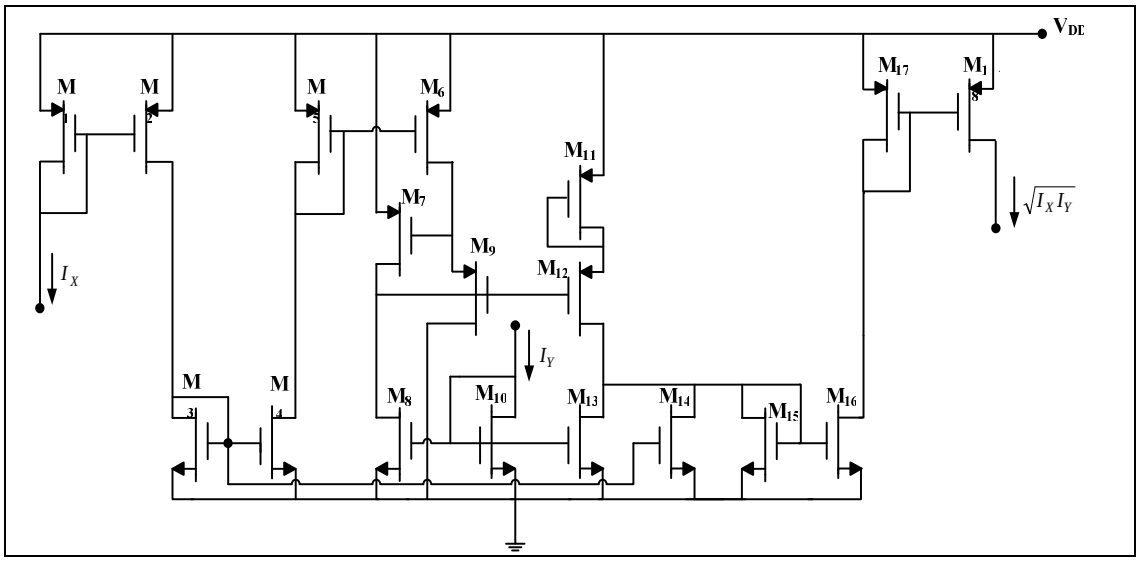

Figure 2. 7 Geometric mean circuit used in this thesis

In the simulation, supply voltage of the circuit was chosen as 2.5V in TSMC 0.25 CMOS process. I_X current was 1μA and I_Y current was triangle source with 1μA amplitude. During the simulation the aspect ratios of transistors W/L=7 μm/ 0.7 μm except W/L = 3.5 μm/ 0.7 μm for transistors M_{13} and M_{14}.

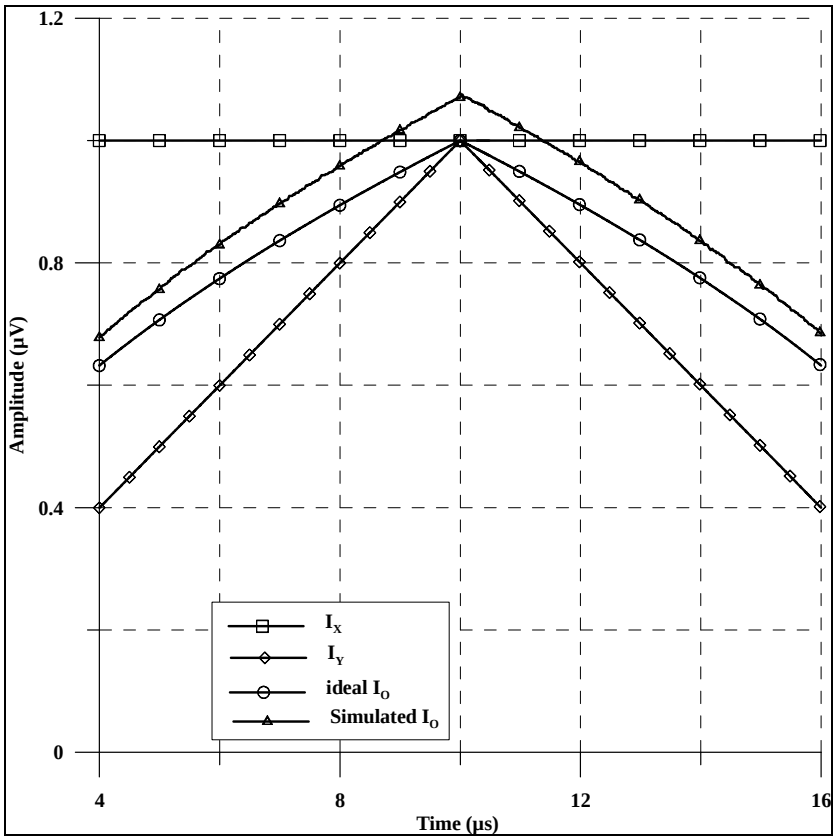

Figure 2. 8 Simulation results of geometric mean circuit

2.4 State Space Synthesis Method for Square-Root Domain Circuits

As mentioned before, there are different synthesis methods for square root domain circuits as state space synthesis, signal flow graph synthesis, and the substitution of the LC ladder of the corresponding prototype by their square root domain equivalents in the literature (Psychalinos, 2007; Psychalinos & Vlassis, 2002).

It is known that square-root domain circuits are externally linear internally nonlinear circuits (ELIN) as log-domain circuits. In ELIN circuits, linear state-space models are used to realize any unknown externally linear systems. State space

synthesis method is very powerful and efficient approach in the synthesis of this type of circuits (Frey, 1993). The method can be also applied for nonlinear systems, time invariant systems, current mode circuits, systematic synthesis and computer aided design (Lathi, 1992) In this thesis, state-space synthesis method was used.

The state-space synthesis method can be briefly reviewed and summarized for square-root domain circuits as follows;

1. Find the appropriate state space description for a system.
2. Make a quadratic mapping function to the input and state variables.
3. Manipulate the equation to obtain a set of nodal equations.
4. Design the circuit using transistors, grounded capacitors, and current sources (Tola & Frey, 2000; Kırçay and Çam, 2006).

Any linear transfer function H(s) can be represented by a set of linear state equations;

$$sX(s) = AX(s) + BU(s) \tag{2.15}$$

$$Y(s) = CX(s) + DU(s) \tag{2.16}$$

A, *B*, *C*, and *D* matrices are coefficient matrices, *X(s)* is a state variable, *U(s)* is input, and *Y(s)* is output in frequency domain. Various techniques can be used to determine the state- variable representation of a given transfer function, but all of them are functionally equivalent.

2.4.1 The Companion Form Technique

The companion form technique is one of the methods to obtain the state space representation of a transfer function. In general the transfer function of the nth order system is;

$$H(s) = \frac{Y(s)}{U(s)} = \frac{b_0 s^n + b_1 s^{n-1} + ...b_{n-1}s + b_n}{s^n + a_1 s^{n-1} + ...a_{n-1}s + a_n} \tag{2.17}$$

According to the b_i coefficients different type of filters are obtained as lowpass, highpass, bandpass, notch, and allpass filters. If the transfer function is rewritten in the time domain, nth order differential equation is;

$$y^{(n)} + a_1 y^{(n-1)} + \ldots\ldots\ldots + a_{n-1}\dot{y} + a_n y = b_0 u^{(n)} + b_1 u^{(n-1)} + \ldots\ldots\ldots + b_{n-1}\dot{u} + b_n u \qquad (2.18)$$

In the companion form technique, to obtain state and output equations two situations is considered (Ogata, 2009).

2.4.1.1 State Space Representation not Involved Derivative Terms of Input

If the b_i coefficients are zero except b_n in the nth order system, differential equation in (2.14) becomes

$$y^{(n)} + a_1 y^{(n-1)} + \ldots\ldots\ldots + a_{n-1}\dot{y} + a_n y = b_n u \qquad (2.19)$$

Under these conditions, by assuming that;

$$\begin{aligned} x_1 &= y \\ x_2 &= \dot{y} \\ &\cdot \\ &\cdot \\ &\cdot \\ x_{n-1} &= y^{(n-2)} \\ x_n &= y^{(n-1)} \end{aligned} \qquad (2.20)$$

The state variable's equations and output equation are obtained as follows by taking the derivative of the state variables and substituting the derivatives of output from the transfer function and delay state equations.

$$\begin{aligned} \dot{x}_1 &= x_2 \\ \dot{x}_2 &= x_3 \\ &\cdot \\ &\cdot \\ &\cdot \\ \dot{x}_{n-1} &= x_n \\ \dot{x}_n &= -a_n x_1 - \ldots\ldots\ldots - a_1 x_n + b_n u \end{aligned} \qquad (2.21)$$

So, the state equation in time domain,

$$\dot{x} = Ax + Bu \qquad (2.22)$$

where

$$x=\begin{bmatrix} x_1 \\ x_2 \\ . \\ . \\ . \\ x_{n-1} \\ x_n \end{bmatrix},\ A=\begin{bmatrix} 0 & 1 & 0 & ... & 0 \\ 0 & 0 & 1 & ... & 0 \\ . & . & . & & . \\ . & . & . & & . \\ . & . & . & . & . \\ 0 & 0 & 0 & ... & 1 \\ -a_n & -a_{n-1} & -a_{n-2} & ... & -a_1 \end{bmatrix},\ B=\begin{bmatrix} 0 \\ 0 \\ . \\ . \\ . \\ 0 \\ b_n \end{bmatrix},$$

and the output equation,

$$y = Cx + Du \tag{2.23}$$

where

$$C=\begin{bmatrix}1 & 0 & . & . & . & 0 & 0\end{bmatrix},\ x=\begin{bmatrix} x_1 \\ x_2 \\ . \\ . \\ . \\ x_{n-1} \\ x_n \end{bmatrix}.$$

In this situation *D* is zero and the system is first order.

2.4.1.2 State Space Representation Involved Derivative Terms of Input

If the transfer function involves derivative terms of input, differential equation in (2.15) is used. To obtain the state equations, there are many choices to determine the A, B, C, and D matrixes in state space representation. In the way mentioned by Ogata, state equations includes derivative of inputs as;

$$\begin{aligned} x_1 &= y - \beta_0 u \\ x_2 &= \dot{y} - \beta_0 \dot{u} - \beta_1 u = \dot{x}_1 - \beta_1 u \\ &. \\ &. \\ &. \\ x_{n-1} &= y^{(n-2)} - \beta_0 u^{(n-2)} - \beta_1 u^{(n-3)} - ..... - \beta_{n-2} u = \dot{x}_{n-2} - \beta_{n-2} u \\ x_n &= y^{(n-1)} - \beta_0 u^{(n-1)} - \beta_1 u^{(n-2)} - ..... - \beta_{n-2} \dot{u} - \beta_{n-1} u = \dot{x}_{n-1} - \beta_{n-1} u \end{aligned} \tag{2.24}$$

where $\beta_0, \beta_1, \beta_2, \ldots\ldots \beta_{n-2}, \beta_{n-1}$ are determined from

$$
\begin{aligned}
&\beta_0 = b_0 \\
&\beta_1 = b_1 - a_1\beta_0 \\
&\beta_2 = b_2 - a_1\beta_1 - a_2\beta_0 \\
&. \\
&. \\
&. \\
&\beta_{n-1} = b_{n-1} - a_1\beta_{n-2} - \ldots\ldots\ldots - a_{n-2}\beta_1 - a_{n-1}\beta_0
\end{aligned}
\tag{2.25}
$$

By using the prevalent β parameters, the state variables are obtained as

$$
\begin{aligned}
&\dot{x}_1 = x_2 + \beta_1 u \\
&\dot{x}_2 = x_3 + \beta_2 u \\
&. \\
&. \\
&. \\
&\dot{x}_{n-1} = x_n + \beta_{(n-1)} u \\
&\dot{x}_n = -a_n x_1 - a_{n-1} x_2 - \ldots\ldots - a_1 x_n + \beta_n u
\end{aligned}
\tag{2.26}
$$

where β_n is given by

$$\beta_n = b_n - a_1\beta_{n-1} - \ldots\ldots\ldots - a_{n-1}\beta_1 - a_{n-1}\beta_0 \tag{2.27}$$

So, the state equation in time domain,

$$\dot{x} = Ax + Bu \tag{2.28}$$

where

$$
x = \begin{bmatrix} x_1 \\ x_2 \\ . \\ . \\ . \\ x_{n-1} \\ x_n \end{bmatrix}, \quad
A = \begin{bmatrix} 0 & 1 & 0 & \ldots & 0 \\ 0 & 0 & 1 & \ldots & 0 \\ . & . & . & & . \\ . & . & . & & . \\ . & . & . & . & . \\ 0 & 0 & 0 & \ldots & 1 \\ -a_n & -a_{n-1} & -a_{n-2} & \ldots & -a_1 \end{bmatrix}, \quad
B = \begin{bmatrix} \beta_1 \\ \beta_2 \\ . \\ . \\ . \\ \beta_{n-1} \\ \beta_n \end{bmatrix},
$$

and the output equation,

$$y = Cx + Du \tag{2.29}$$

where

$$C = \begin{bmatrix} 1 & 0 & . & . & . & 0 & 0 \end{bmatrix},\quad x = \begin{bmatrix} x_1 \\ x_2 \\ . \\ . \\ . \\ x_{n-1} \\ x_n \end{bmatrix},\quad D = \beta_0 = b_0 .$$

During the circuit design, it is known that the coefficients of the state and input variables determine currents and voltages of devices. Since the each device has some limited current and/or voltage range, if these coefficients are out of the range, this kind of circuit are not realizable. From this point of view Arslanalp and Tola were presented a modified companion form technique in 2006. In this method, state variables are multiplied with arbitrary coefficients;

$$\begin{aligned}
&\alpha_1 x_1 = ky - \beta_0 u \\
&\alpha_2 x_2 = \alpha_1 \dot{x}_1 - \beta_1 u = k\dot{y} - \beta_0 \dot{u} - \beta_1 u \\
&. \\
&. \\
&. \\
&\alpha_{n-1} x_{n-1} = k\overset{(n-2)}{y} - \beta_0 \overset{(n-2)}{u} - \beta_1 \overset{(n-3)}{u} - \ldots\ldots\ldots - \beta_{n-2} u = \alpha_{n-2} \dot{x}_{n-2} - \beta_{n-2} u \\
&\alpha_n . x_n = k\overset{(n-1)}{y} - \beta_0 . \overset{(n-1)}{u} - \beta_1 . \overset{(n-2)}{u} - \ldots\ldots\ldots - \beta_{n-2} . \dot{u} - \beta_{n-1} . u = \alpha_{n-1} . \dot{x}_{n-1} - \beta_{n-1} . u
\end{aligned} \tag{2.30}$$

By choosing values of these coefficients, the state equations become compatible for circuit design.

2.4.2 Canonical Forms

Another method to obtain state space representation is to use the canonical forms; observable canonical form and controllable canonical form. Observable and controllable canonical forms are often used when modeling starting from input-output description or in pole placement design (Moscinski and Ogonowski,1995).

These two canonical forms provide appropriate state space representation to realize square root domain circuits.

2.4.2.1 Observable Canonical Form

For nth order differential equation in Equation (2.18), the state equation is

$$\dot{x} = Ax + Bu \tag{2.31}$$

where

$$x = \begin{bmatrix} x_1 \\ x_2 \\ . \\ . \\ . \\ x_{n-1} \\ x_n \end{bmatrix}, \; A = \begin{bmatrix} 0 & 0 & 0 & ... & 0 & -a_n \\ 1 & 0 & 0 & ... & 0 & -a_{n-1} \\ . & . & . & ... & . & . \\ . & . & . & ... & . & . \\ . & . & . & . & . & . \\ 0 & 0 & 0 & ... & 0 & -a_2 \\ 0 & 0 & 0 & ... & 1 & -a_1 \end{bmatrix}, \; B = \begin{bmatrix} (b_n - b_0.a_n) \\ . \\ . \\ . \\ . \\ (b_2 - b_0.a_2) \\ (b_1 - b_0.a_1) \end{bmatrix},$$

and the output equation is,

$$y = Cx + Du \tag{2.32}$$

where

$$C = \begin{bmatrix} 0 & 0 & . & . & . & 0 & 1 \end{bmatrix}, \; x = \begin{bmatrix} x_1 \\ x_2 \\ . \\ . \\ . \\ x_{n-1} \\ x_n \end{bmatrix}, \; D = b_0 .$$

in observable canonical form.

2.4.2.2 Controllable Canonical Form

For nth order differential equation in Equation (2.15), the state equation is

$$\dot{x} = Ax + Bu \tag{2.33}$$

where

$$x=\begin{bmatrix} x_1 \\ x_2 \\ . \\ . \\ . \\ x_{n-1} \\ x_n \end{bmatrix},\ A=\begin{bmatrix} 0 & 1 & 0 & ... & 0 \\ 0 & 0 & 1 & ... & 0 \\ . & . & . & & . \\ . & . & . & & . \\ . & . & . & . & . \\ 0 & 0 & 0 & ... & 1 \\ -a_n & -a_{n-1} & -a_{n-2} & ... & -a_1 \end{bmatrix},\ B=\begin{bmatrix} 0 \\ 0 \\ . \\ . \\ . \\ 0 \\ 1 \end{bmatrix},$$

and the output equation is,

$$y = Cx + Du \tag{2.34}$$

where

$$C=\begin{bmatrix}(b_n - b_0.a_n) & (b_{n-1} - b_0.a_{n-1}) & . & . & . & (b_2 - b_0.a_2) & (b_1 - b_0.a_1)\end{bmatrix},\ x=\begin{bmatrix} x_1 \\ x_2 \\ . \\ . \\ . \\ x_{n-1} \\ x_n \end{bmatrix},$$

$$D = b_0 .$$

in controllable canonical form.

CHAPTER THREE
SQUARE ROOT DOMAIN FIRST ORDER CIRCUITS

In this chapter, lossless integrator, first order highpass filter, and first order allpass filter designed by using state space synthesis method in square root domain are proposed for the first time in the literature. First order lowpass which is introduced before in the literature, is presented that is designed by using different state space equations. All circuits are simulated by using PSpice simulation program.

3.1 Lossless Integrator

Lossless integrator circuit is a useful basic element of integrated circuit filters. By combining lossless integrators and another circuit block, biquad filters and high order filters can be realized. The transfer function of the lossless integrator is

$$H(s) = \frac{k}{s} \tag{3.1}$$

where k is scaling factor. To make appropriate the lossless integrator to realization of biquad filters and high order filters, k can be chosen $\pm\omega_0 Q$ or $\pm\omega_0/Q$ where ω_0 is natural frequency and Q is the quality factor, respectively. In the literature, there are many lossless integrator circuit designed with OTA (Sinencio, Geiger, and Lozano, 1998), current differential amplifiers (Souliotis, Chrisanthopoulos and Haritantis, 2001). In square root domain, lossless integrator designed by using signal flow graph approach was presented by Psychalinos and Vlassis in 2002 and by using state space synthesis was presented by Ölmez and Çam in 2009. To predispose the lossless integrator to biquad filters, the transfer function is chosen as

$$H(s) = \frac{\omega_0 / Q}{s} \tag{3.2}$$

where ω_0, Q are natural frequency and quality factor, respectively. The state space representation obtained by using companion form technique is expressed as

$$\dot{x} = \frac{\omega_0}{Q} u \tag{3.3}$$

$$y = x$$

If the node voltage V_1 and voltage signal U are assumed the state variable x and input u, state and output equations in (3.3) are rewritten as

$$C\dot{V}_1 = \frac{C\omega_0 U}{Q} \tag{3.4}$$

$$y = V_1$$

where C is a capacitor value seemed multiplying factor. By assuming that U is gate-source voltages of MOS transistor operating in saturation region with its drain current is defined as I_u and $C\dot{V}_1 = I_C$ is current of the capacitor Equation (3.4) is arranged that

$$I_C = \frac{C\omega_0}{Q}\left(\sqrt{\frac{I_u}{\beta}} + V_{TH}\right) \tag{3.5}$$

where $I_u=\beta(U-V_{TH})^2$. Hence, the state equation in (3.5) is transformed into

$$I_C = \frac{1}{Q}\sqrt{I_0 I_u} + \frac{1}{Q} I_{TH} \tag{3.6}$$

where the bias current $I_0 = (\omega_0{}^2 C^2)/\beta$, and threshold voltage compensation current $I_{TH}=\omega_0 C V_{TH}$. The square root domain lossless integrator consisting of a geometric mean circuit, a current mirror, a capacitor is shown in Figure 3.1.

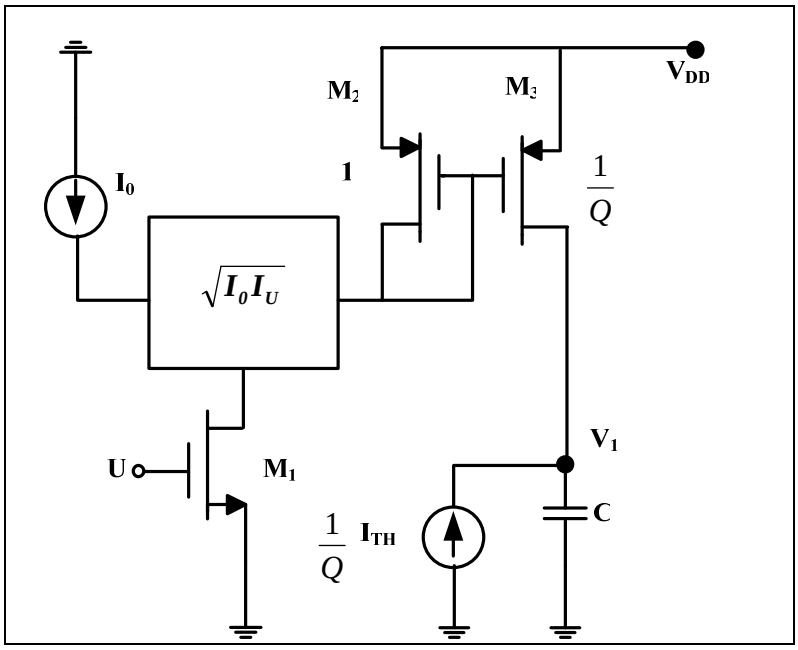

Figure 3. 1 The lossless integrator circuit

To implement the lossless integrator circuit, D.C. operating points must be considered. By assuming that the state variable *x* has D.C. term V_1 and A.C. term v_1 and similarly the input *u* has D.C. term *U* and A.C. term *u* (Chen, 2003), state equation in Equation (3.4) is rearranged as

$$C(\dot{V}_1 + \dot{v}_1) = \frac{C\omega_0(U+u)}{Q} \tag{3.7}$$

When D.C. terms and A.C. terms are separated, the state equation is

$$C\dot{V}_1 + C\dot{v}_1 = \frac{C\omega_0 U}{Q} + \frac{C\omega_0 u}{Q} \tag{3.8}$$

In D.C. operating point analysis, current of a capacitor must be zero. So, the D.C. terms must also be equal to zero. To equate the D.C. terms of Equation (3.8) to zero a D.C. current is added

$$C\dot{V}_1 = \frac{C\omega_0 U}{Q} + I_{DC} = 0 \tag{3.9}$$

where $I_{DC}=-(C\omega_0 U)/Q$. By substituting the D.C. current source in Equation (3.6)

$$I_C = \frac{1}{Q}\sqrt{I_0 I_u} + \frac{1}{Q} I_{TH} + I_{DC} = \frac{1}{Q}\sqrt{I_0 I_u} + \frac{1}{Q} I_{TH} - \frac{C\omega_0 U}{Q} \tag{3.10}$$

Due to I_{TH} is also a DC current source, an external current source I_{bias} added to state equation is

$$I_{bias} = \frac{1}{Q} C\omega_0 V_{TH} - \frac{C\omega_0 U}{Q} \tag{3.11}$$

According to adjustments, the D.C. current source applied to V_1 node is changed with the I_{bias} current source. The quality factor can be adjusted by changing W/L ratio of M_3 transistor and value of I_{bias} current source.

Similarly, to make appropriate lossless integrator to biquad filters, the transfer function can be chosen as

$$H(s) = \frac{\omega_0 Q}{s} \tag{3.12}$$

By using companion form technique, the state space representation is obtained as

$$\dot{x} = Q\omega_0 u \tag{3.13}$$

$$y = x$$

While same design steps for first lossless integrator are followed, second lossless integrator is designed with state equations as follows

$$I_C = Q\sqrt{I_0 I_u} + QI_{TH} \tag{3.14}$$

$$y = V_1$$

where $I_u=\beta(U-V_{TH})^2$, $I_0 = (\omega_0{}^2 C^2)/\beta$, and $I_{TH} = \omega_0 C V_{TH}$. The second lossless integrator circuit under these state equations is shown in Figure 3.2.

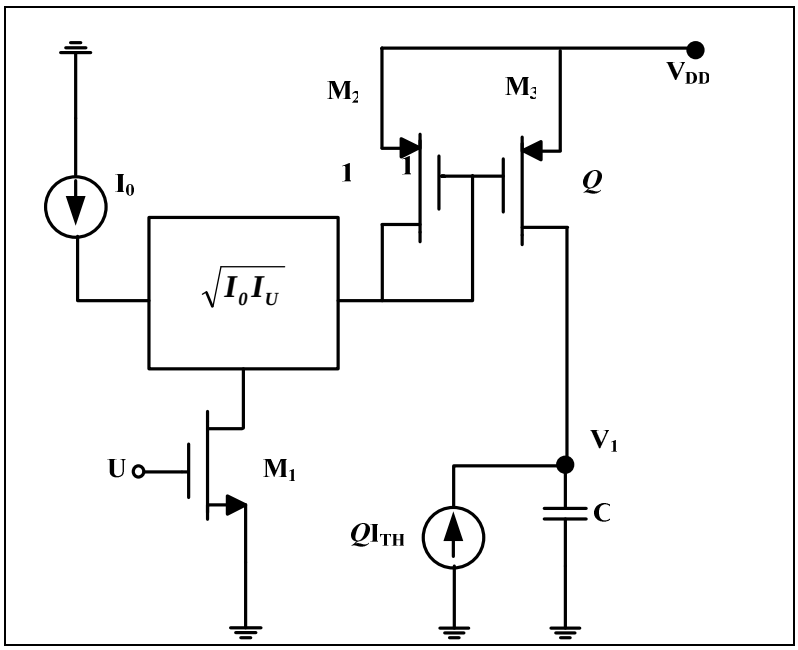

Figure 3. 2 Second lossless integrator circuit

Similarly to first lossless integrator circuit, to provide D.C. conditions, a bias current is added to state equation as $I_{bias}=QC\omega_0 V_{TH}$ - $QC\omega_0 U$ and this current is changed with QI_{TH} current source.

By using TSMC 0.25µm CMOS Level 3 model parameters (Appendix), the proposed first lossless integrator was simulated with values of integrator parameters given in Table 3.1. Under these conditions, theoretical natural frequency is 1.87MHz while simulated is 1.84MHz. Gain and phase responses of the proposed lossless integrator are indicated in Figure 3.3 and Figure 3.4, respectively.

Table 3. 1 The parameters of the proposed first lossless integrator

Parameter values	
Q	1
V_{DD}	2.5V
U (D.C. voltage)	0.7V
C	7pF
I_0	70μA
I_{bias}	27.2μA
Aspect ratio of transistor M_1	7μm/7μm
Aspect ratios of transistors M_2 and M_3	1μm/7μm

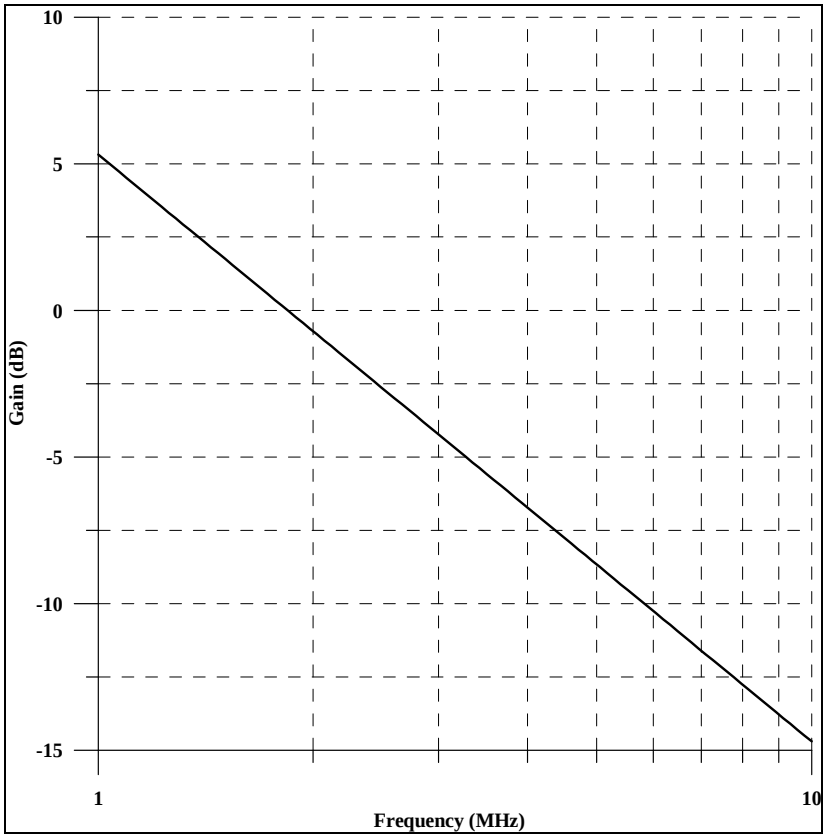

Figure 3. 3 Gain response of the proposed first lossless integrator

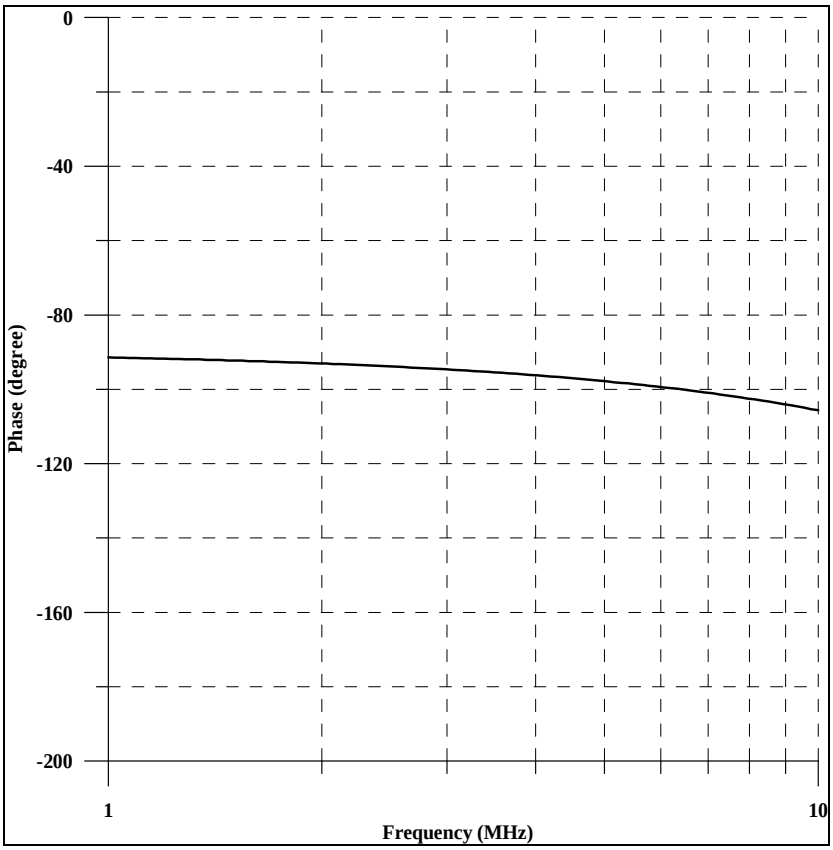

Figure 3. 4 Phase responses of the proposed first lossless integrator

When input sinusoidal amplitude was 10mV at 1.87MHz, bias current was 70µA the time response of the lossless integrator was simulated as given in Figure 3.5. This causes 139ns time delay at the output of the integrator corresponding to 93.5° phase difference. As it is seen from the equations, the natural frequency and quality factor are tunable. So to verify the theoretical study, the cut-off frequency and the quality factor were varied by adjusting the bias current and by adjusting the aspect ratios of M_3 transistor and value of I_{bias} current source, respectively. Electronically tunable gain response of the proposed filter for six different bias currents, from 40 µA to 90 µA, is depicted in Figure 3.6. Figure 3.7 shows the gain response of the lossless integrator, while quality factor is 0.1, 0.5, 1, 5, and 10.

The dependence of the output harmonic distortion of lossless integrator on input signal amplitude was illustrated in Figure 3.8. As shown in this Figure, THD increases with input signal. As such, input signal must be 340 mV or less to avoid output distortion.

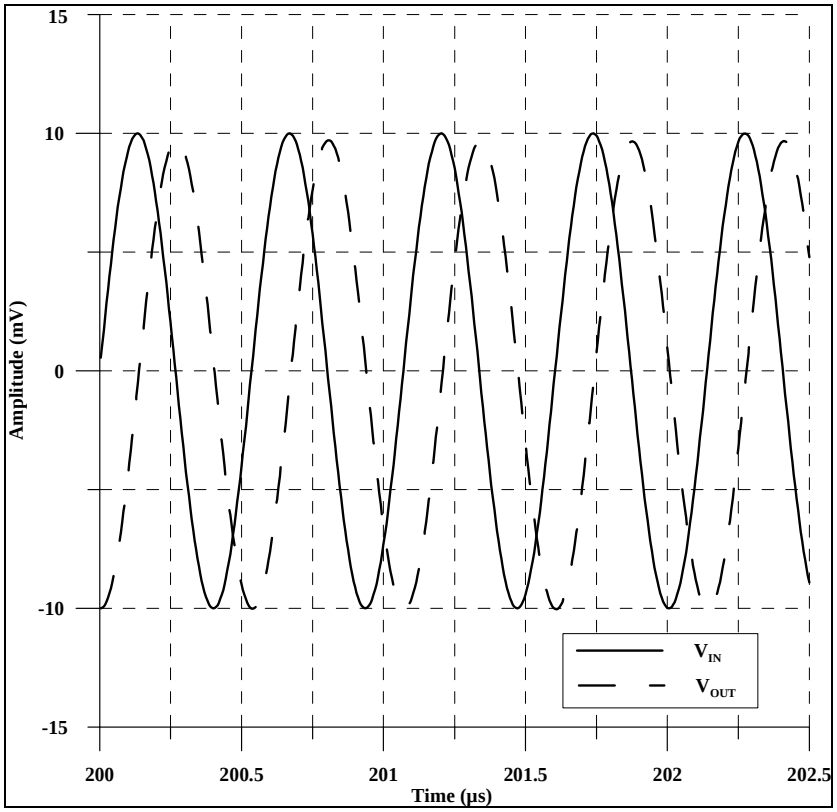

Figure 3. 5 The time response of the proposed lossless integrator

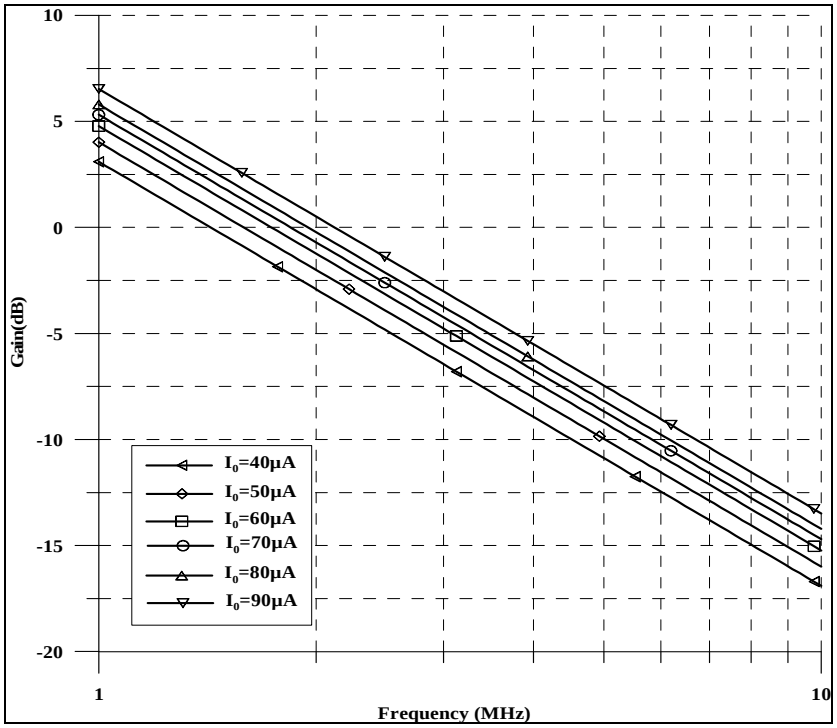

Figure 3. 6 The phase response of the proposed lossless integrator for I_0 is 40µA, 50µA, 60µA, 70µA, 80µA, and 90µA

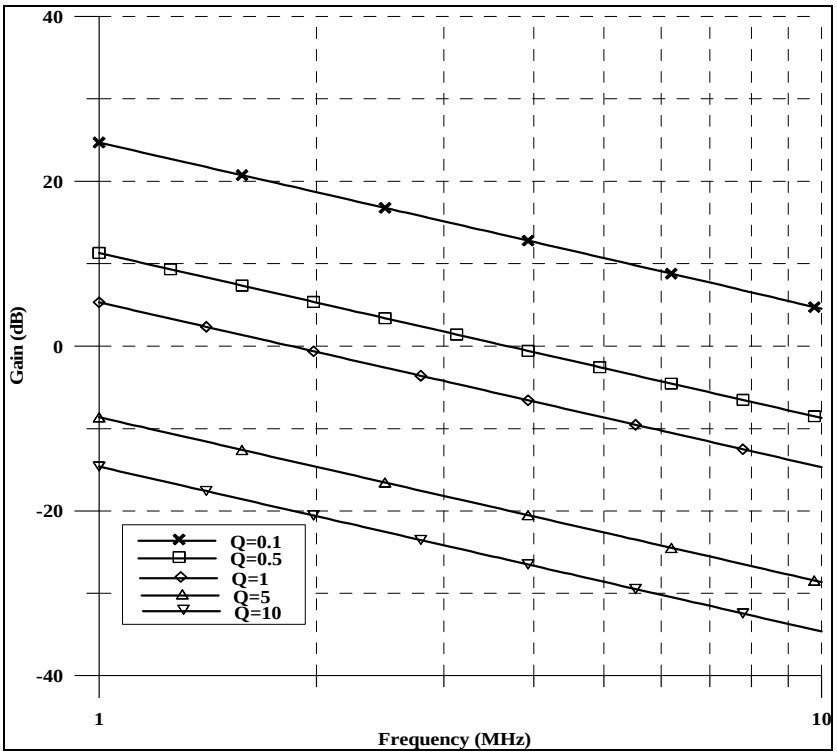

Figure 3. 7 The gain response of the proposed lossless integrator for Q is 0.1, 0.5, 1, 5, and 10

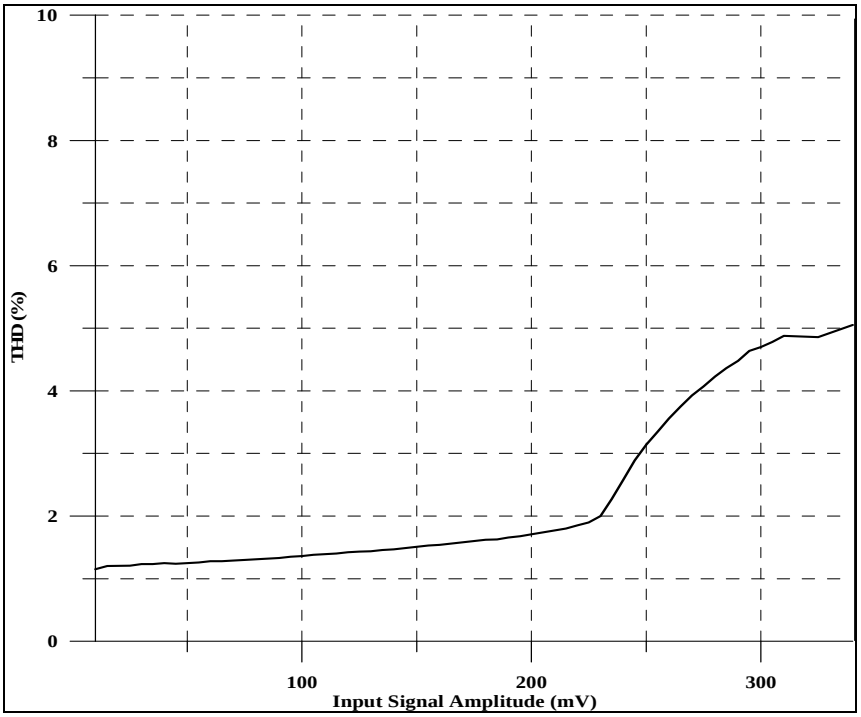

Figure 3. 8 Total harmonic distortion (THD) as a function of input signal amplitude at 1.87 MHz.

3.2 First Order Lowpass Filter

In square root domain, first order lowpass filter was presented by Eskiyerli, Payne, and Toumazou in 1996 with state space synthesis method and by Psychalinos and Vlassis in 2002 with combining geometric mean and multiplier/divider blocks. In this dissertation, a different first order lowpass filter was introduced by using state space synthesis method.

It is known that, a transfer function of any system can be represented by different state space equations and also with different state variables but it does not cause any effect on system behavior. The transfer function of a first order low pass filter is expressed as

$$H(s) = \frac{\omega_0}{s + \omega_0} \tag{3.15}$$

where ω_0 is cut-off frequency. The state space representation obtained by using companion form technique (Eskiyerli and others, 1996) is expressed as

$$\dot{x} = \omega_0 u - \omega_0 x \tag{3.16}$$
$$y = x$$

If the node voltage V_1 and voltage signal U are assumed the state variables x and u, state and output equations in (3.16) are rewritten as

$$C\dot{V}_1 = C\omega_0 U - C\omega_0 V_1 \tag{3.17}$$
$$y = V_1$$

where C is a capacitor value as seemed multiplying factor. By assuming that U and V_1 are gate-source voltages of MOS transistors operating in saturation region with their drain currents are defined as I_u, I_1, respectively. So, $C\dot{V}_1 = I_C$ is current of the capacitor Equation (3.17) is arranged as

$$I_C = C\omega_0\left(\sqrt{\frac{I_u}{\beta}} + V_{TH}\right) - C\omega_0\left(\sqrt{\frac{I_1}{\beta}} + V_{TH}\right) \tag{3.18}$$

where $I_u=\beta(U-V_{TH})^2$ and $I_1=\beta(V_1-V_{TH})^2$. Hence, the state equation in (3.18) is transformed into

$$I_C = \sqrt{I_0 I_u} - \sqrt{I_0 I_1} \tag{3.19}$$

where the bias current $I_0 = (\omega_0{}^2 C^2)/\beta$. The square root domain first order lowpass filter consisting of two geometric mean circuits, current mirror circuits, and a capacitor is shown in Figure 3.9.

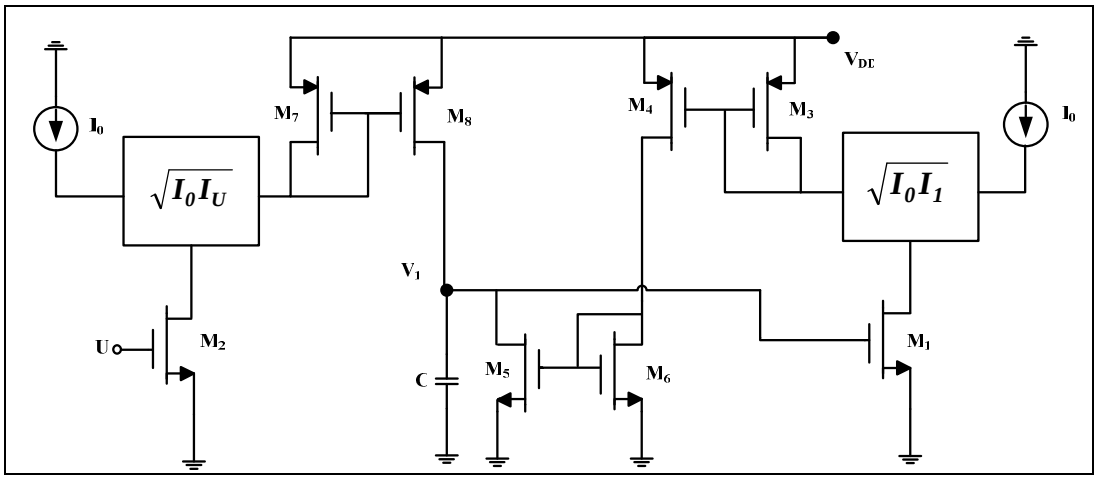

Figure 3. 9 A square root domain first order lowpass filter

It is seen that, D.C. operating conditions must be provided. By assuming that the state variable *x* has D.C. term V_1 and A.C. term v_1 and similarly the input *u* has D.C. term *U* and A.C. term *u*, state equation in Equation (3.17) is rearranged as

$$C(\dot{V}_1 + \dot{v}_1) = C\omega_0(U + u) - C\omega_0(V_1 + v_1) \tag{3.20}$$

When D.C. terms and A.C. terms are separated, the state equation is

$$C.\dot{V}_1 + C\dot{v}_1 = C\omega_0 U + C\omega_0 u - C\omega_0 V_1 - C\omega_0 v_1 \tag{3.21}$$

Since current of a capacitor should be zero in D.C. operating point analysis, the D.C. terms of Equation (3.21) are set to zero. If it is assumed that V_1 is equal to *U*, the D.C. operating conditions are provided and there is no need to add any bias current to the circuit.

By using TSMC 0.25μm CMOS Level 3 model parameters (Appendix), the first order lowpass filter was simulated with values of parameters given in Table 3.2. Under these conditions, theoretical cut-off frequency is 1.66MHz while simulated is 1.69MHz. Gain and phase responses of the first order lowpass filter are indicated in Figure 3.10 with theoretical response.

Similarly to lossless integrator, cut off frequency of all square root domain filters designed with state space synthesis method can be adjustable by changing the bias current I_0. Electronically tunable gain response of the filter for five different bias currents, from 5 µA to 45 µA, is depicted in Figure 3.11 with theoretical response.

Table 3. 2 The parameters of the first order lowpass filter

Parameter values	
V_{DD}	2.5V
U (D.C. voltage)	0.7V
C	1pF
I_0	10µA
Aspect ratio of transistor M_1 and M_2	10µm/10µm
Aspect ratios of transistors M_3-M_7	0.7µm/7µm

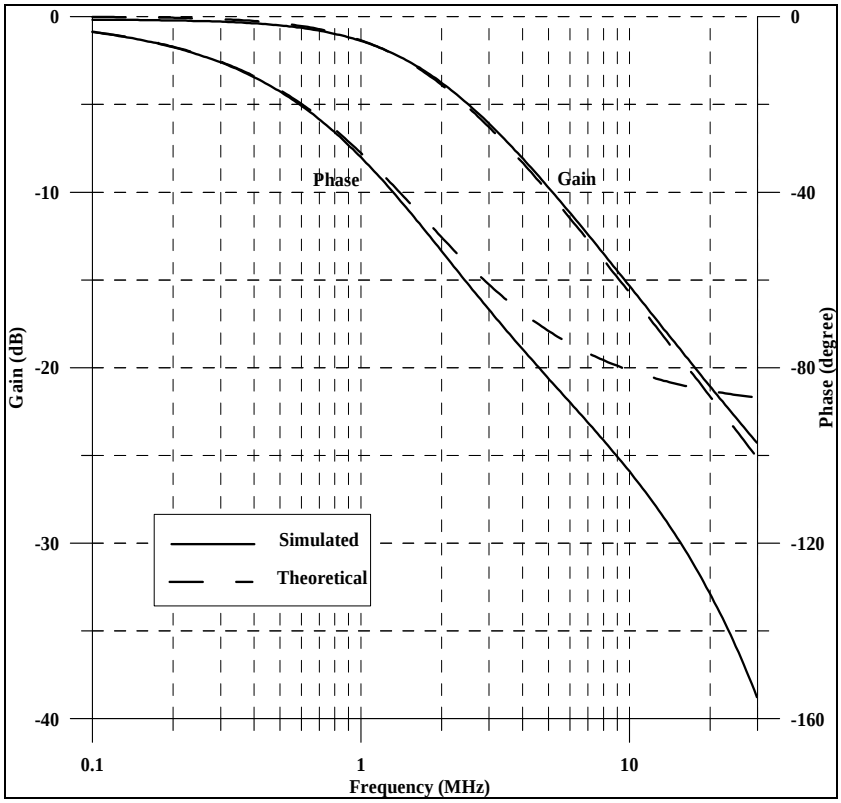

Figure 3. 10 Gain and phase responses of the first order lowpass filter

When input sinusoidal amplitude was 10mV at 1.66MHz, bias current was 10µA the time response of the first order lowpass filter was simulated as given in Figure 3.12. This causes 79.857ns time delay at the output of the filter corresponding to 47° phase difference.

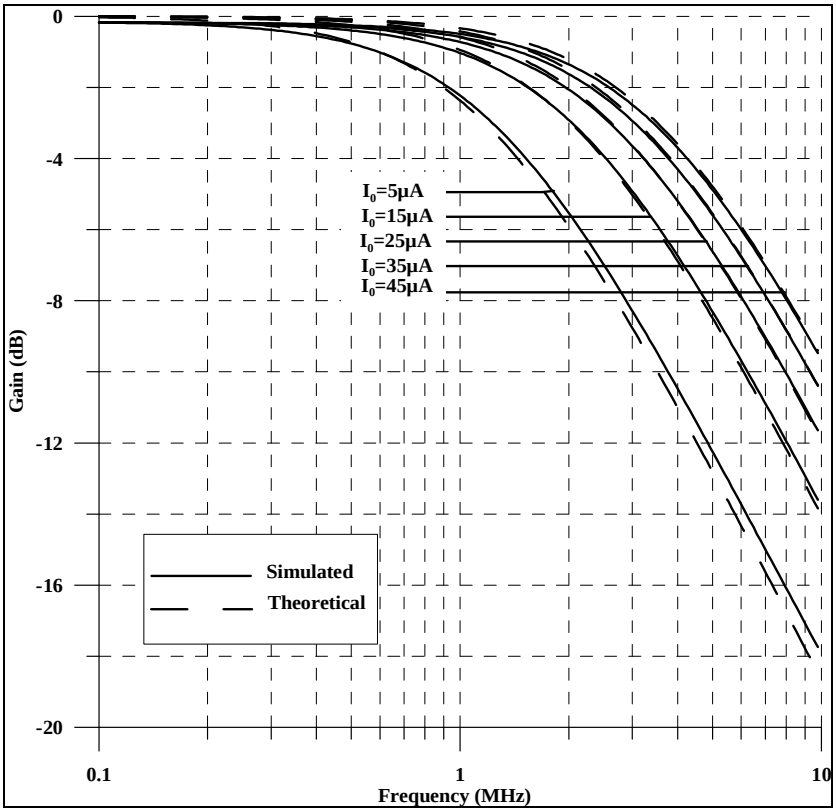

Figure 3. 11 Electronically tunable gain response of the first order lowpass filter for I_0 is 5µA, 15µA, 25µA, 35µA, and 45µA

The dependence of the output harmonic distortion of first order lowpass filter on input signal amplitude was illustrated in Figure 3.13. As shown in this Figure, THD increases with input signal. As such, input signal must be 280 mV or less to avoid output distortion.

The performance of the first order lowpass filter in terms of the sensitivity of MOS transistor parameter mismatch and tolerances of the capacitors has been evaluated by performing Monte Carlo simulations. For performing the Monte Carlo

analysis, *W* and *L* dimensions of the all transistors in the filter have uniform distribution with 5% tolerances and the capacitor in the filter circuit have uniform deviation with 10% tolerances. The gain response of the first order lowpass filter with Monte Carlo analysis for 100 runs is shown in Figure 3.14 when the cut off frequency is 1.66MHz. The cut off frequency was obtained between 1.54MHz and 1.86 MHz during the analysis.

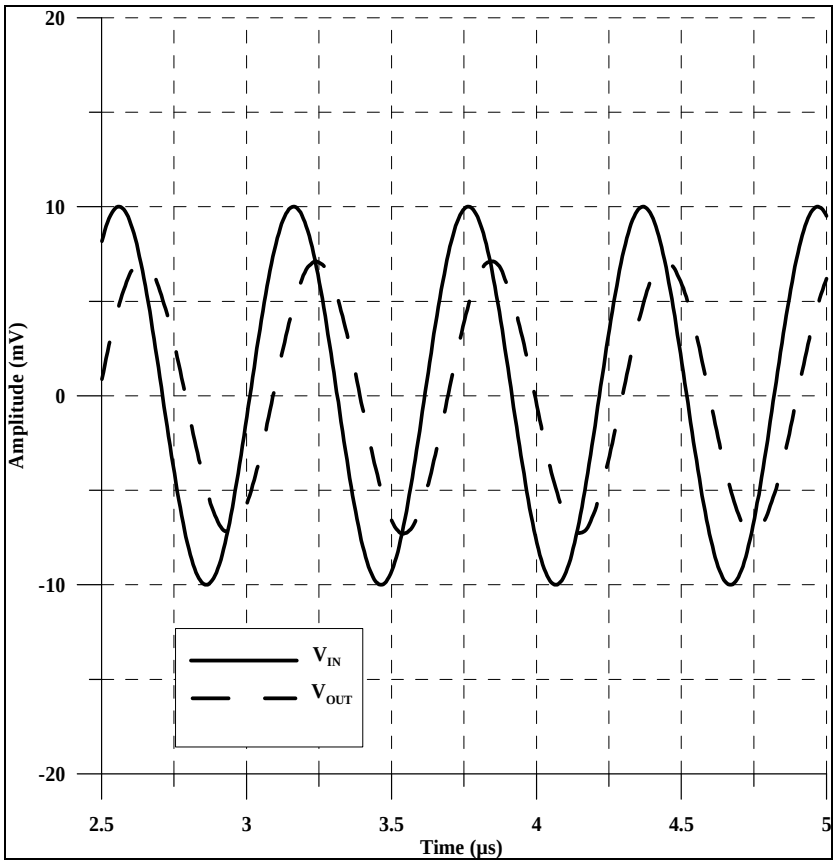

Figure 3. 12 The time response of the first order lowpass filter

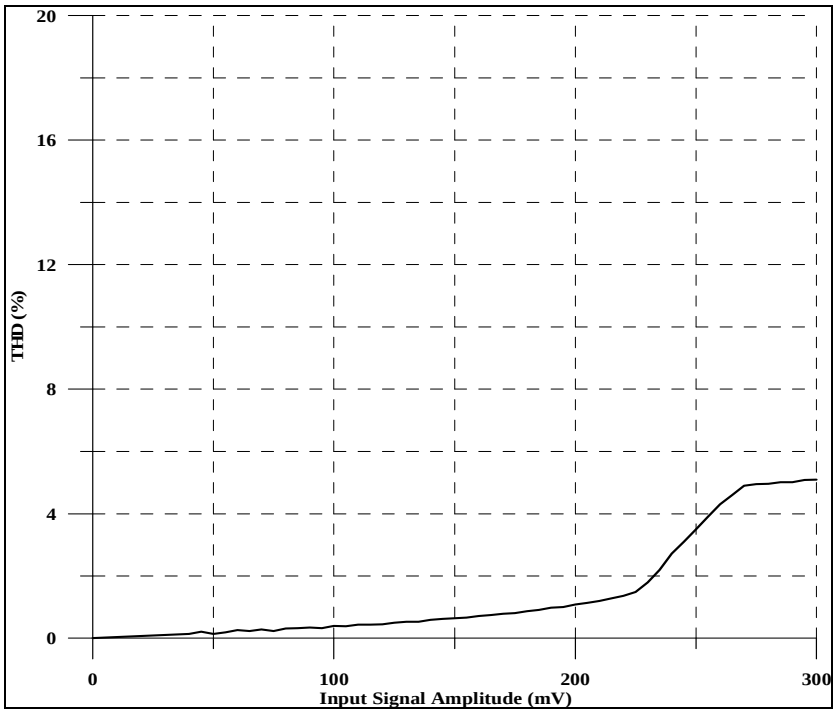

Figure 3. 13 Total harmonic distortion (THD) of first order lowpass filter as a function of input signal amplitude at 1.66 MHz.

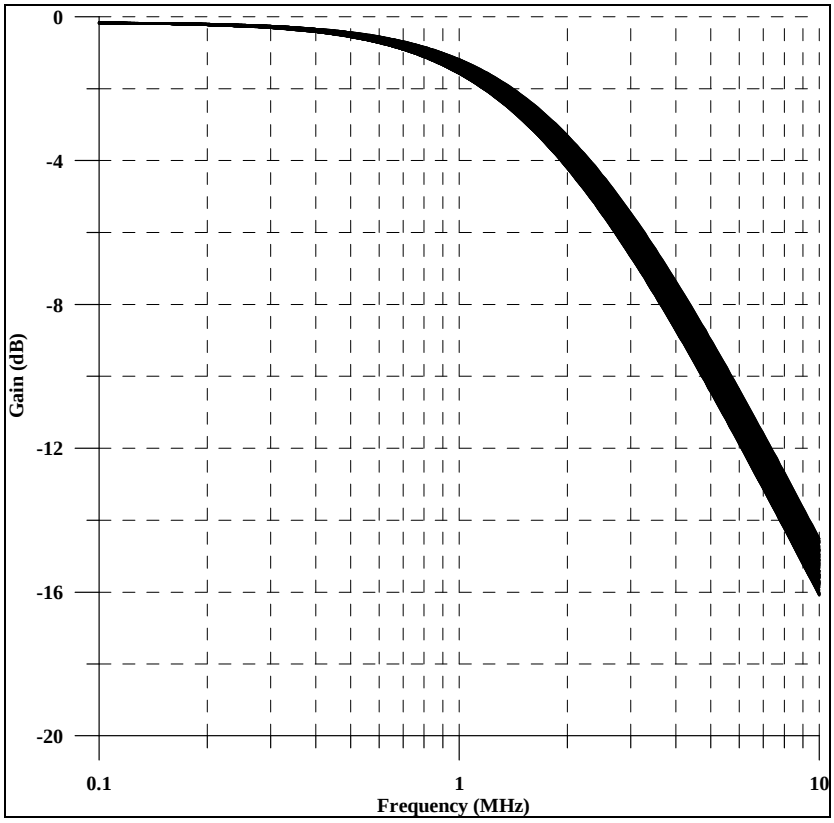

Figure 3. 14 Gain response of the first order lowpass filter with Monte Carlo analysis

3.3 First Order Highpass Filter

It is known that highpass filter is the one of useful basic filter type. In the literature, there are square root domain differentiator circuits that are pure differentiator and not designed by using state space synthesis method (Vlassis and Psychalinos, 2004; Fouad and Soliman, 2005). In this thesis, a square root domain first order highpass filter is presented for the first time in literature.

The transfer function of a first order high pass filter is expressed as

$$H(s) = \frac{s}{s + \omega_0} \tag{3.22}$$

where ω_0 is cut-off frequency. The state space representation obtained by using observable canonical form is expressed as

$$\dot{x} = -\omega_0 x - \omega_0 u \tag{3.23}$$
$$y = x + u$$

To realize the filter, state variable x is multiplied with -1 and the final state equations are obtained;

$$\dot{x} = -\omega_0 x + \omega_0 u \tag{3.24}$$
$$y = -x + u$$

If the node voltage V_1 and voltage signal U are assumed the state variables x and u, state and output equations in (3.24) are rewritten as

$$C\dot{V}_1 = -C\omega_0 V_1 + C\omega_0 U \tag{3.25}$$
$$y = -V_1 + U$$

where C is a capacitor value as seemed multiplying factor. By assuming that U and V_1 are gate-source voltages of MOS transistors operating in saturation region with their drain currents are defined as I_u, I_1, respectively. So, $C\dot{V}_1 = I_C$ is current of the capacitor Equation (3.25) is arranged that

$$I_C = C\omega_0\left(\sqrt{\frac{I_u}{\beta}} + V_{TH}\right) - C\omega_0\left(\sqrt{\frac{I_1}{\beta}} + V_{TH}\right) \tag{3.26}$$

where $I_u=\beta(U-V_{TH})^2$ and $I_1=\beta(V_1-V_{TH})^2$. Hence, the state equation in (3.26) is transformed into

$$I_C = -\sqrt{I_0 I_1} + \sqrt{I_0 I_u} \tag{3.27}$$

where the bias current $I_0 = (\omega_0{}^2 C^2)/\beta$. The square root domain first order highpass filter consisting of two geometric mean circuits, current mirror circuits, a summation block and a capacitor is shown in Figure 3.15.

At the first sight, it can be said that similarly to first order lowpass filter, when D.C. operating point analysis is considered, if it is assumed that V_1 is equal to U, the D.C. operating conditions are provided and there is no need to add any bias current to the circuit. This is valid for state equation but not for output equation. So, if it is assumed that $U/2$ is equal to V_1; Equation (3.25) is rearranged

$$C\dot{V}_1 = -C\omega_0 \frac{U}{2} + C\omega_0 U \tag{3.28}$$

To equate the D.C. terms of Equation (3.28) to zero a D.C. current is added

$$C.\dot{V}_1 = -C\omega_0 \frac{U}{2} + C\omega_0 U + I_{DC} = 0 \tag{3.29}$$

where $I_{DC}=-C\omega_0 U/2$. By substituting the D.C. current source in Equation (3.27)

$$I_C = -\sqrt{I_0 I_1} + \sqrt{I_0 I_u} + I_{DC} \tag{3.30}$$

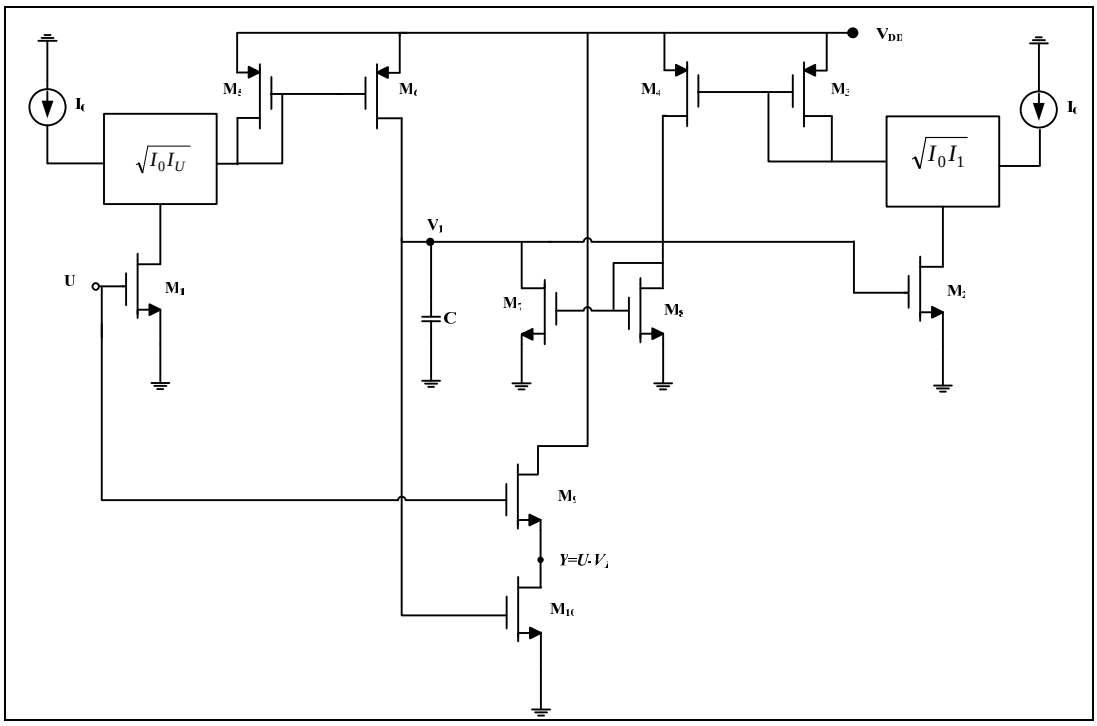

Figure 3. 15 Square root domain first order highpass filter

According to adjustments, the modified square root domain first order highpass filter circuit is indicated in Figure 3.16.

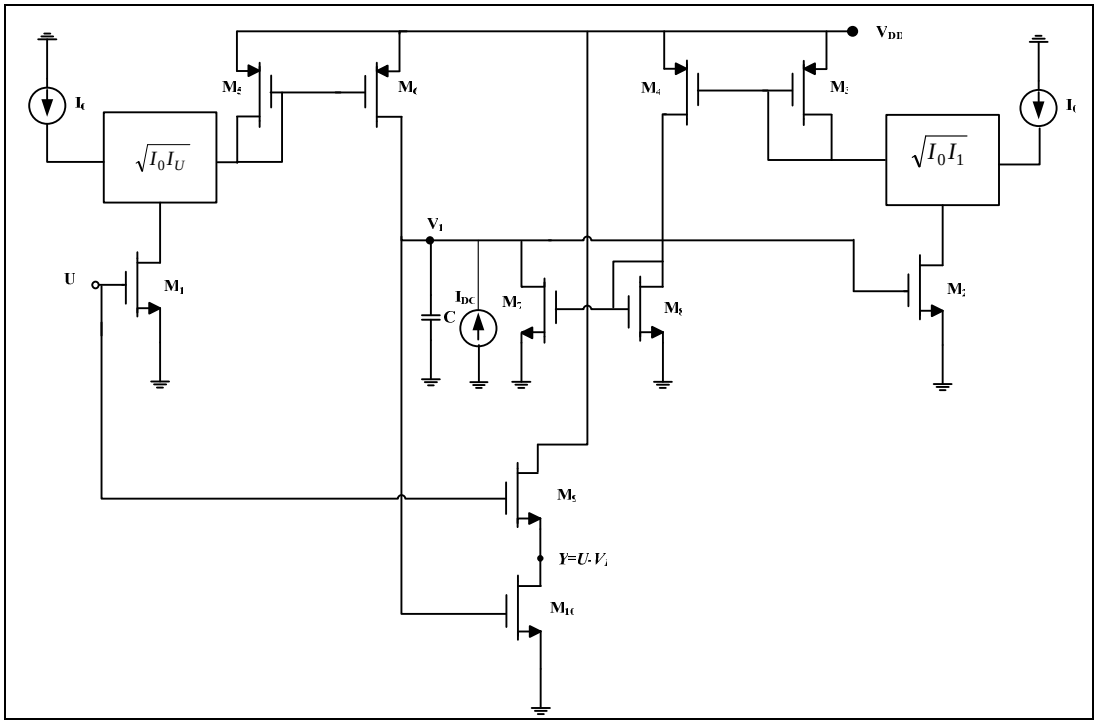

Figure 3. 16 Modified square root domain first order highpass filter

By using TSMC 0.25µm CMOS Level 3 model parameters (Appendix), the presented first order highpass filter was simulated with values of parameters given in Table 3.3. Under these conditions, theoretical cut-off frequency is 1.65MHz while simulated is 1.7MHz. Gain and phase responses of the first order highpass filter are indicated in Figure 3.17 with theoretical response.

Table 3. 3 The parameters of the first order highpass filter

Parameter values	
V_{DD}	2.5V
U (D.C. voltage)	1.4V
C	3pF
I_0	10µA
I_{DC}	21.83µA
Aspect ratio of transistor M_1 and M_2	7µm/7µm
Aspect ratios of transistors M_3-M_{10}	0.7µm/7µm

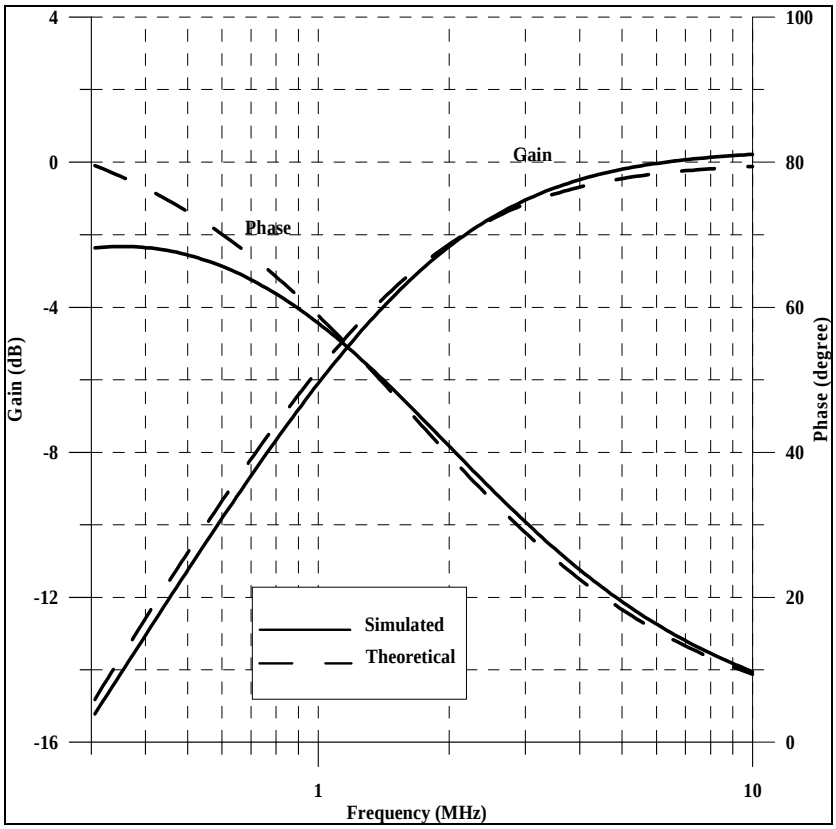

Figure 3. 17 Gain and phase responses of the first order highpass filter

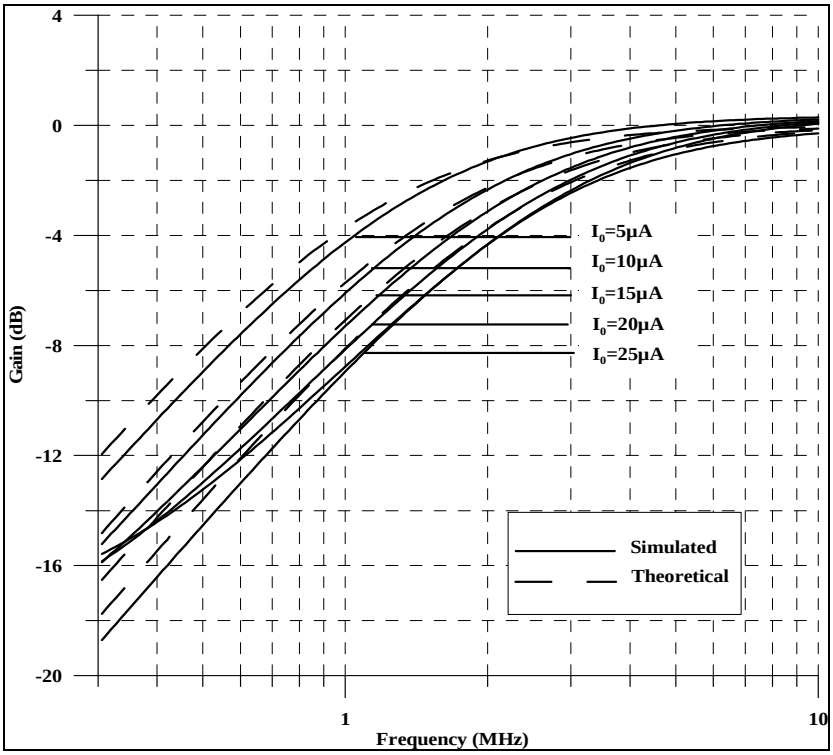

Figure 3. 18 Electronically tunable gain response of the first order highpass filter for I_0 is 5µA, 10µA, 15µA, 20µA, and 25µA

Electronically tunable gain response of the filter for five different bias currents, from 5µA to 25µA, is depicted in Figure 3.18 with theoretical response. When input sinusoidal amplitude was 10mV at 2.02MHz, bias current was 15µA the time response of presented first order highpass filter was simulated as given in Figure 3.19. This causes 59.4ns time delay at the output of the filter corresponding to -43.2° phase difference.

The dependence of the output harmonic distortion of presented first order highpass filter on input signal amplitude was illustrated in Figure 3.20. As shown in this Figure, THD increases with input signal. As such, input signal must be 470 mV or less to avoid output distortion.

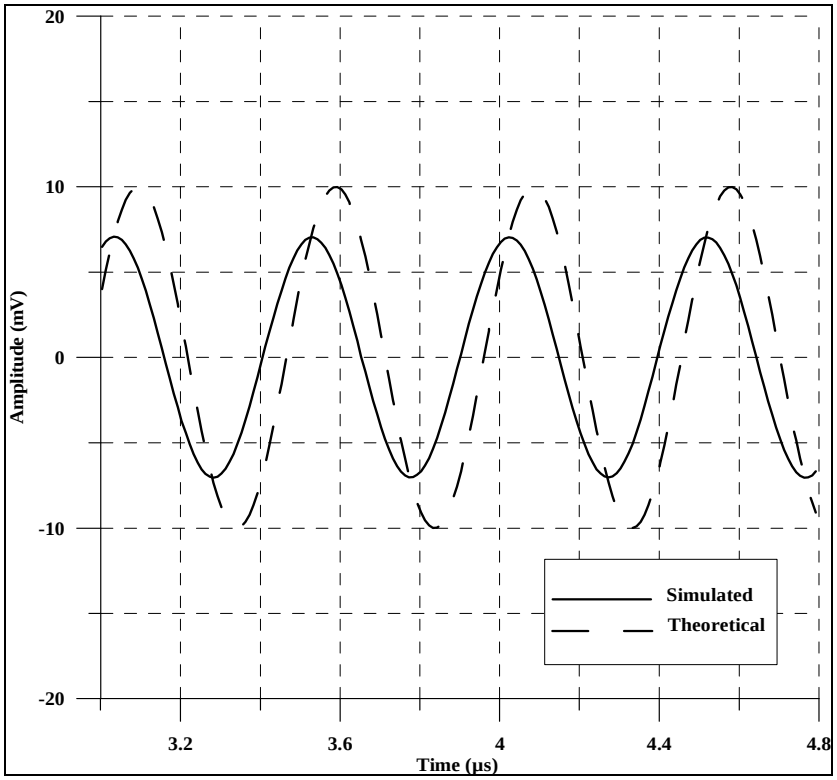

Figure 3. 19 The time response of the first order highpass filter

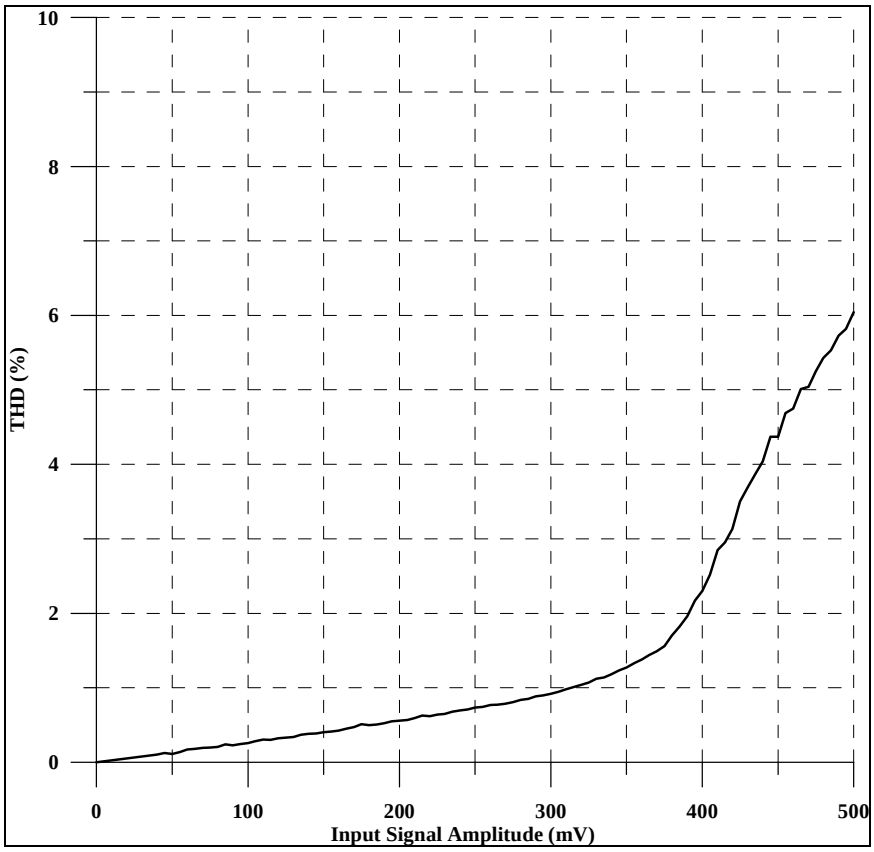

Figure 3. 20 Total harmonic distortion (THD) of presented first order highpass filter as a function of input signal amplitude at 2.02MHz.

The performance of the first order highpass filter in terms of the sensitivity of MOS transistor parameter mismatch and tolerances of the capacitors has been evaluated by performing Monte Carlo simulations. For performing the Monte Carlo analysis, *W* and *L* dimensions of the all transistors in the filter have uniform distribution with 5% tolerances and the capacitor in the filter circuit have uniform deviation with 10% tolerances. The gain response of the first order highpass filter with Monte Carlo analysis for 100 runs is shown in Figure 3.21 when the cut off frequency is 2.02MHz. The cut off frequency was obtained between 1.88MHz and 2.25MHz during the analysis.

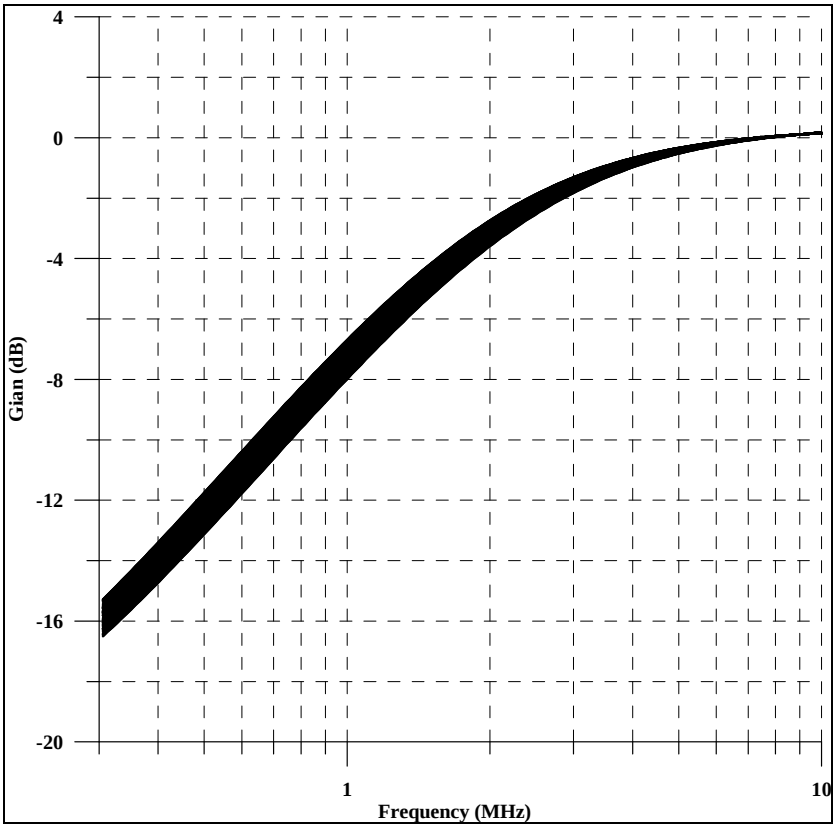

Figure 3. 21 Gain response of the first order highpass filter with Monte Carlo analysis

3.4 First Order Allpass Filter

One of the most important building blocks in analog signal processing applications is the allpass filter. Allpass filters also called phase shifters generate frequency-dependent delay while holding the amplitude of the input signal over the desired frequency range (Schaumann & Valkenburg, 2001). There are two square root domain first order allpass filters presented in the literature. One of them is designed by using N-cell and P-cell (Ozoğuz, Abdelrahman, & Elwakil, 2006) and the other is designed by using state space synthesis method (Ölmez and Çam, 2010a).

A first-order allpass filter transfer function can be written as follows,

$$H(s) = a\frac{s-\omega_0}{s+\omega_0} \tag{3.31}$$

where ω_0 is the center frequency and *a* is gain of the filter. When *a* is chosen as -1, the transfer function of the first order allpass filter is expressed as

$$H(s) = -\frac{s-\omega_0}{s+\omega_0} \tag{3.32}$$

By using observable canonical form, transfer function in Equation (3.32) is transformed to the following equations:

$$\dot{x} = -\omega_0 x + 2\omega_0 u \tag{3.33}$$
$$y = x - u$$

If the node voltage V_1 and voltage signal *U* are assumed the state variables *x* and *u*, state and output equations in (3.33) are rewritten as

$$C\dot{V}_1 = -C\omega_0 V_1 + 2C\omega_0 U \tag{3.34}$$
$$y = V_1 - U$$

where *C* is a capacitor value as seemed multiplying factor. By assuming that *U* and V_1 are gate-source voltages of MOS transistors operating in saturation region with their drain currents are defined as I_u, I_1, respectively. So, $C\dot{V}_1 = I_C$ is current of the capacitor Equation (3.34) is arranged that

$$I_C = -C\omega_0\left(\sqrt{\frac{I_1}{\beta}} + V_{TH}\right) + 2C\omega_0\left(\sqrt{\frac{I_u}{\beta}} + V_{TH}\right) \tag{3.35}$$

where $I_u=\beta(U-V_{TH})^2$ and $I_1=\beta(V_1-V_{TH})^2$. Hence, the state equation in (3.35) is transformed into

$$I_C = -\sqrt{I_0 I_1} + 2\sqrt{I_0 I_u} + I_{TH} \tag{3.36}$$

where $I_C = C\dot{V}_1, I_0 = (\omega_0{}^2 C^2)/\beta$, and $I_{TH} = \omega_0 C V_{TH}$. When D.C. operating point analysis is considered, if it is assumed that V_1 is equal to $2U$, the output equation of the filter can be realized. Under this condition state equation in Equation (3.34) is rearranged as

$$C\dot{V}_1 = -C\omega_0 2U + 2C\omega_0 U \tag{3.37}$$

To equate the D.C. terms of Equation (3.37) to zero there is no need to add any D.C. current. So, the state equation in (3.36) is appropriate to realize the filter.

According to this configuration, the negative gain first order allpass filter is indicated in Figure 3.22.

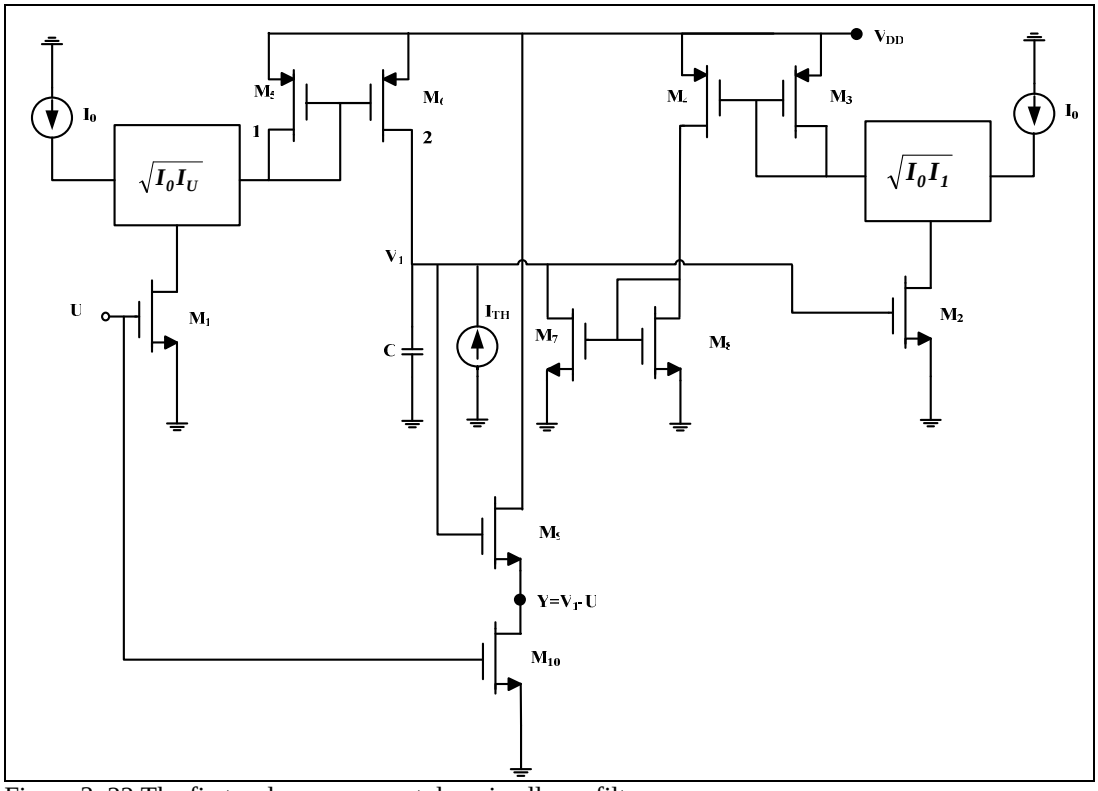

Figure 3. 22 The first order square-root domain allpass filter

To realize the negative gain first order allpass filter, there is a one way more that; if I_u is defined as $4\beta(U-V_{TH})^2$, the state equation is rearranged as

$$I_C = -\sqrt{I_0 I_1} + \sqrt{I_0 I_u} + I_{TH} \tag{3.38}$$

where $I_C = C\dot{V}_1, I_0 = (\omega_0{}^2 C^2)/\beta$, and $I_{TH} = \omega_0 C V_{TH}$.

By using TSMC 0.25μm CMOS Level 3 model parameters (Appendix), the first order allpass filter was simulated with values of parameters given in Table 3.4. Under these conditions, theoretical cut-off frequency is 3.21MHz while simulated is 3.18MHz. Gain and phase responses of the first order allpass filter are indicated in Figure 3.23 with theoretical response.

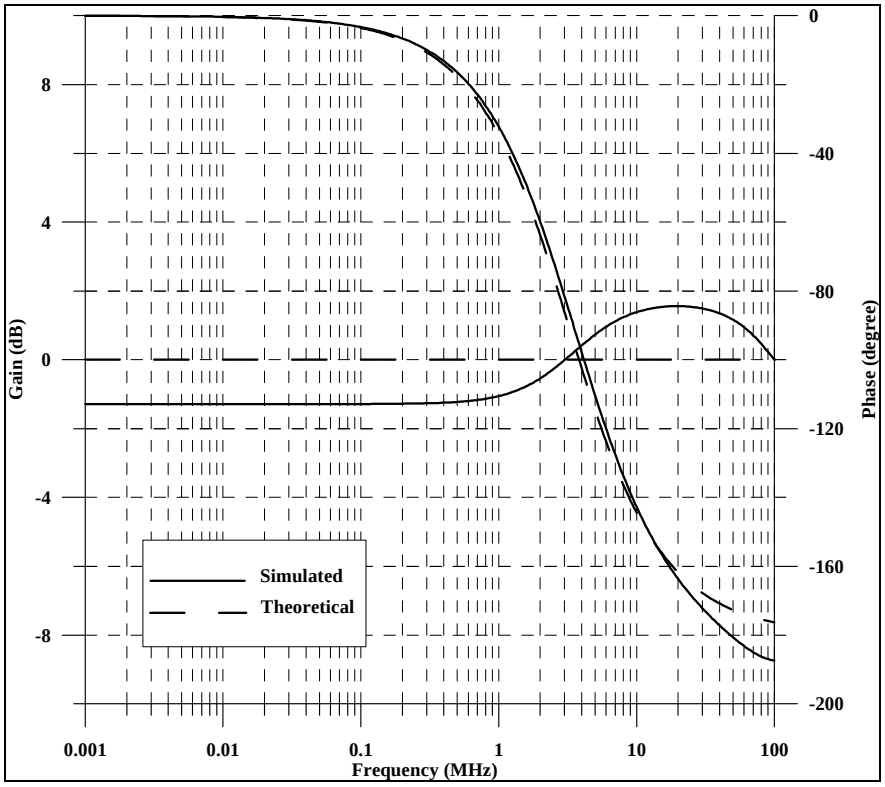

Figure 3. 23 Gain and phase response of the first-order allpass filter

Table 3. 4 The parameters of the first order allpass filter

Parameter values	
V_{DD}	2.5V
U (D.C. voltage)	0.85V
C	1.5pF
I_0	10μA
I_{TH}	12.06 μA
Aspect ratio of transistor M_1 and M_2	7μm/7μm
Aspect ratios of transistors M_3-M_5 and M_7-M_{10}	0.7μm/7μm
Aspect ratios of transistor M_6	0.7μm /14μm

Similarly to other filter circuits, the cut off frequency of allpass filter can be adjustable by chancing the bias current I_0. Electronically tunable gain response of

the filter for five different bias currents, from 5 µA to 25 µA, is depicted in Figure 3.24.

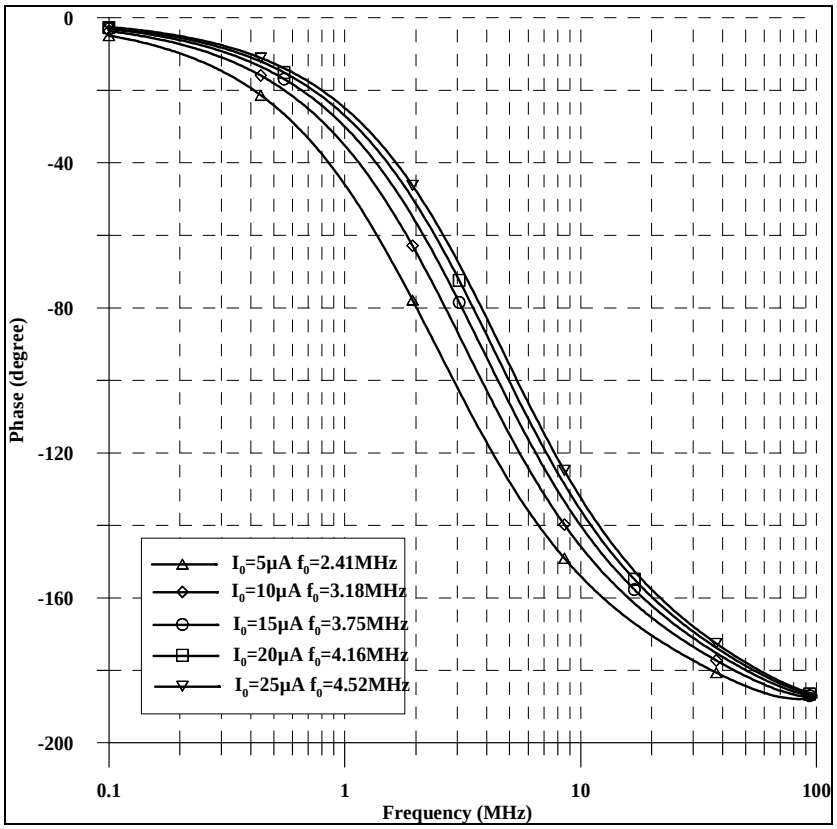

Figure 3. 24 Electronically tunable phase response of the first order allpass filter

Figure 3.25 shows the time domain response of the filter when bias current is 10µA and input voltage with 10mV amplitude at 3.21MHz frequency. This causes 78.07ns time delay at the output of the filter corresponding to 91.94° phase difference which is close to the theoretical value (90°). The dependence of the output harmonic distortion of presented filter on input signal amplitude is illustrated in Figure 3.26. Due to this Figure THD increases when the input signal is increased. To avoid the distortions at the output signal, maximum amplitude value of the input signal must be 200mV.

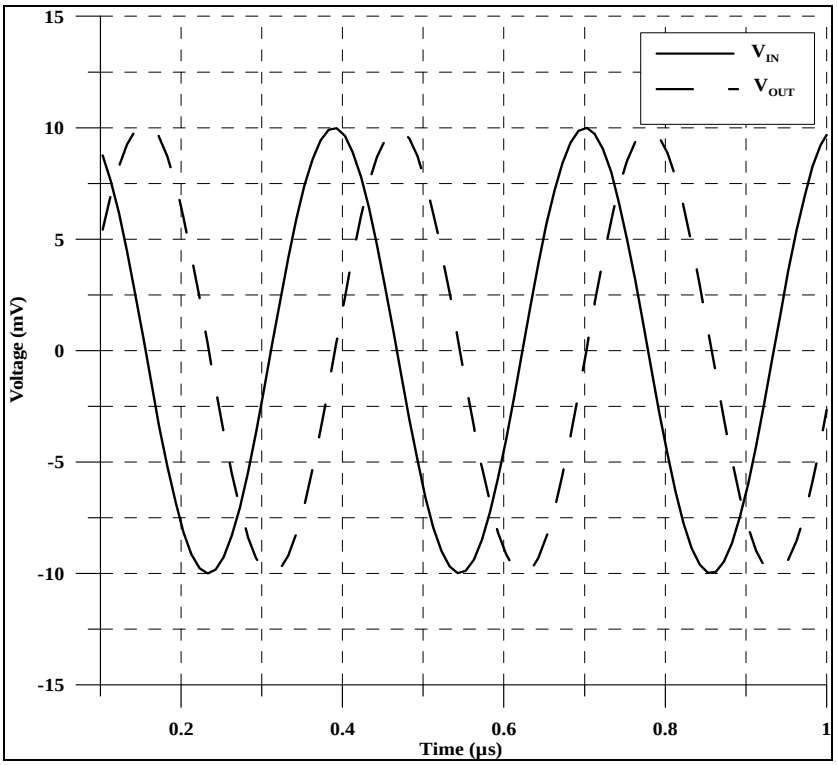

Figure 3. 25 Time domain response of the presented negative gain first order all pass filter

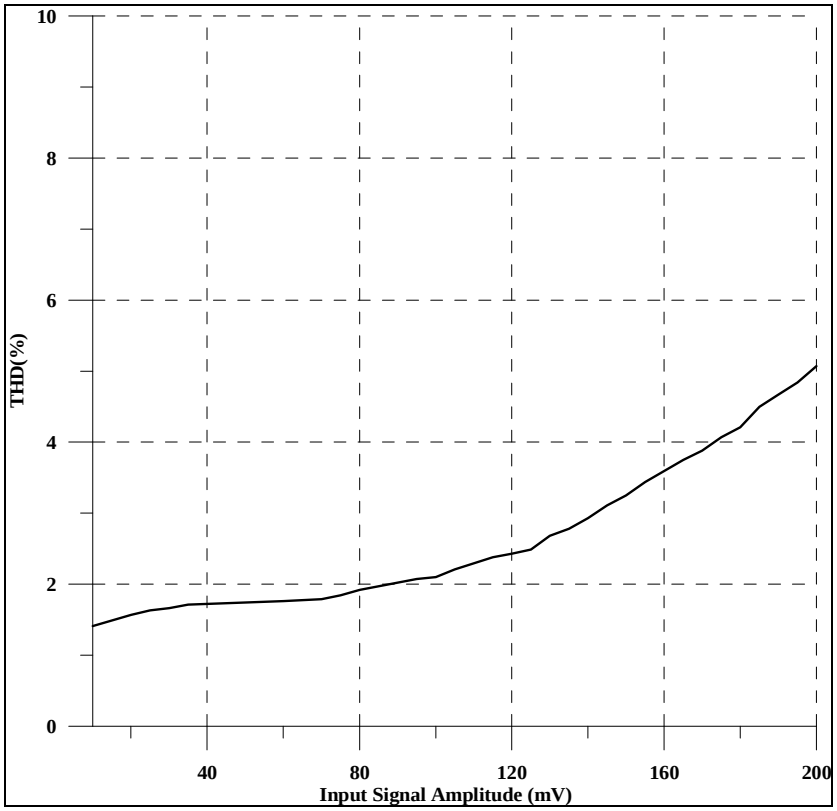

Figure 3. 26 THD versus input signal amplitude at 3.21MHz of allpass filter

CHAPTER FOUR
SQUARE ROOT DOMAIN SECOND ORDER CIRCUITS

In this chapter, second order highpass, second order notch filter with regular, lowpass and highpass notch cases, second order allpass filter, KHN biquad filter, and Tow-Thomas biquad filter are proposed as novel square root domain filters to the literature. Second order lowpass and second order bandpass filters are also simulated in this chapter as having alternative structures from the papers in the literature. To obtain operating conditions of filters, different analysis are done.

4.1 Second Order Lowpass Filter

In the literature, there are square root domain second order lowpass filters (Gwo-Jeng Yu, 2005; Menekay, Tarcan, & Kuntman, 2006;) designed by using state space synthesis method. It is proven that any system having transfer function can be represented by different state and output equations. Although one form of state equations is seen in the literature, in this dissertation, to make easier to realize the filter circuit some modifications were done. The transfer function of second order low pass filter is expressed as

$$H(s) = \frac{\omega_0^2}{s^2 + \frac{\omega_0}{Q}s + \omega_0^2} \tag{4.1}$$

where ω_0, Q are cut-off frequency and quality factor, respectively. The state space representation obtained by using observable canonical form is expressed as

$$\dot{x}_1 = -\omega_0^2 x_2 + \omega_0^2 u \tag{4.2}$$

$$\dot{x}_2 = x_1 - \frac{\omega_0}{Q} x_2$$

$$y = x_2$$

To realize the filter, state variable x is multiplied with ω_0/Q and the final state equations are obtained;

$$\dot{x}_1 = -Q\omega_0 x_2 + Q\omega_0 u \tag{4.3}$$

$$\dot{x}_2 = \frac{\omega_0}{Q} x_1 - \frac{\omega_0}{Q} x_2$$

$$y = x_2$$

If the node voltage V_1, V_2 and voltage signal U are assumed the state variables x_1, x_2, and input u, state and output equations in (3.24) are rewritten as

$$C\dot{V}_1 = -QC\omega_0 V_2 + QC\omega_0 U \tag{4.4}$$

$$C\dot{V}_2 = \frac{C\omega_0}{Q} V_1 - \frac{C\omega_0}{Q} V_2$$

$$y = V_2$$

where C is a capacitor value seemed as multiplying factor. $C\dot{V}_1$ and $C\dot{V}_2$ are accepted a current flows through a grounded capacitor C whose voltage across its terminals in order given V_1 and V_2 and by assuming that U, V_2, and V_1 are gate-source voltages of MOS transistors operating in saturation region with their drain currents are defined as I_u, I_2, and I_1, respectively. So capacitor current equations in (4.4) are arranged as

$$I_{C1} = -QC\omega_0 \left(\sqrt{\frac{I_2}{\beta}} + V_{TH}\right) + QC\omega_0 \left(\sqrt{\frac{I_u}{\beta}} + V_{TH}\right) \tag{4.5}$$

$$I_{C2} = \frac{C\omega_0}{Q} \left(\sqrt{\frac{I_1}{\beta}} + V_{TH}\right) - \frac{C\omega_0}{Q} \left(\sqrt{\frac{I_2}{\beta}} + V_{TH}\right)$$

where $I_1=\beta(V_1-V_{TH})^2$, $I_2=\beta(V_2-V_{TH})^2$, $I_u=\beta(U-V_{TH})^2$, $I_{C1} = C\dot{V}_1$, and $I_{C2} = C\dot{V}_2$. Hence, the state equations in (4.5) are transformed into

$$I_{C1} = -Q\sqrt{I_0 I_2} + Q\sqrt{I_0 I_u} \tag{4.6}$$

$$I_{C2} = \frac{1}{Q}\sqrt{I_0 I_2} - \frac{1}{Q}\sqrt{I_0 I_2}$$

where the bias current $I_0 = (\omega_0{}^2 C^2)/\beta$. The square root domain second order lowpass filter consisting of three geometric mean circuits, current mirror circuits, and two capacitors is shown in Figure 4.1.

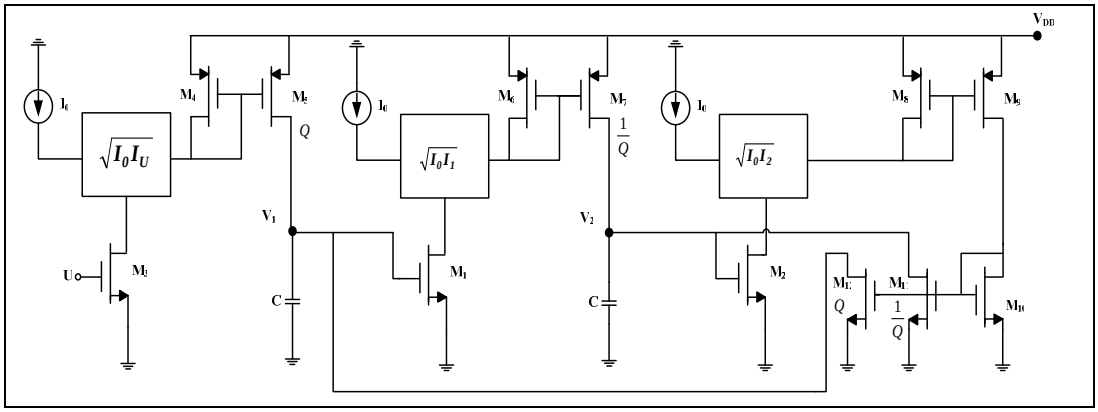

Figure 4. 1 Square root domain second order lowpass filter

It is shown that, D.C. operating point must be considered to realize square root domain circuits. Similarly to first order circuits in Chapter 3, state equations symbolized of a capacitor's current must be equal to zero. So, if V_1 is assumed to equal to U and also to V_2, D.C. operating point analysis is ensured.

In the other square root domain second order lowpass filter simulations in the literature, there is an additive D.C. current source beside the configuration of the presented. By using TSMC 0.25µm CMOS Level 3 model parameters (Appendix), the second order lowpass filter was simulated with values of parameters given in Table 4.1. Under these conditions, theoretical cut-off frequency is 1MHz while simulated is also 1MHz as seen in Figure 4.2.

Table 4. 1 The parameters of the second order lowpass filter

Parameter values	
V_{DD}	2.5V
U (D.C. voltage)	0.7 V
Q	1
C	5pF
I_0	10µA
Aspect ratio of transistors M_1-M_3	10µm/10µm
Aspect ratios of transistors M_4-M_{12}	0.7µm/7µm

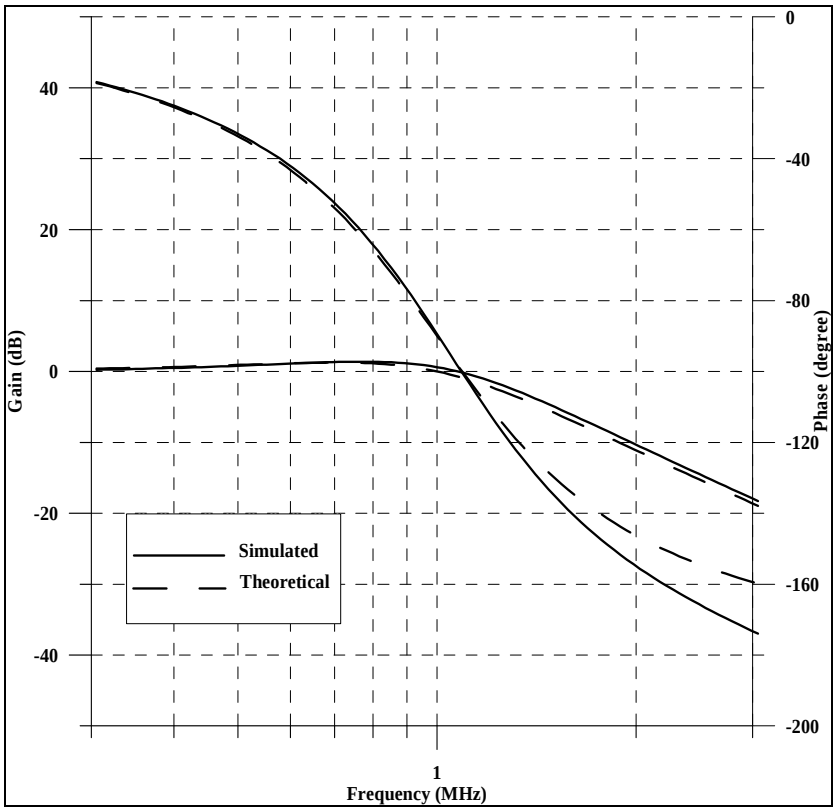

Figure 4. 2 Gain and phase responses of the second order lowpass filter

It can be noticed that the cut off frequency can be tuneable by chancing the bias current I_0. Electronically tunable gain response of the filter for four different bias currents, from 10 µA to 40 µA, is depicted in Figure 4.3 with theoretical response.

The quality factor can be adjusted by changing W/L ratio of M_5, M_7, M_{11}, and M_{12} transistors. Figure 4.4 shows the gain response of the second order lowpass filter, while quality factor is 0.1, 0.5, 1, 2, and 5.

To examine the time response of the filter, a sinusoidal signal was applied to input when its amplitude was 10mV at 1MHz. Figure 4.5 indicates the time response of the second order lowpass filter when bias current is 10µA. This causes 246ns time delay at the output of the filter corresponding to -89° phase difference. The dependence of the output harmonic distortion of filter on input signal amplitude was illustrated in Figure 4.6. As shown in this figure, THD increases with input signal. As such, input signal must be 220 mV or less to avoid output distortion.

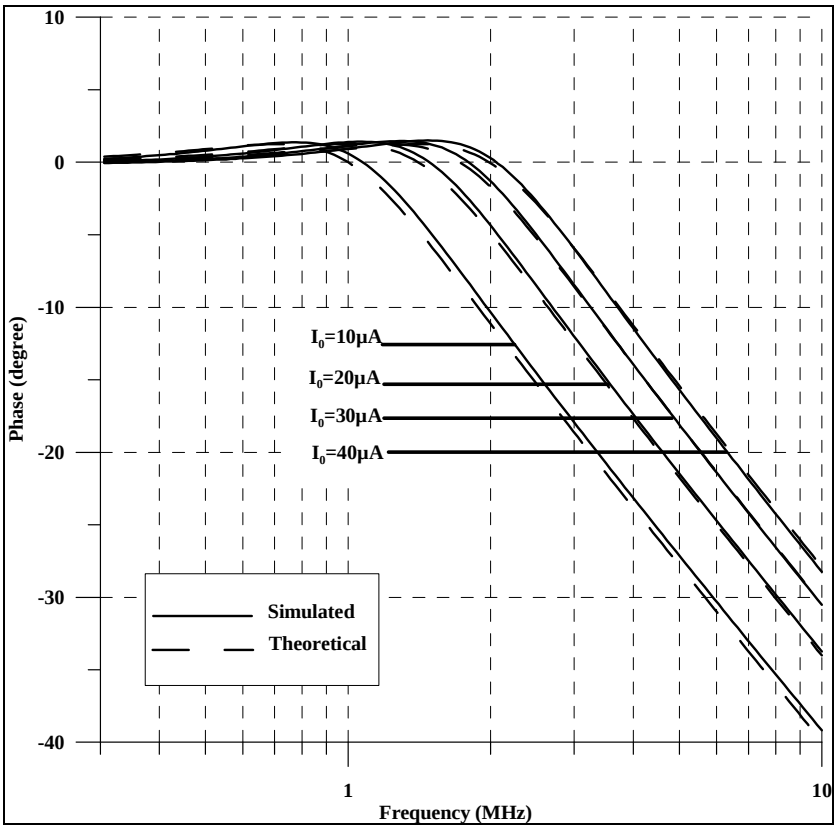

Figure 4. 3 Electronically tunable gain response of the second order lowpass filter for I_0 is 10µA, 20µA, 30µA, and 40µA

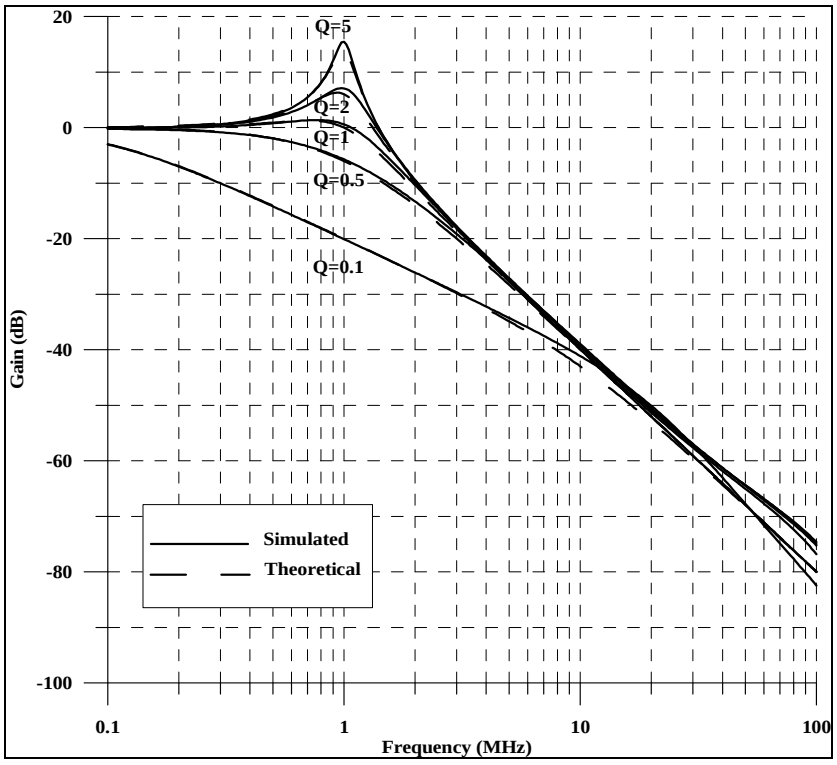

Figure 4. 4 The gain response of the second order lowpass filter for Q is 0.1, 0.5, 1, 2, and 5

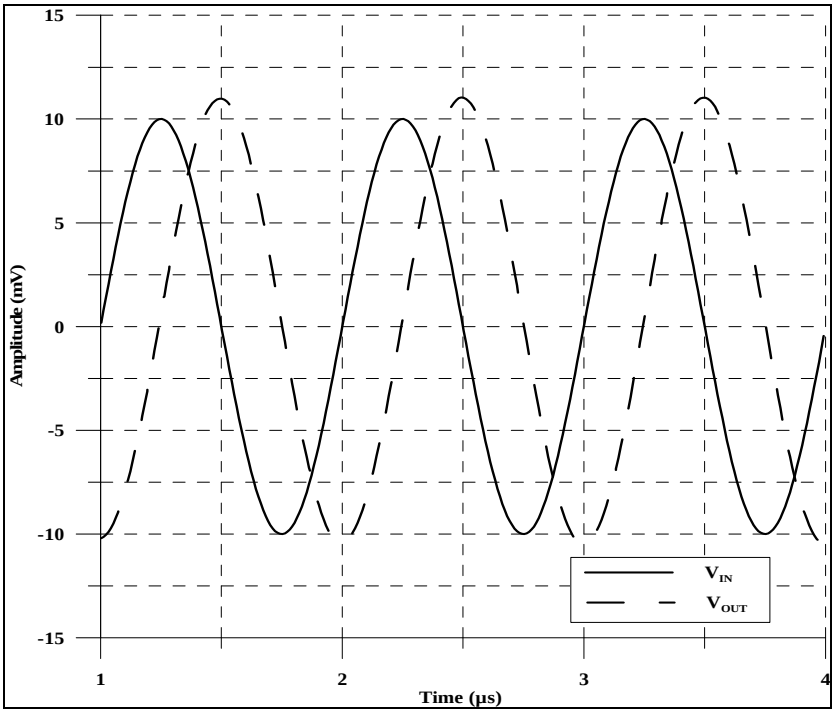

Figure 4. 5 The time response of the second order lowpass filter

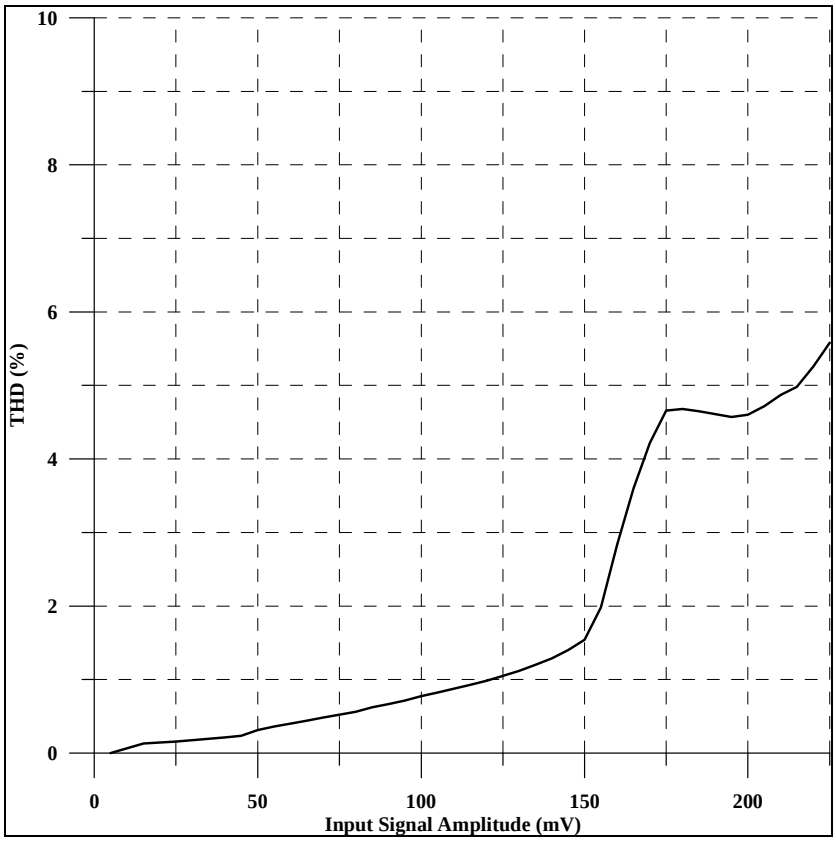

Figure 4. 6 Total harmonic distortion (THD) as a function of input signal amplitude at 1MHz

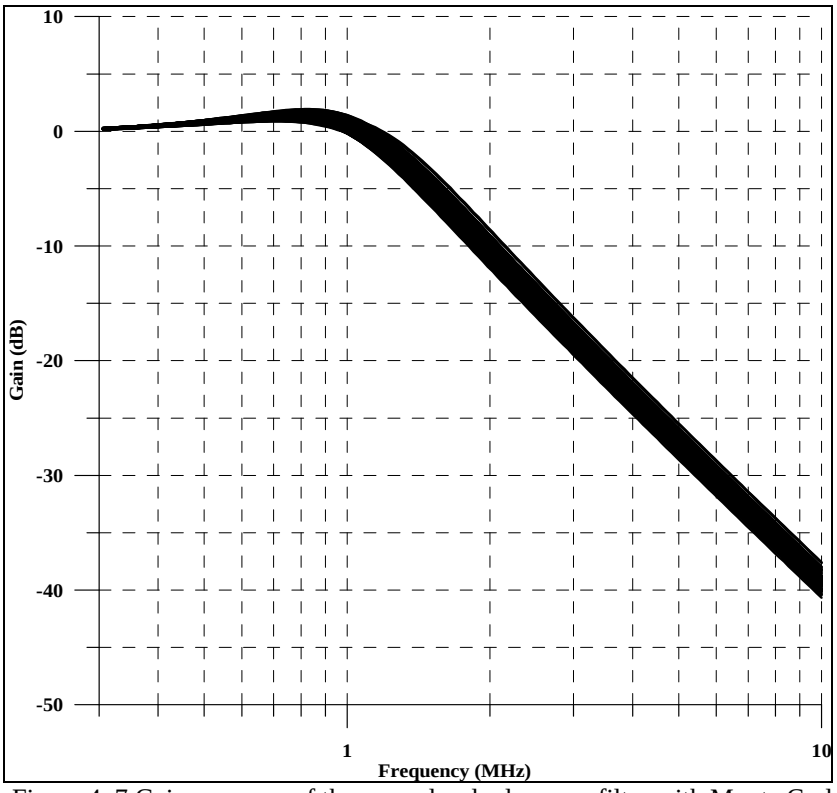

Figure 4. 7 Gain response of the second order lowpass filter with Monte Carlo analysis

The performance of the second order lowpass filter in terms of the sensitivity of MOS transistor parameter mismatch and tolerances of the capacitors has been evaluated by performing Monte Carlo simulations. For performing the Monte Carlo analysis, *W* and *L* dimensions of the all transistors in the filter have uniform distribution with 5% tolerances and the capacitor in the filter circuit have uniform deviation with 10% tolerances. The gain response of the second order lowpass filter with Monte Carlo analysis for 100 runs is shown in Figure 4.7 under the conditions in Table 4.1. The cut off frequency was obtained between 963KHz and 1.19MHz during the analysis.

4.2 Second Order Highpass Filter

The square root domain second order highpass filter is designed by mapping on the state variables of the state space description of its transfer function declared as;

$$H(s) = \frac{s^2}{s^2 + \frac{\omega_0}{Q}s + \omega_0^2} \tag{4.7}$$

where ω_0, Q are cut-off frequency and quality factor, respectively. The state space representation obtained by using companion form technique is expressed as

$$\dot{x}_1 = x_2 - \frac{\omega_0}{Q}u \tag{4.8}$$

$$\dot{x}_2 = -\omega_0^2 x_1 - \frac{\omega_0}{Q}x_2 + u\left(\frac{\omega_0^2}{Q^2} - \omega_0^2\right)$$

$$y = x_1 + u$$

To realize the filter, state variable x_1 and x_2 are multiplied with -1 and ω_0/Q, respectively. So the final state equations are obtained;

$$\dot{x}_1 = -\frac{\omega_0}{Q}x_2 + \frac{\omega_0}{Q}u \tag{4.9}$$

$$\dot{x}_2 = Q\omega_0 x_1 - \frac{\omega_0}{Q}x_2 + u\left(\frac{\omega_0}{Q} - Q\omega_0\right)$$

$$y = -x_1 + u$$

If the node voltage V_1 , V_2 and voltage signal U are assumed the state variables x_1, x_2, and u, state and output equations in (4.9) are rewritten as

$$C\dot{V}_1 = -C\frac{\omega_0}{Q}V_2 + C\frac{\omega_0}{Q}U \tag{4.10}$$

$$C\dot{V}_2 = QC\omega_0 V_1 - \frac{C\omega_0}{Q}V_2 + U\left(\frac{C\omega_0}{Q} - QC\omega_0\right)$$

$$y = -V_1 + U$$

where C is a capacitor value seemed as multiplying factor. $C\dot{V}_1$ and $C\dot{V}_2$ are accepted a current flows through a grounded capacitor C whose voltage across its terminals in order given V_1 and V_2 and by assuming that U, V_2, and V_1 are gate-source voltages of MOS transistors operating in saturation region with their drain currents are defined as I_u, I_2, and I_1, respectively. So capacitor current equations in (4.10) are arranged that

$$I_{C1} = -\frac{C\omega_0}{Q}\left(\sqrt{\frac{I_2}{\beta}} + V_{TH}\right) + \frac{C\omega_0}{Q}\left(\sqrt{\frac{I_u}{\beta}} + V_{TH}\right) \tag{4.11}$$

$$I_{C2} = QC\omega_0\left(\sqrt{\frac{I_1}{\beta}} + V_{TH}\right) - \frac{C\omega_0}{Q}\left(\sqrt{\frac{I_2}{\beta}} + V_{TH}\right) + \frac{C\omega_0}{Q}\left(\sqrt{\frac{I_u}{\beta}} + V_{TH}\right) - C\omega_0 Q\left(\sqrt{\frac{I_u}{\beta}} + V_{TH}\right)$$

where $I_1=\beta(V_1-V_{TH})^2$, $I_2=\beta(V_2-V_{TH})^2$, $I_u=\beta(U-V_{TH})^2$, $I_{C1} = C\dot{V}_1$, and $I_{C2} = C\dot{V}_2$. Hence, the state equations in (4.11) are transformed into

$$I_{C1} = -\frac{1}{Q}\sqrt{I_0 I_2} + \frac{1}{Q}\sqrt{I_0 I_u} \tag{4.12}$$

$$I_{C2} = Q\sqrt{I_0 I_1} - \frac{1}{Q}\sqrt{I_0 I_2} + \frac{1}{Q}\sqrt{I_0 I_u} - Q\sqrt{I_0 I_u}$$

where the bias current $I_0 = (\omega_0{}^2 C^2)/\beta$. The square root domain second order highpass filter consisting of three geometric mean circuits, current mirror circuits, a summation block, and two capacitors is shown in Figure 4.8.

When D.C. operating point analysis is considered, if it is assumed that V_2 *is* equal to *U*, the D.C. operating condition in the first state equation is provided and there is no need to add any bias current to this equation. To realize the difference circuit, it is supposed that *U*/2 is equal to V_1, second state equation is rearranged as;

$$C\dot{V}_2 = QC\omega_0\frac{U}{2} - \frac{C\omega_0}{Q}U + U\left(\frac{C\omega_0}{Q} - QC\omega_0\right) \tag{4.13}$$

To equate the D.C. terms of Equation (4.13) to zero a D.C. current is added

$$C\dot{V}_2 = QC\omega_0\frac{U}{2} - \frac{C\omega_0}{Q}U + U\left(\frac{C\omega_0}{Q} - QC\omega_0\right) + I_{DC} = 0 \tag{4.14}$$

where $I_{DC}=QC\omega_0(U/2)$. By substituting the D.C. current source in second state equation

$$I_{C2} = Q\sqrt{I_0 I_1} - \frac{1}{Q}\sqrt{I_0 I_2} + \frac{1}{Q}\sqrt{I_0 I_u} - Q\sqrt{I_0 I_u} + I_{DC} \tag{4.15}$$

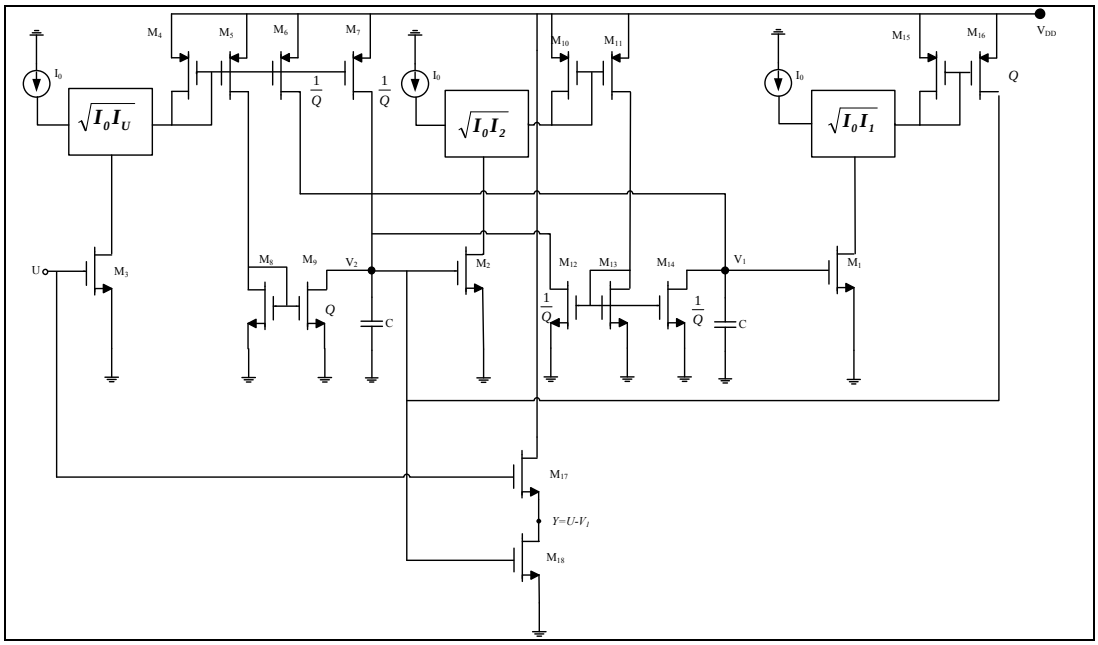

Figure 4. 8 Square root domain second order highpass filter

According to adjustments, the modified square root domain second order highpass filter circuit is indicated in Figure 4.9.

By using TSMC 0.25µm CMOS Level 3 model parameters (Appendix), the presented first order highpass filter was simulated with values of parameters given in Table 4.2. Under these conditions, theoretical cut-off frequency is 1 MHz while simulated is 1MHz. Gain and phase responses of the second order highpass filter are indicated in Figure 4.10 with theoretical response.

Electronically tunable gain response of the filter for four different bias currents, from 10µA to 40µA, is depicted in Figure 4.11 with theoretical response.

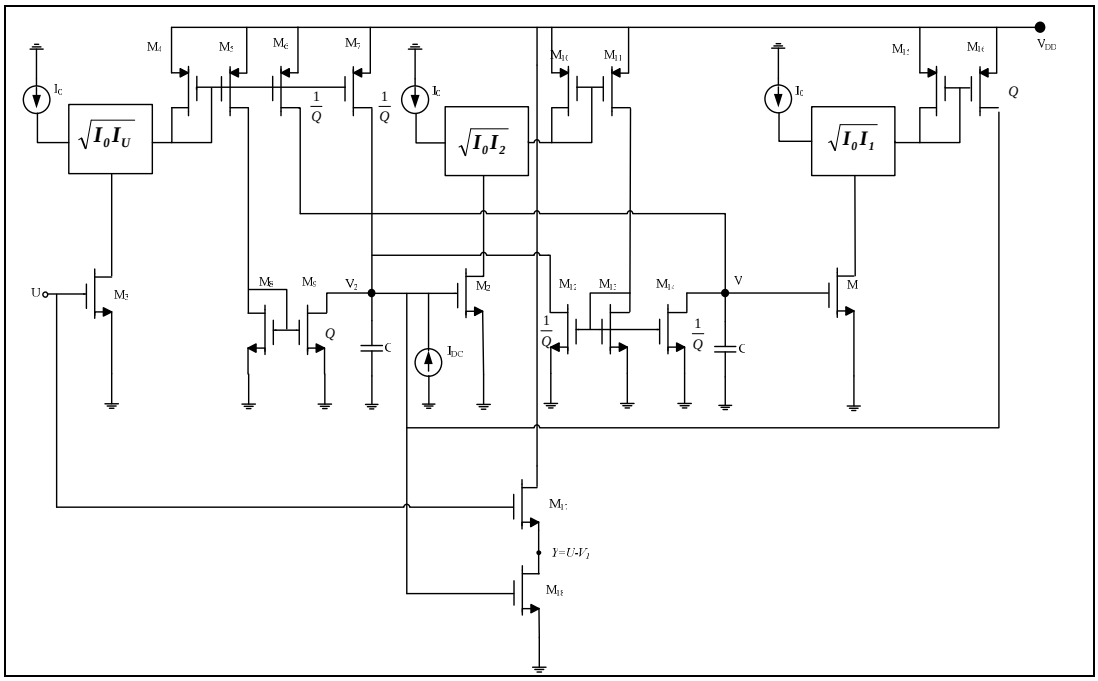

Figure 4. 9 Modified square root domain second order highpass filter

Table 4. 2 The parameters of the second order highpass filter

Parameter values	
V_{DD}	2.5V
U (D.C. voltage)	1.4V
C	5pF
Q	1
I_0	10μA
I_{DC}	21.99μA
Aspect ratio of transistor M_1 - M_3, M_{17} and M_{18}	10μm/10μm
Aspect ratios of transistors M_4-M_{16}	0.7μm/7μm

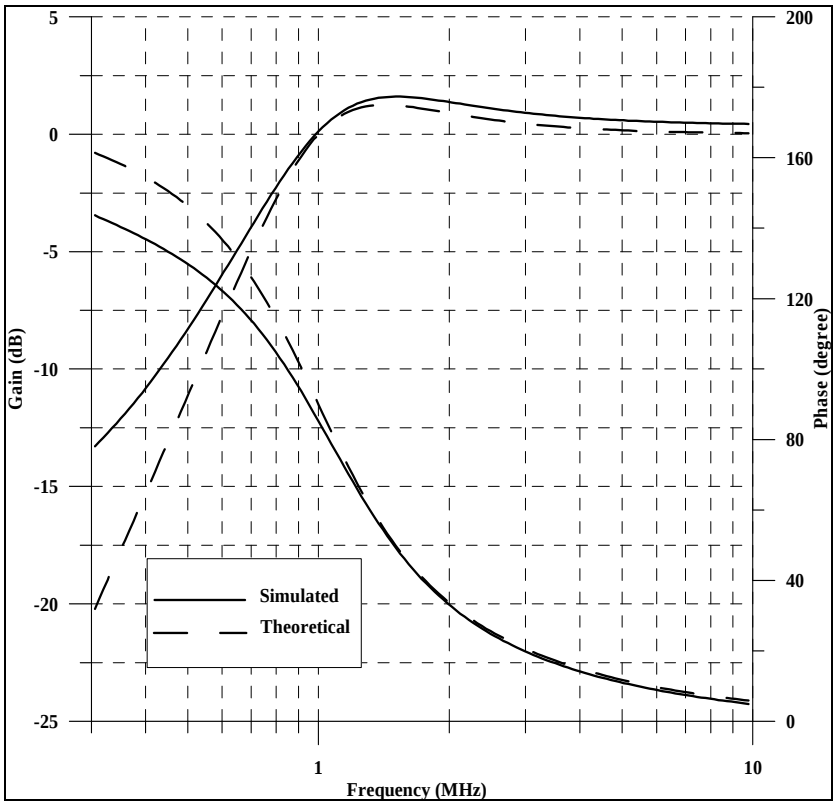

Figure 4. 10 Gain and phase responses of the second order highpass filter

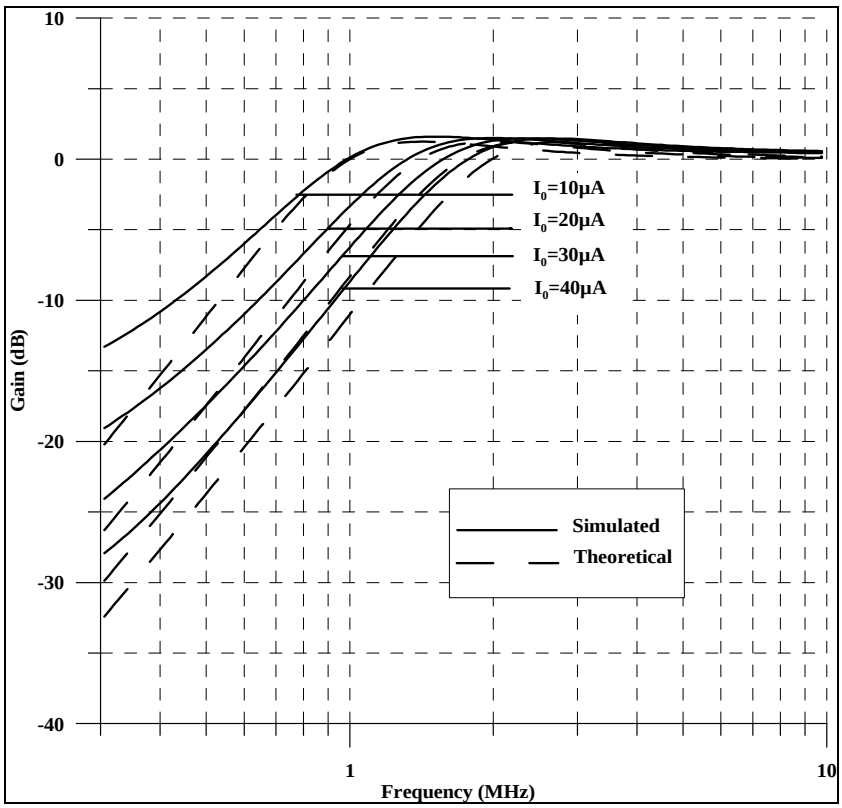

Figure 4. 11 Electronically tuneable gain response of the second order highpass filter for I_0 is 10µA, 20µA, 30µA, and 40µA

W/L ratio of M_6, M_7, M_9, M_{12}, M_{14}, and M_{16} transistors and value of I_{DC} current source are changed to adjust the quality factor. Figure 4.12 shows the gain response of the second order highpass filter, while quality factor is 0.1, 0.5, 1, 2, and 5.

The time response of the filter was investigated by applying a sinusoidal signal to input when its amplitude was 10mV at 1MHz under the conditions in Table 4.2. This causes 262ns time delay at the output of the filter corresponding to 94.32° phase difference as shown in Figure 4.13. The dependence of the output harmonic distortion of second order highpass filter on input signal amplitude was illustrated in Figure4.14. As shown in this figure, THD increases with input signal. As such, input signal must be 130 mV or less to avoid output distortion.

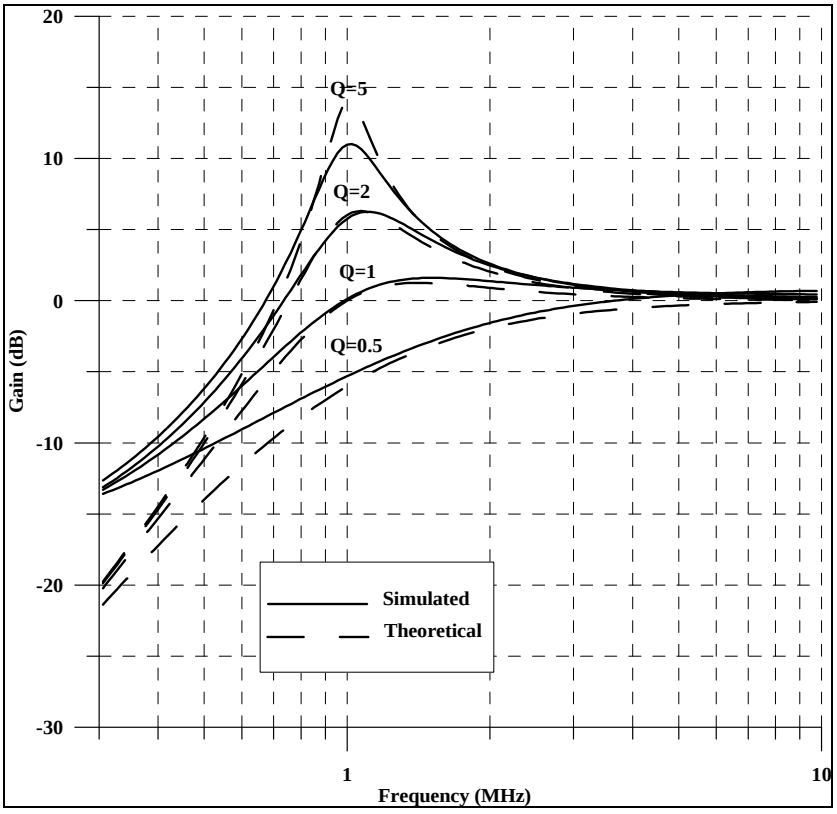

Figure 4. 12 The gain response of the second order highpass filter for Q is 0.5, 1, 2, and 5

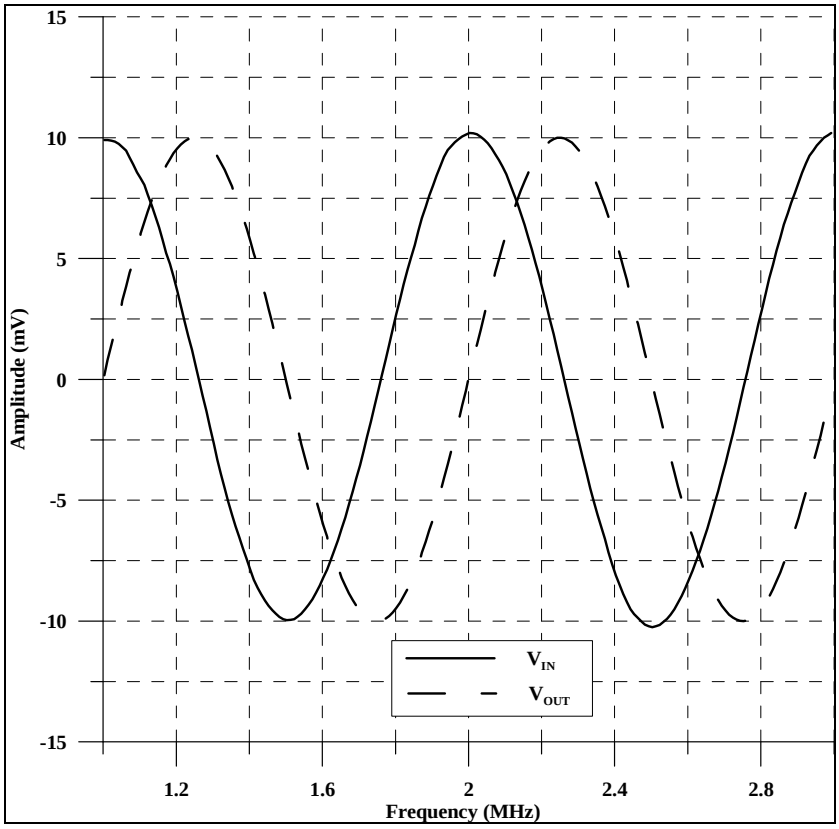

Figure 4. 13 The time response of the second order highpass filter

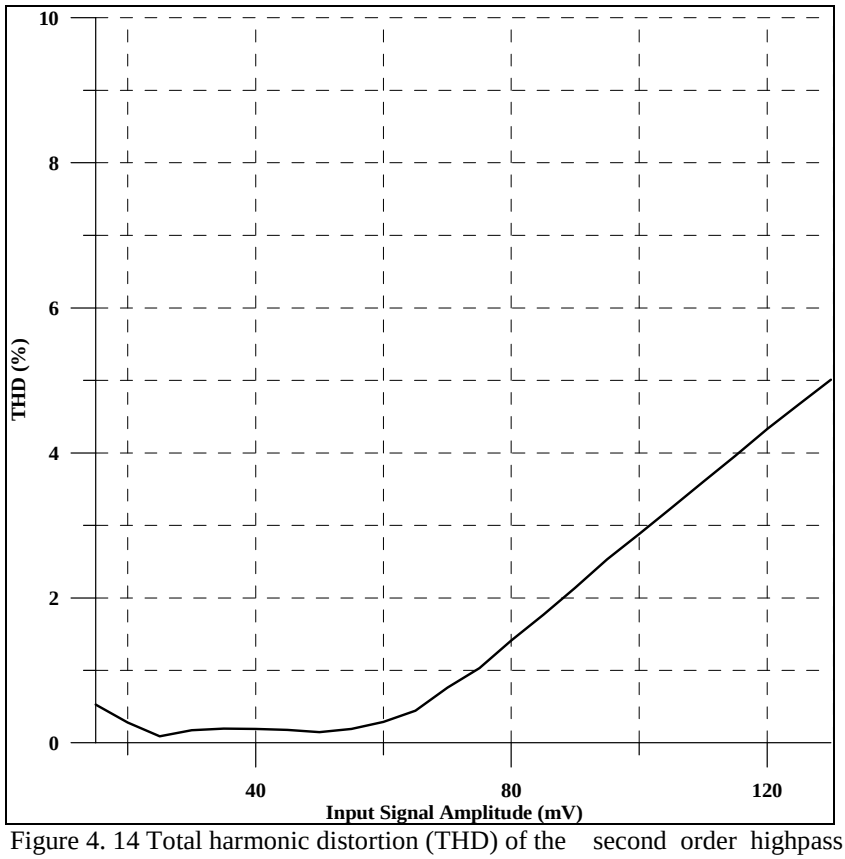

Figure 4. 14 Total harmonic distortion (THD) of the second order highpass filter as a function of input signal amplitude at 1MHz

Monte Carlo simulation was used to examine the performance of the second order highpass fiter in terms of the sensitivity of MOS transistor parameter mismatch and tolerances of the capacitors. For performing the Monte Carlo analysis, *W* and *L* dimensions of the all transistors in the filter have uniform distribution with 5% tolerances and the capacitor in the filter circuit have uniform deviation with 10% tolerances. The gain response of the second order highpass filter with Monte Carlo analysis for 100 runs is shown in Figure 4.15 under the conditions in Table 4.2. The cut off frequency was obtained between 999KHz and 1.17MHz during the analysis.

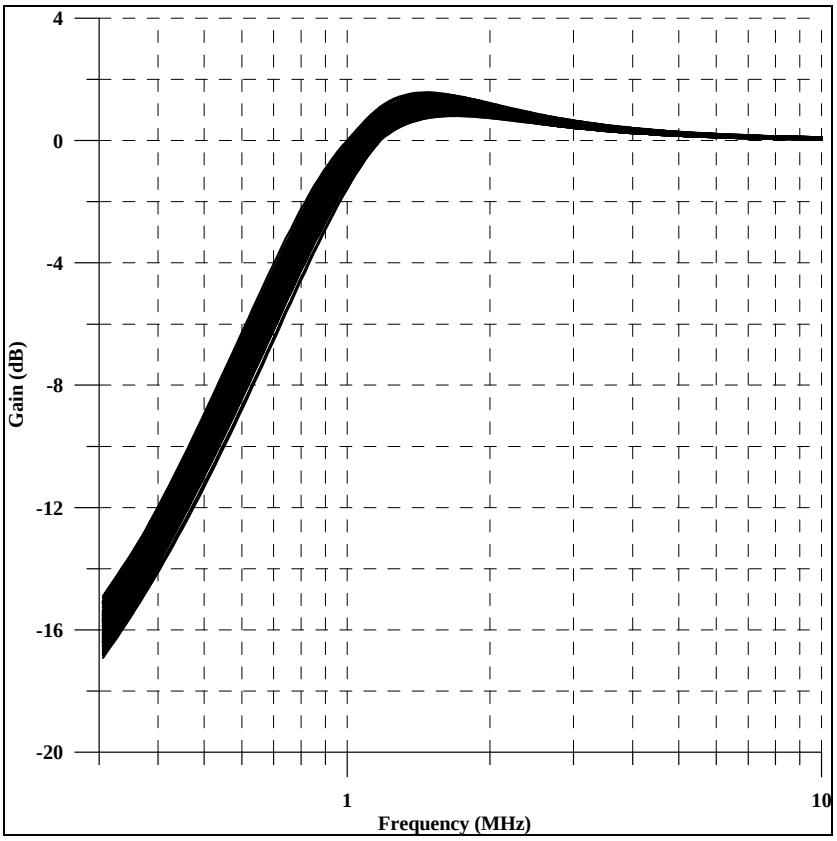

Figure 4. 15 Gain response of the second order filter with Monte Carlo analysis

4.3 Second Order Bandpass Filter

In the literature, a square root domain second order bandpass filter designed with state space synthesis method by Yu and others in 2005. In this thesis, a square root domain bandpass filter is introduced that its state space representation was obtained

by using companion form technique. The transfer function of second order band pass filter is expressed as

$$H(s) = \frac{\frac{\omega_0}{Q} s}{s^2 + \frac{\omega_0}{Q} s + \omega_0^2} \tag{4.16}$$

where ω_0, Q are cut-off frequency and quality factor, respectively. The state space representation obtained by using companion form technique is expressed as

$$\dot{x}_1 = x_2 + \frac{\omega_0}{Q} u \tag{4.17}$$

$$\dot{x}_2 = -\omega_0^2 x_1 - \frac{\omega_0}{Q} x_2 - \frac{\omega_0^2}{Q^2} u$$

$$y = x_1$$

To realize the filter, state variable x_2 is multiplied with $-\omega_0/Q$. So the final state equations are obtained;

$$\dot{x}_1 = -\frac{\omega_0}{Q} x_2 + \frac{\omega_0}{Q} u \tag{4.18}$$

$$\dot{x}_2 = Q\omega_0 x_1 - \frac{\omega_0}{Q} x_2 + \frac{\omega_0}{Q} u$$

$$y = x_1$$

If the node voltage V_1 , V_2 and voltage signal U are assumed the state variables x_1, x_2, and input u, state and output equations in (4.18) are rewritten as

$$C\dot{V}_1 = -C\frac{\omega_0}{Q} V_2 + C\frac{\omega_0}{Q} U \tag{4.19}$$

$$C\dot{V}_2 = QC\omega_0 V_1 - \frac{C\omega_0}{Q} V_2 + \frac{C\omega_0}{Q} U$$

$$y = V_1$$

where C is a capacitor value seemed as multiplying factor. $C\dot{V}_1$ and $C\dot{V}_2$ are accepted a current flows through a grounded capacitor C whose voltage across its terminals in order given V_1 and V_2 and by assuming that U, V_2, and V_1 are gate-source voltages of MOS transistors operating in saturation region with their drain currents are defined as I_u, I_2, and I_1, respectively. So capacitor current equations in

(4.19) are arranged as

$$I_{C1} = -\frac{C\omega_0}{Q}\left(\sqrt{\frac{I_2}{\beta}} + V_{TH}\right) + \frac{C\omega_0}{Q}\left(\sqrt{\frac{I_u}{\beta}} + V_{TH}\right) \tag{4.20}$$

$$I_{C2} = QC\omega_0\left(\sqrt{\frac{I_1}{\beta}} + V_{TH}\right) - \frac{C\omega_0}{Q}\left(\sqrt{\frac{I_2}{\beta}} + V_{TH}\right) + \frac{C\omega_0}{Q}\left(\sqrt{\frac{I_u}{\beta}} + V_{TH}\right)$$

where $I_1=\beta(V_1-V_{TH})^2$, $I_2=\beta(V_2-V_{TH})^2$, $I_u=\beta(U-V_{TH})^2$, $I_{C1} = C\dot{V}_1$, and $I_{C2} = C\dot{V}_2$. Hence, the state equations in (4.20) are transformed into

$$I_{C1} = -\frac{1}{Q}\sqrt{I_0 I_2} + \frac{1}{Q}\sqrt{I_0 I_u} \tag{4.21}$$

$$I_{C2} = Q\sqrt{I_0 I_1} - \frac{1}{Q}\sqrt{I_0 I_2} + \frac{1}{Q}\sqrt{I_0 I_u} + QI_{TH}$$

where the bias current $I_0 = (\omega_0{}^2 C^2)/\beta$ and threshold voltage compensation current $I_{TH}=\omega_0 C V_{TH}$. The square root domain second order bandpass filter consisting of three geometric mean circuits, current mirror circuits, and two capacitors is shown in Figure 4.16.

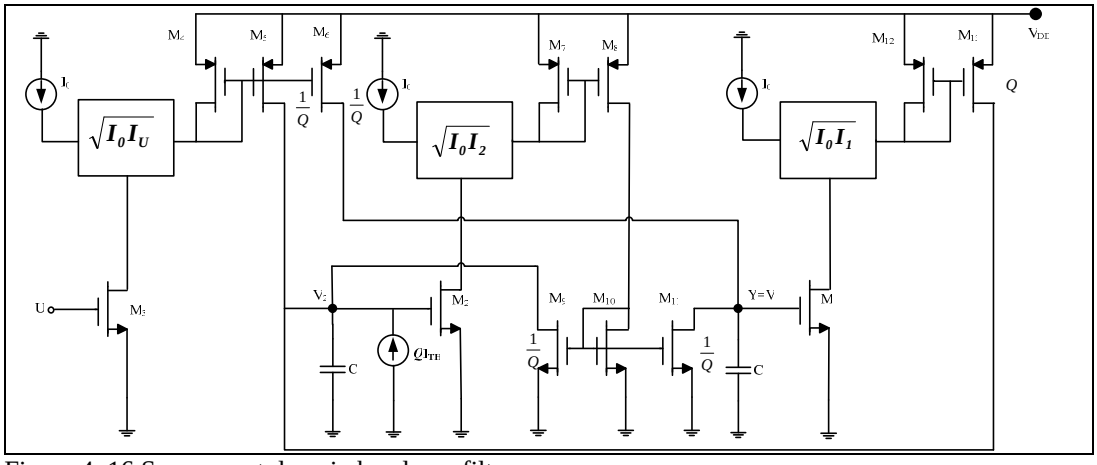

Figure 4. 16 Square root domain bandpass filter

When D.C. operating point analysis is considered, if it is assumed that V_2 is equal to U, and also V_1 , the D.C. operating condition in the first state equation is provided and there is no need to add any bias current to this equation. Under these conditions second state equation is rearranged as;

$$C\dot{V}_2 = QC\omega_0 U - \frac{C\omega_0}{Q}U + \frac{C\omega_0}{Q}U \tag{4.22}$$

To equate the D.C. terms of Equation (4.22) to zero a D.C. current is added

$$C\dot{V}_2 = QC\omega_0 U - \frac{C\omega_0}{Q}U + \frac{C\omega_0}{Q}U + I_{DC} = 0 \tag{4.23}$$

where I_{DC}=-$QC\omega_0 U$. By substituting the D.C. current source in second state equation in Equation (4.21)

$$I_{C2} = Q\sqrt{I_0 I_1} - \frac{1}{Q}\sqrt{I_0 I_2} + \frac{1}{Q}\sqrt{I_0 I_u} + QI_{TH} + I_{DC} \tag{4.24}$$

Since I_{TH} is also a D.C. current source, an external current I_{bias} added to second state equation is

$$I_{bias} = QC\omega_0 V_{TH} - QC\omega_0 U \tag{4.25}$$

On the way of rearrangements, the modified square root domain second order bandpass filter circuit is indicated in Figure 4.17.

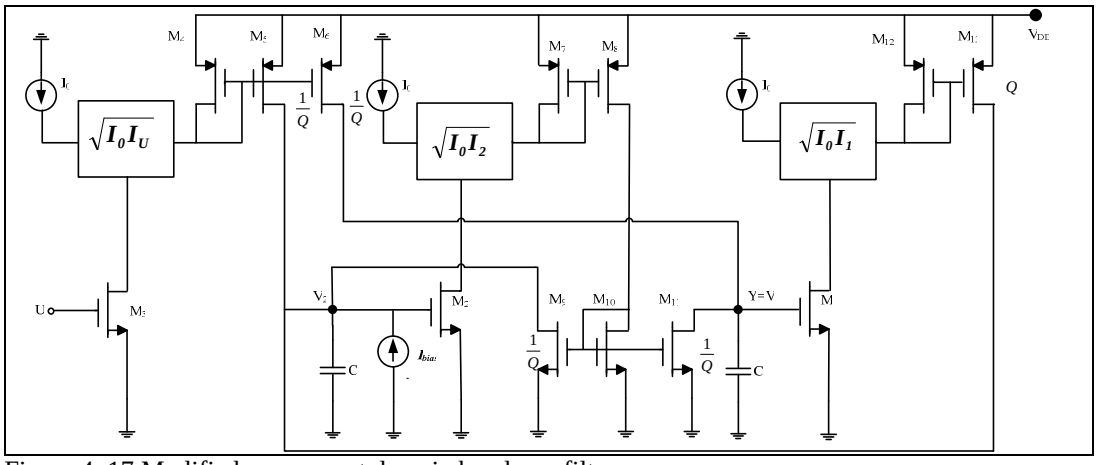

Figure 4. 17 Modified square root domain bandpass filter

The presented second order bandpass filter was simulated with values of parameters given in Table 4.3 by using TSMC 0.25µm CMOS Level 3 model parameters (Appendix). Under these conditions, theoretical cut-off frequency is 1.65 MHz while simulated is 1.60 MHz. Gain and phase responses of the second order bandpass filter are indicated in Figure 4.18 with theoretical response. Equations show that the cut off frequency of the filter can be adjustable. According to bias current value, gain response of the filter for four different bias currents, from 10µA to 40µA, is depicted in Figure 4.19 with theoretical response.

Table 4. 3 The parameters of the second order bandpass filter

Parameter values	
V_{DD}	2.5V
U (D.C. voltage)	0.75V
C	3pF
Q	1
I_0	10μA
I_{bias}	-10.92μA
Aspect ratio of transistor M_1 - M_3	10μm/10μm
Aspect ratios of transistors M_4-M_{13}	0.7μm/7μm

W/L ratio of M_5, M_6, M_9, $M_{11,}$ and M_{13} transistors and value of I_{bias} current source are changed to adjust the quality factor. Figure 4.20 shows the gain response of the second order bandpass filter, while quality factor is 0.1, 0.5, 1, 2, and 5 with other parameters in Table 4.3.

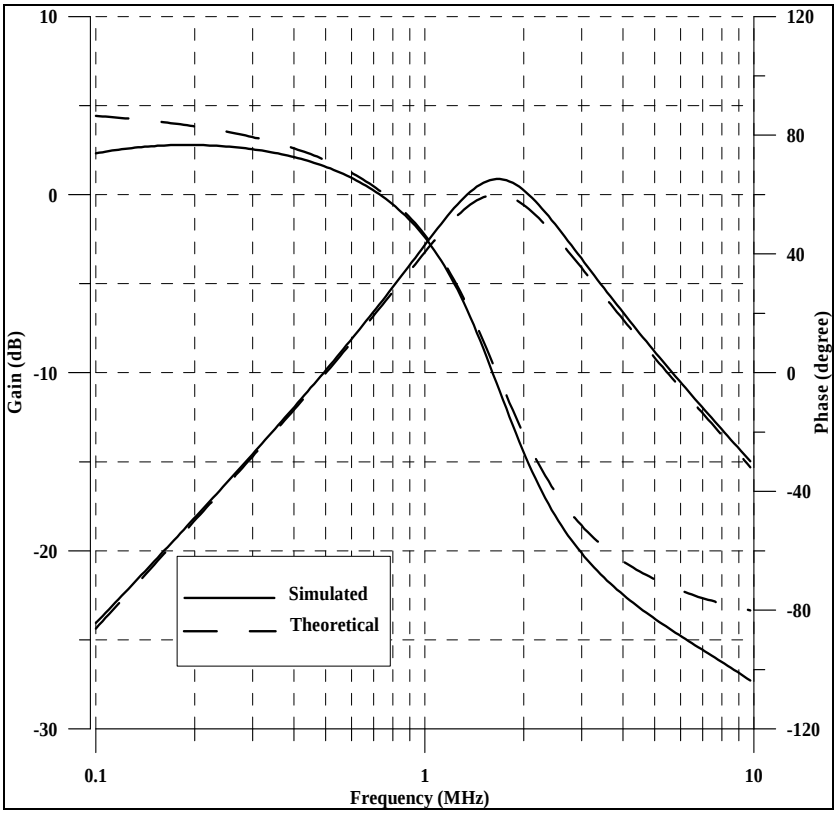

Figure 4. 18 Gain and phase responses of the second order bandpass filter

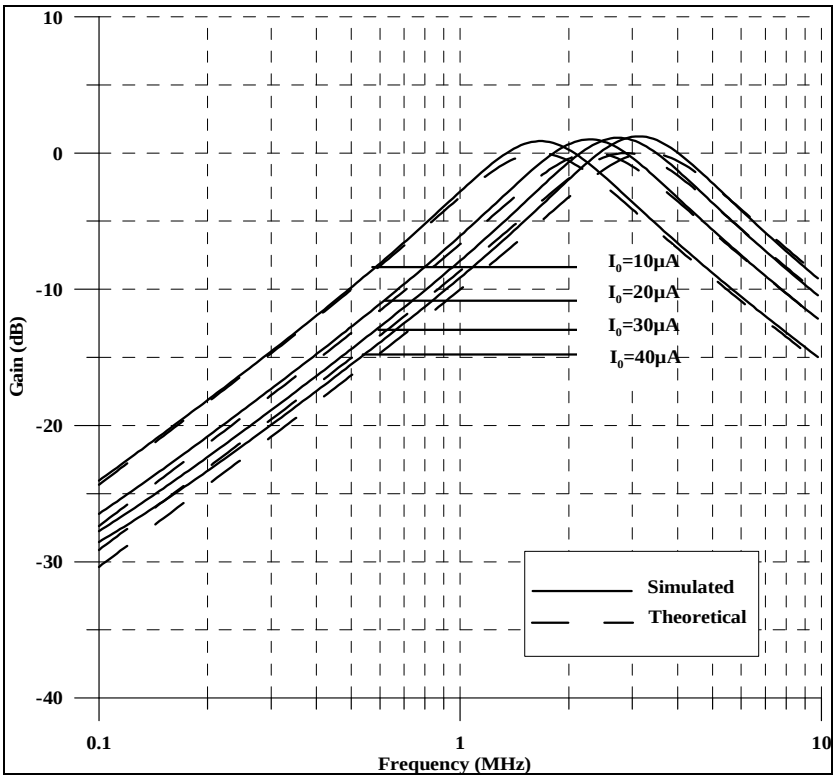

Figure 4. 19 Electronicaly tuneable gain response of the second order bandpass filter for I_0 is 10μA, 20μA, 30μA, and 40μA

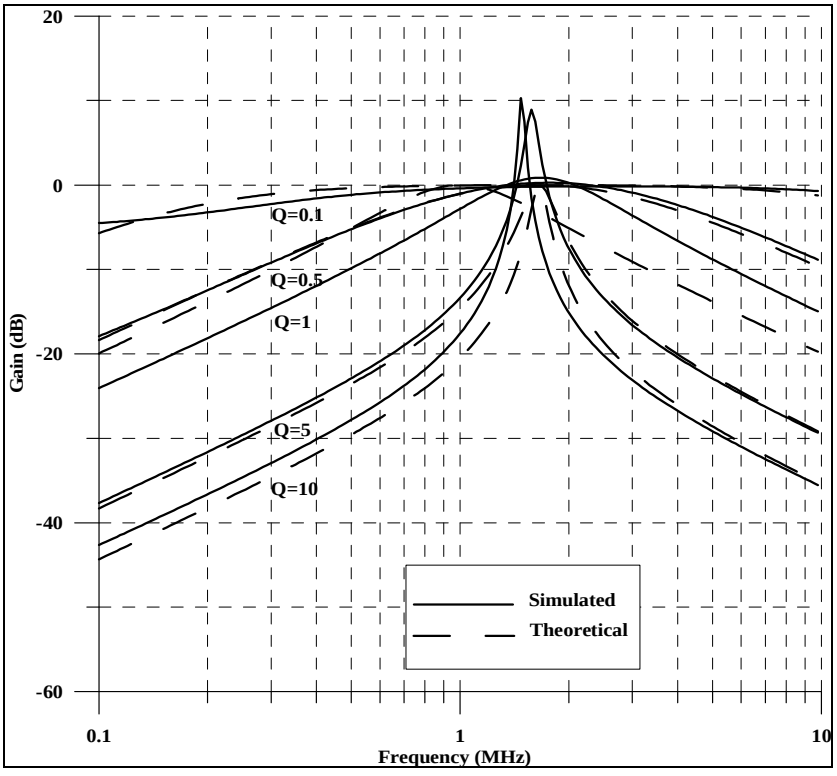

Figure 4. 20 The gain response of the second order bandpass filter for Q is 0.1, 0.5, 1, 5, and 10

The time response with 10mV sinusoidal input voltage at 1.65MHz and the dependence of the harmonic distorition on input signal amplitude of the filter are indicated in Figure 4.22 and 4.23 respectively. As such, input signal must be 200mV or less to avoid output distortion.

The performance of the second order bandpass filter in terms of the sensitivity of MOS transistor parameter mismatch and tolerances of the capacitors has been evaluated by performing Monte Carlo simulations. For performing the Monte Carlo analysis, *W* and *L* dimensions of the all transistors in the filter have uniform distribution with 5% tolerances and the capacitor in the filter circuit have uniform deviation with 10% tolerances. The gain response of the second order bandpass filter with Monte Carlo analysis for 100 runs is shown in Figure 4.24 when the cut off frequency is 1.65MHz.

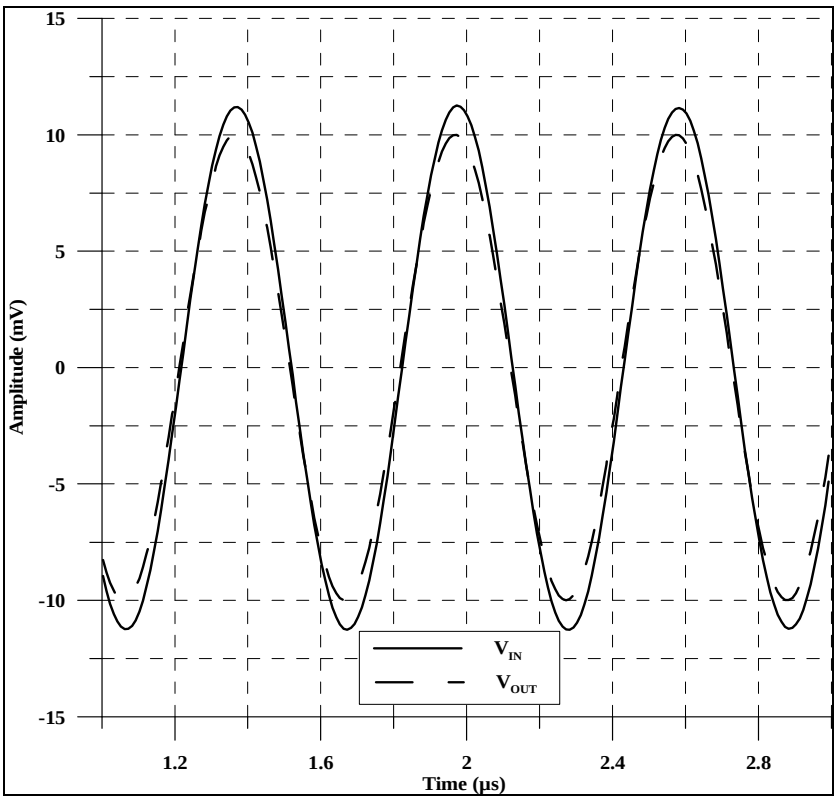

Figure 4. 21 The time response of the second order bandpass filter

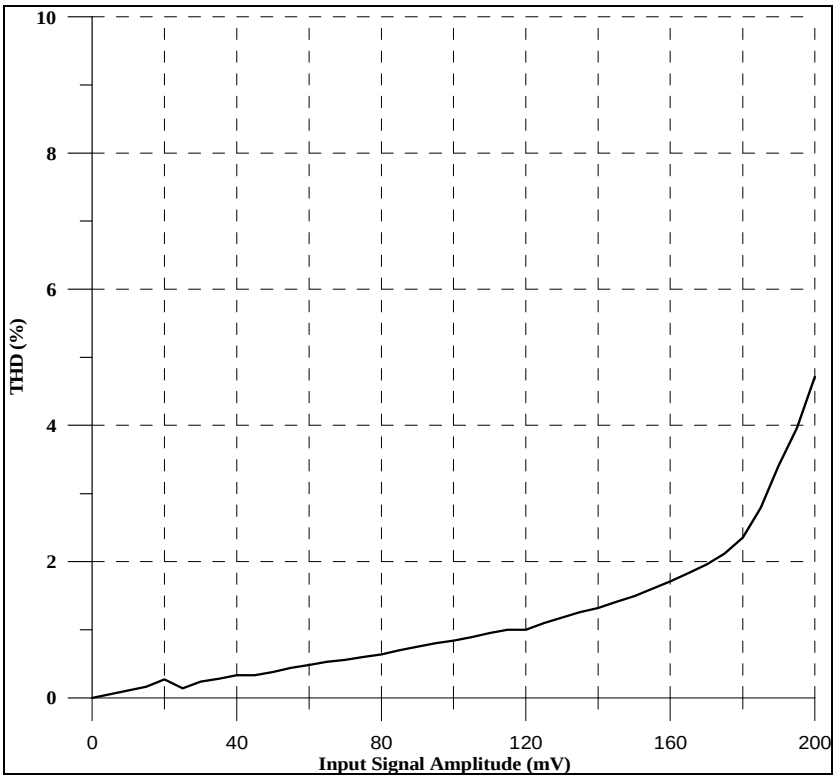

Figure 4. 22 Total harmonic distortion (THD) of presented second order bandpass filter as a function of input signal amplitude at 1.65MHz

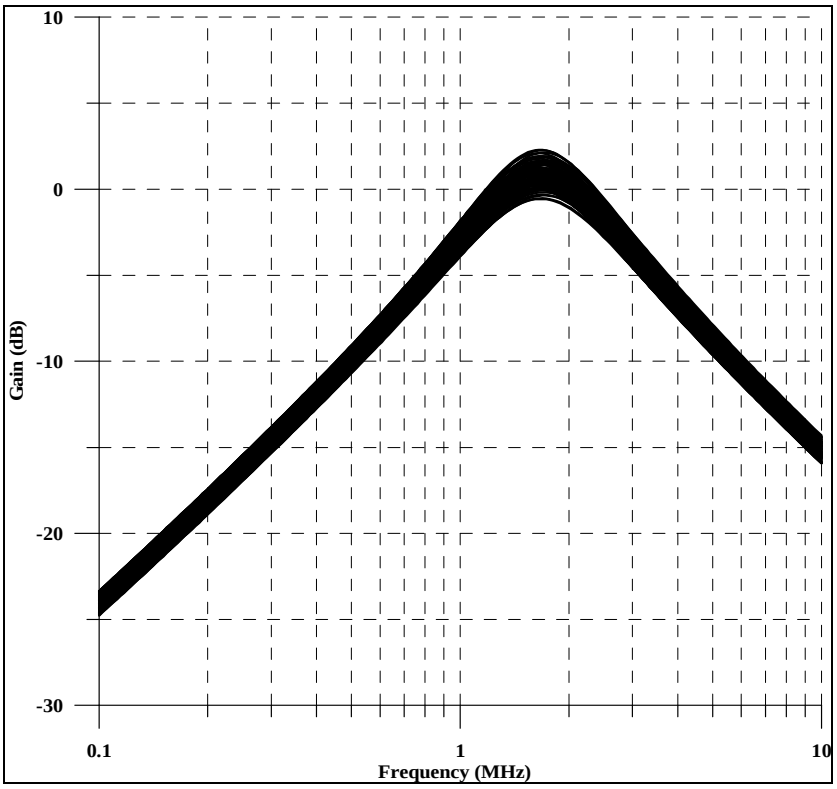

Figure 4. 23 Gain response of the second order bandpass filter with Monte Carlo analysis

4.4 Second Order Notch Filter

In the literature, there is a square root domain notch filter in current mode designed by Kırçay, Keserlioğlu, and Çam in 2009. In this thesis, a square root domain notch filter in voltage mode was designed by using different state space form and has a simpler circuit structure. The transfer function of second order notch filter is expressed as

$$H(s) = \frac{s^2 + \omega_n^2}{s^2 + \frac{\omega_0}{Q}s + \omega_0^2} \tag{4.26}$$

where ω_0, ω_n, and Q are cut-off frequency, notch frequency and quality factor, respectively. The state space representation obtained by using observable canonical form is expressed as

$$\dot{x}_1 = -\omega_0^2 x_2 + (\omega_n^2 - \omega_0^2)u \tag{4.27}$$

$$\dot{x}_2 = x_1 - \frac{\omega_0}{Q}x_2 - \frac{\omega_0}{Q}u$$

$$y = x_2 + u$$

To realize the filter, state variable x_1 and x_2 are multiplied with ω_0 and -1, respectively. So the final state equations are obtained;

$$\dot{x}_1 = \omega_0 x_2 + \frac{\omega_n^2}{\omega_0}u - \omega_0 u \tag{4.28}$$

$$\dot{x}_2 = -\omega_0 x_1 - \frac{\omega_0}{Q}x_2 + \frac{\omega_0}{Q}u$$

$$y = -x_2 + u$$

If the node voltage V_1 , V_2 and voltage signal U are assumed the state variables x_1, x_2, and u, state and output equations in (4.28) are rewritten as

$$C\dot{V}_1 = C\omega_0 V_2 + C\frac{\omega_n^2}{\omega_0}U - C\omega_0 U \tag{4.29}$$

$$C\dot{V}_2 = -C\omega_0 V_1 - C\frac{\omega_0}{Q}V_2 + C\frac{\omega_0}{Q}U$$

$$y = -V_2 + U$$

where C is a capacitor value seemed as multiplying factor. $C\dot{V}_1$ and $C\dot{V}_2$ are accepted a current flows through a grounded capacitor C whose voltage across its terminals in order given V_1 and V_2 and by assuming that U, V_2, and V_1 are gate-source voltages of MOS transistors operating in saturation region with their drain currents are defined as I_u, I_2, and I_1, respectively. So capacitor current equations in (4.29) are arranged that

$$I_{C1} = C\omega_0\left(\sqrt{\frac{I_2}{\beta}} + V_{TH}\right) + C\frac{\omega_n^2}{\omega_0}\left(\sqrt{\frac{I_u}{\beta}} + V_{TH}\right) - C\omega_0\left(\sqrt{\frac{I_u}{\beta}} + V_{TH}\right) \quad (4.30)$$

$$I_{C2} = -C\omega_0\left(\sqrt{\frac{I_1}{\beta}} + V_{TH}\right) - \frac{C\omega_0}{Q}\left(\sqrt{\frac{I_2}{\beta}} + V_{TH}\right) + \frac{C\omega_0}{Q}\left(\sqrt{\frac{I_u}{\beta}} + V_{TH}\right)$$

where $I_1=\beta(V_1-V_{TH})^2$, $I_2=\beta(V_2-V_{TH})^2$, $I_u=\beta(U-V_{TH})^2$, $I_{C1} = C\dot{V}_1$, and $I_{C2} = C\dot{V}_2$. Hence, the state equations in (4.30) are transformed into

$$I_{C1} = \sqrt{I_0 I_2} + \frac{\omega_n^2}{\omega_0^2}\sqrt{I_0 I_u} - \sqrt{I_0 I_u} + \frac{\omega_n^2}{\omega_0^2} I_{TH} \quad (4.31)$$

$$I_{C2} = -\sqrt{I_0 I_1} - \frac{1}{Q}\sqrt{I_0 I_2} + \frac{1}{Q}\sqrt{I_0 I_u} - I_{TH}$$

where the bias current $I_0 = (\omega_0{}^2 C^2)/\beta$ and threshold voltage compensation current $I_{TH}=\omega_0 C V_{TH}$. There is an important point that, if a regular notch filter is designed when ω_n is equal to ω_0, second state equation remains constant but first state equation in Equation (4.31) is rearranged that

$$I_{C1} = \sqrt{I_0 I_2} + I_{TH} \quad (4.32)$$

So, the construction of the filter gets smaller. Square root domain notch filter has three cases as regular notch, lowpass notch, and highpass notch consisting of three geometric mean circuits, current mirror circuits, a summation block, and two capacitors as shown in Figure 4.24.

It is known that D.C. operating points are very important to make circuits operate. Because output equation is a difference equation, V_2 must not be equal to U.

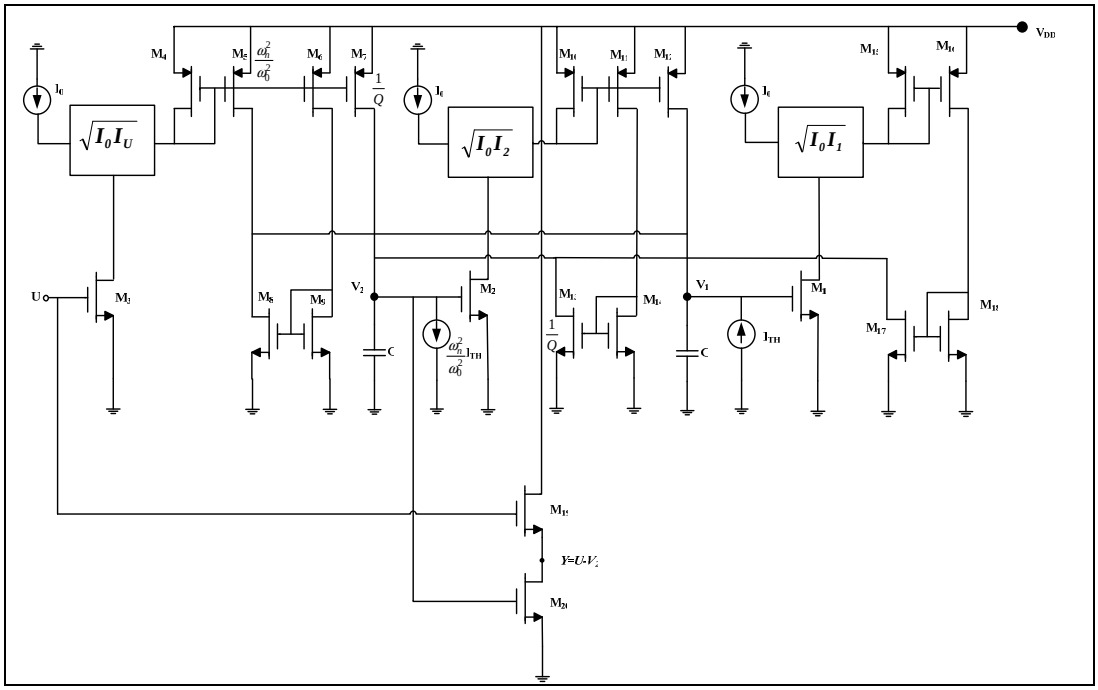

Figure 4. 24 Square root domain second order notch filter

If it is supposed that $U/2$ is equal to V_2 , and also $V_1/2$, state equations are rearranged as;

$$C\dot{V}_1 = C\omega_0 \frac{U}{2} + C\frac{\omega_n^2}{\omega_0}U - C\omega_0 U \tag{4.33}$$

$$C\dot{V}_2 = -C\omega_0 U - C\frac{\omega_0}{Q}\frac{U}{2} + C\frac{\omega_0}{Q}U$$

To equate the D.C. terms of Equation (4.33) to zero a D.C. currents are added

$$C\dot{V}_1 = C\omega_0 \frac{U}{2} + C\frac{\omega_n^2}{\omega_0}U - C\omega_0 U + I_{DC1} \tag{4.34}$$

$$C\dot{V}_2 = -C\omega_0 U - C\frac{\omega_0}{Q}\frac{U}{2} + C\frac{\omega_0}{Q}U + I_{DC2}$$

where $I_{DC1} = C\omega_0 U(\frac{1}{2} - \frac{\omega_n^2}{\omega_0^2})$ and $I_{DC2} = C\omega_0 U(\frac{1}{2Q} - 1)$. By substituting the D.C. current source in second state equation in Equation (4.31)

$$I_{C1} = \sqrt{I_0 I_2} + \frac{\omega_n^2}{\omega_0^2}\sqrt{I_0 I_u} - \sqrt{I_0 I_u} + \frac{\omega_n^2}{\omega_0^2} I_{TH} + I_{DC1} \tag{4.35}$$

$$I_{C2} = -\sqrt{I_0 I_1} - \frac{1}{Q}\sqrt{I_0 I_2} + \frac{1}{Q}\sqrt{I_0 I_u} - I_{TH} + I_{DC2}$$

Since I_{TH} is also a D.C. current source, an external current I_{bias1} and I_{bias2} are added to state equations respectively.

$$I_{bias1} = \frac{\omega_n^2}{\omega_0^2} C\omega_0 V_{TH} + C\omega_0 U(\frac{1}{2} - \frac{\omega_n^2}{\omega_0^2}) \tag{4.36}$$

$$I_{bias2} = -C\omega_0 V_{TH} + C\omega_0 U(\frac{1}{2Q} - 1)$$

On the way of rearrangements, the modified square root domain second order notch filter circuit is indicated in Figure 4.25.

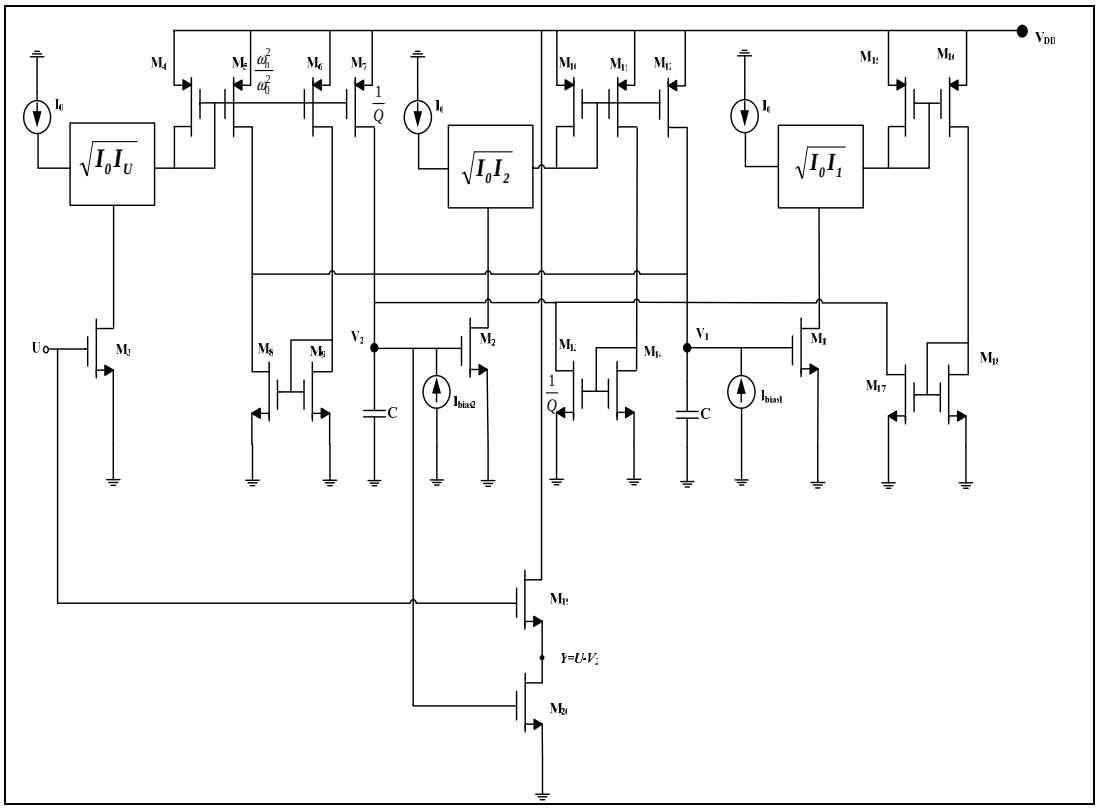

Figure 4. 25 Modified square root domain notch filter

By using TSMC 0.25µm CMOS Level 3 model parameters (Appendix), the proposed first lossless integrator was simulated with values of integrator parameters

given in Table 4.4.The simulations was repeated for three cases; regular notch, low-pass notch, and high-pass notch filter.

Table 4. 4 The parameters of the proposed second order notch filter

Parameter values	
Q	1
V_{DD}	2.5V
U (D.C. voltage)	1.4V
C	5pF
I_0	10µA
Aspect ratio of transistor M_1 - M_3	7µm/7µm
Aspect ratios of transistors M_4 - M_9	0.7µm/14µm
Aspect ratios of transistors M_{10} - M_{18}	0.7µm/7µm
Aspect ratios of transistors M_{19} and M_{20}	10µm/10µm

4.4.1 Regular Notch

While the notch frequency is equal to center frequency of the filter, regular notch filter is obtained. Under the conditions in Table 4.4 the cut-off frequency is theoretically 992 KHz; the simulation result was 978 KHz. Figure 4.26 shows the gain and phase responses of the regular notch filter under these conditions with theorstical results. The center frequency of the filter can be tunable by changing the bias current I_0. The theoretical and simulation results for different bias current are indicated in Figure 4.27. The quality factor tuning of the notch filter is done by changing the dimensions of the M_7 and M_{13} transistors used in current mirrors. Figure 4.28 shows the quality factor tuning of the regular notch filter. The gain

response of the regular notch filter with Monte Carlo analysis for 100 runs is shown in Figure 4.29 under the conditions in Table 4.4 and *W* and *L* dimensions of the all transistors and the capacitor in the filter have uniform distribution with 10 % tolerances and 5% tolerances, respectively. The cut off frequency was obtained between 963KHz and 1.19MHz during the analysis.

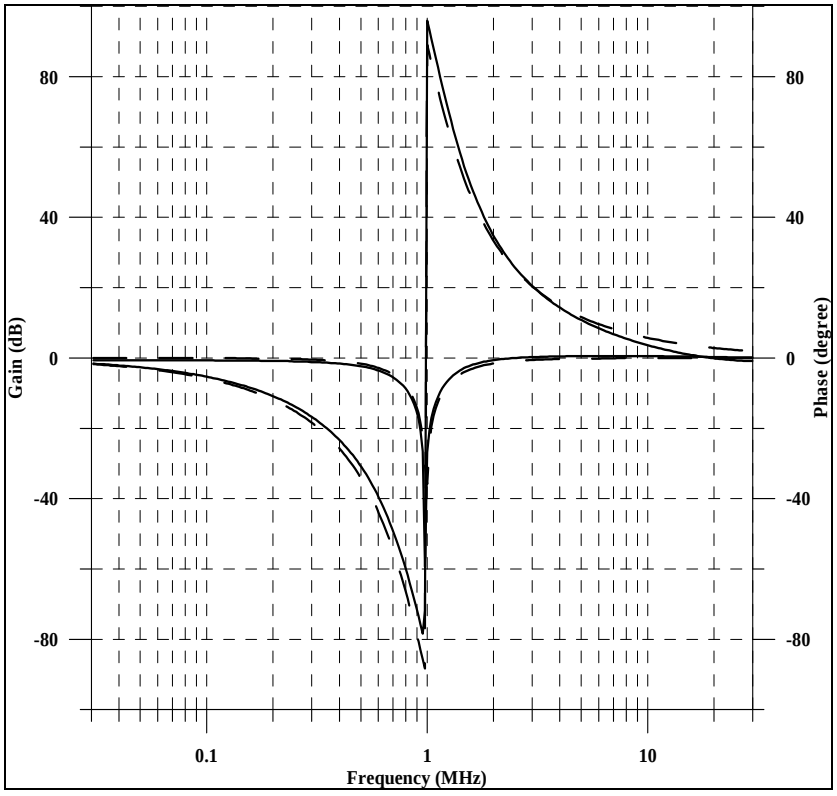

Figure 4. 26 Gain and phase responses of the regular notch filter

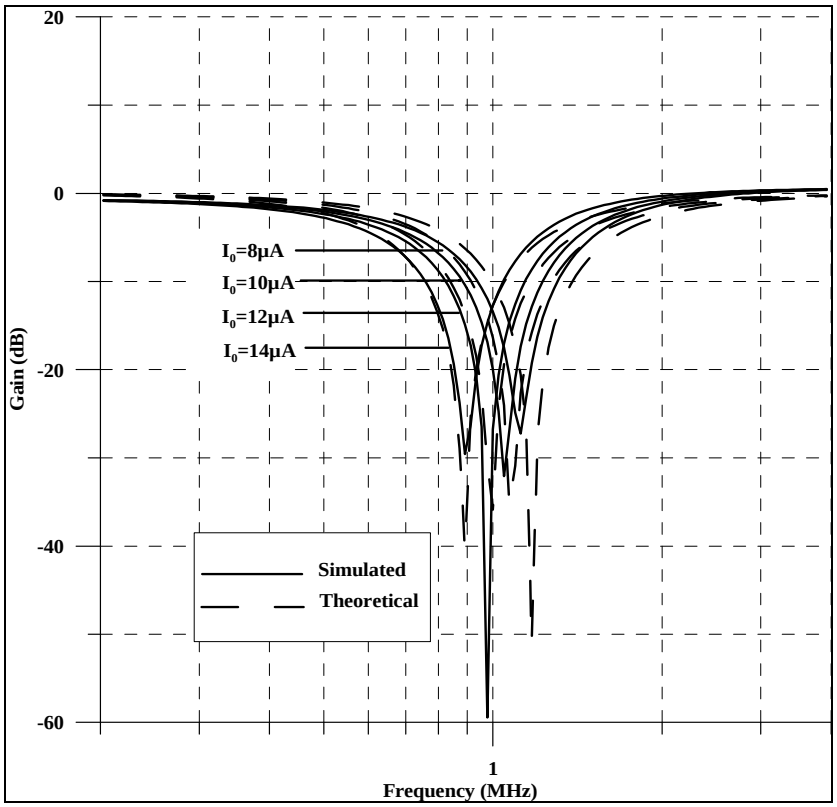

Figure 4. 27 Electronically tuneable gain response of the regular notch filter for I_0 is 8µA, 10µA, 12µA, and 14µA

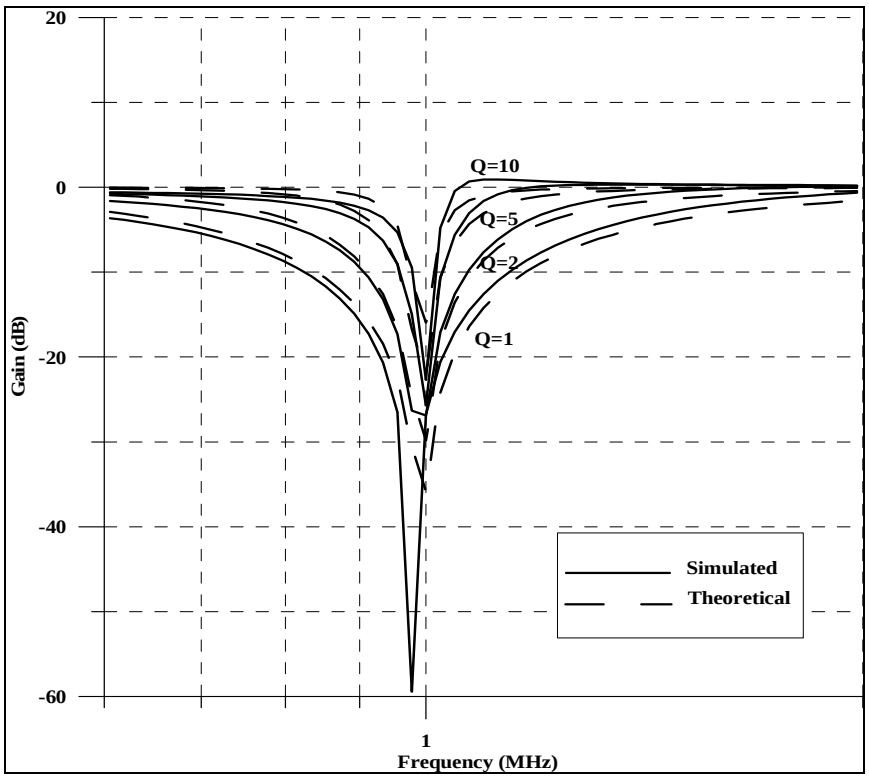

Figure 4. 28 The gain response of the regular notch filter for Q is 1,2,5,and 10

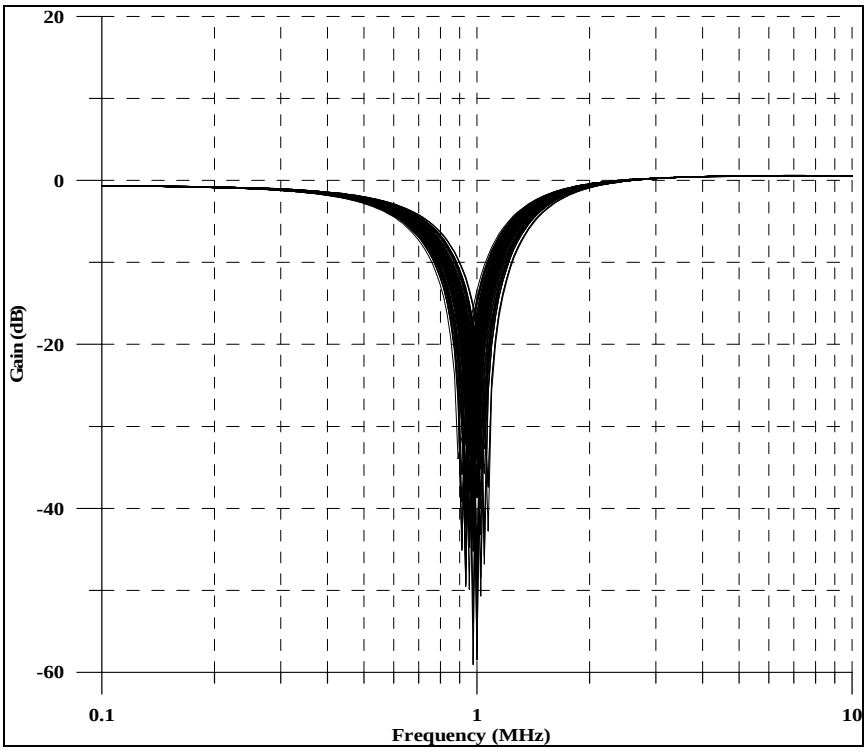

Figure 4. 29 Gain response of the regular notch filter with Monte Carlo analysis

4.4.2 Low-Pass Notch Filter

The low-pass notch filter was obtained when the notch frequency ω_n was greater than the cut-off frequency ω_0 of the filter. The notch frequency was adjusted to 1.2 MHz, and the cut-off frequency of the filter was set to 992 KHz, when the bias current was 10 μA. The gain response of the second order low-pass notch filter is shown in Figure 4.30. The simulated filter notch frequency was 1.19 MHz.

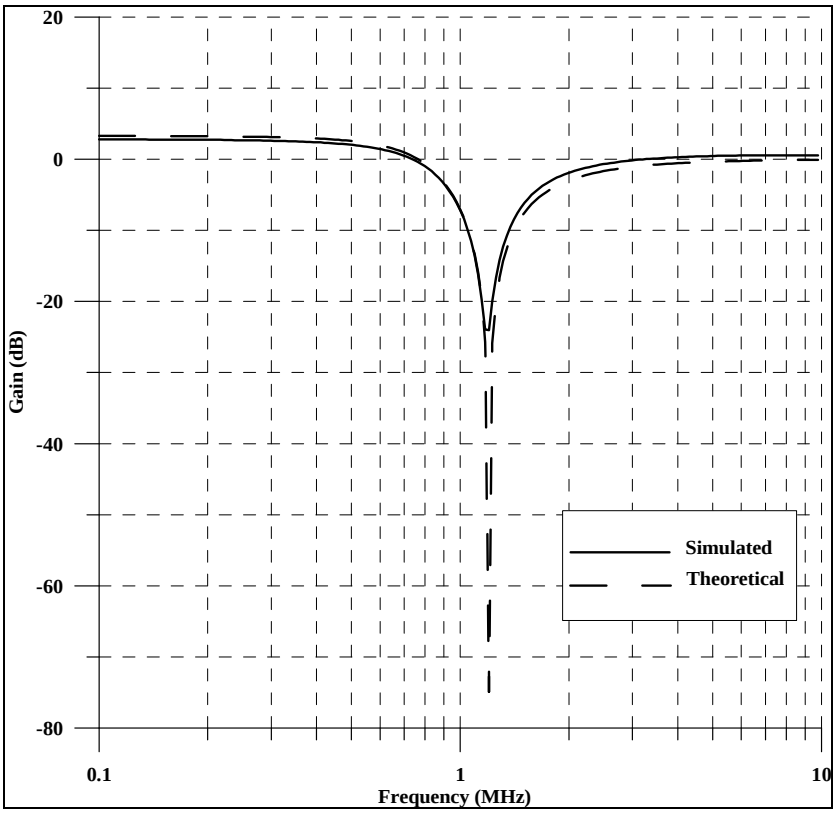

Figure 4. 30 Gain response of the low-pass notch filter

4.4.3 High-Pass Notch Filter

The high-pass notch filter was obtained when ω_n was less than ω_0. The notch frequency and cut-off frequency of the filter were set to 800 KHz and 992 KHz, respectively with bias current 10 μA. Figure 4.31 shows the gain response high-pass and simulation results was observed that notch frequency was 777 KHz.

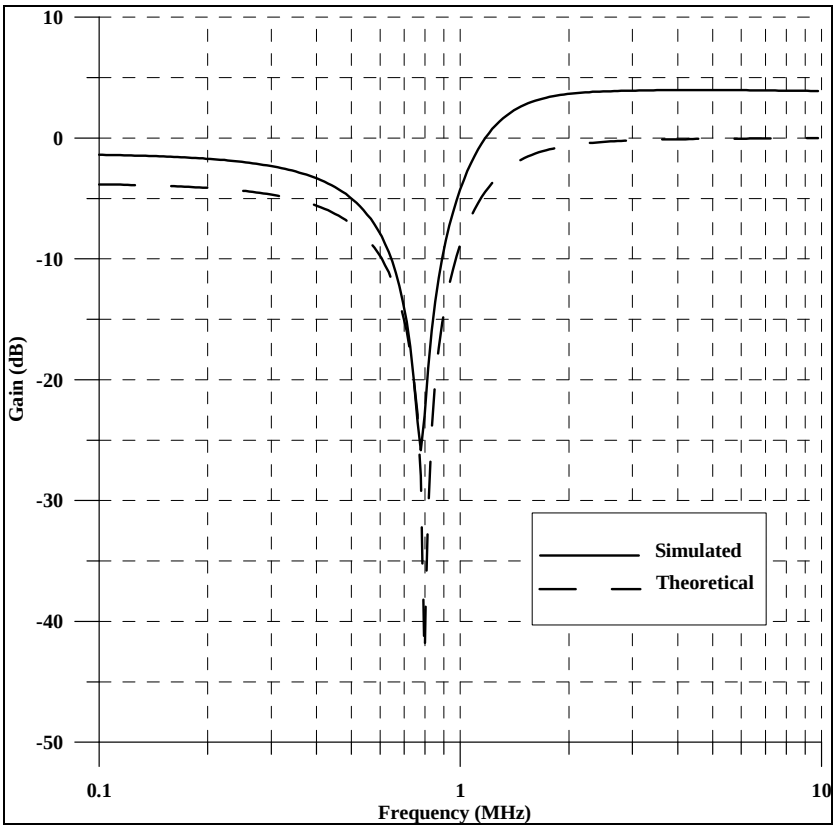

Figure 4. 31 Gain response of the high-pass notch filter

4.5 Second Order Allpass Filter

The square root domain second order allpass filter has a novel property which is presented for the first time in the literature. The transfer function of a second order allpass filter is expressed as

$$H(s) = \frac{s^2 - \frac{\omega_0}{Q}s + \omega_0^2}{s^2 + \frac{\omega_0}{Q}s + \omega_0^2} \tag{4.36}$$

where ω_0 and Q are cut-off frequency and quality factor, respectively. The state space representation obtained by using observable canonical form is expressed as

$$\dot{x}_1 = -\omega_0^2 x_2 \tag{4.37}$$

$$\dot{x}_2 = x_1 - \frac{\omega_0}{Q}x_2 - \frac{2\omega_0}{Q}u$$

$$y = x_2 + u$$

To realize the filter, state variable x_1 and x_2 are multiplied with $3\omega_0/Q$ and -1, respectively. So the final state equations are obtained;

$$\dot{x}_1 = \frac{1}{3} Q \omega_0 x_2 \tag{4.38}$$

$$\dot{x}_2 = -\frac{3\omega_0}{Q} x_1 - \frac{\omega_0}{Q} x_2 + \frac{2\omega_0}{Q} u$$

$$y = -x_2 + u$$

If the node voltage V_1 , V_2 and voltage signal U are assumed the state variables x_1, x_2, and input u, state and output equations in (4.38) are rewritten as

$$C\dot{V}_1 = \frac{1}{3} Q \omega_0 V_2 \tag{4.39}$$

$$C\dot{V}_2 = -\frac{3\omega_0}{Q} V_1 - \frac{\omega_0}{Q} V_2 + \frac{2\omega_0}{Q} U$$

$$y = -V_2 + U$$

where C is a capacitor value seemed as multiplying factor. $C\dot{V}_1$ and $C\dot{V}_2$ are accepted a current flows through a grounded capacitor C whose voltage across its terminals in order given V_1 and V_2 and by assuming that U, V_2, and V_1 are gate-source voltages of MOS transistors operating in saturation region with their drain currents are defined as I_u, I_2, and I_1, respectively. So capacitor current equations in (4.39) are arranged that

$$I_{C1} = \frac{1}{3} QC\omega_0 \left(\sqrt{\frac{I_2}{\beta}} + V_{TH}\right) \tag{4.40}$$

$$I_{C2} = -\frac{3C\omega_0}{Q}\left(\sqrt{\frac{I_1}{\beta}} + V_{TH}\right) - \frac{C\omega_0}{Q}\left(\sqrt{\frac{I_2}{\beta}} + V_{TH}\right) + \frac{2C\omega_0}{Q}\left(\sqrt{\frac{I_u}{\beta}} + V_{TH}\right)$$

where $I_1=\beta(V_1-V_{TH})^2$, $I_2=\beta(V_2-V_{TH})^2$, $I_u=\beta(U-V_{TH})^2$, $I_{C1} = C\dot{V}_1$, and $I_{C2} = C\dot{V}_2$. Hence, the state equations in (4.40) are transformed into

$$I_{C1} = \frac{Q}{3}\sqrt{I_0 I_2} + \frac{Q}{3} I_{TH} \tag{4.41}$$

$$I_{C2} = -\frac{3}{Q}\sqrt{I_0 I_1} - \frac{1}{Q}\sqrt{I_0 I_2} + \frac{2}{Q}\sqrt{I_0 I_u} - \frac{2}{Q} I_{TH}$$

where the bias current $I_0 = (\omega_0{}^2 C^2)/\beta$ and threshold voltage compensation current $I_{TH}=\omega_0 C V_{TH}$. In the light of the design, square root domain second order allpass

filter circuit composed of three geometric mean circuits, current mirror circuits, a summation block, and two capacitors as shown in Figure 4.32.

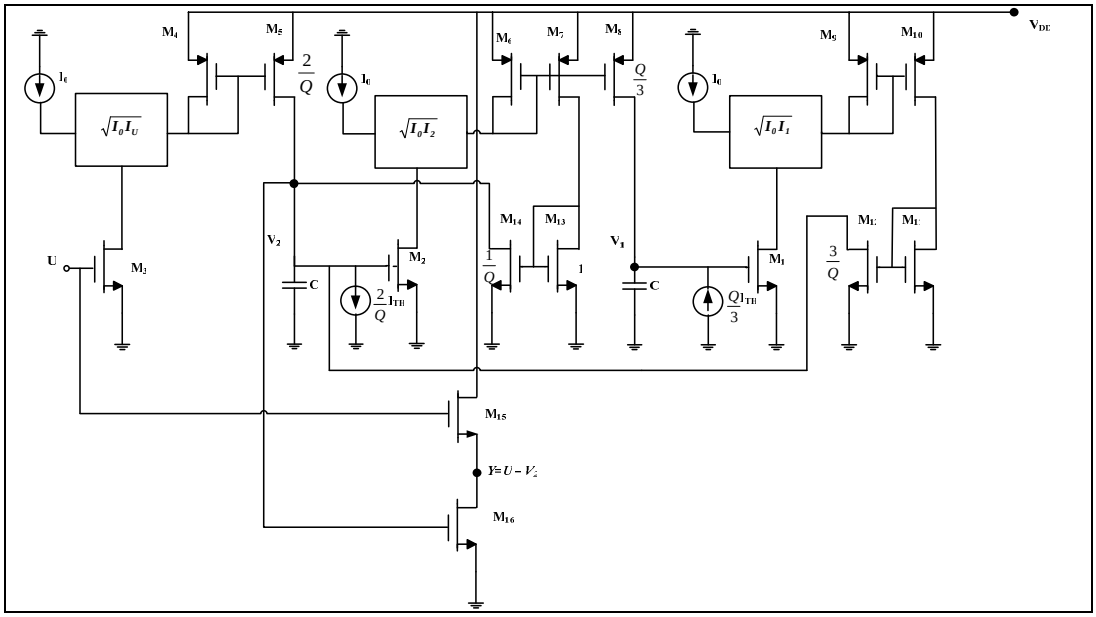

Figure 4. 32 Square root domain second order allpass filter

It is known that D.C. operating points are very important to make circuits operate. Because output equation is a difference equation, V_2 must not be equal to U. When it is considered that V_2 is equal to V_1 and also $U/2$, state equations are rearranged that;

$$C\dot{V}_1 = \frac{1}{3} Q \omega_0 \frac{U}{2} \tag{4.42}$$

$$C\dot{V}_2 = -\frac{3\omega_0 U}{Q2} - \frac{\omega_0 U}{Q2} + \frac{2\omega_0}{Q} U$$

To provide the D.C. operating conditions, D.C. current sources are added to each state equation

$$C\dot{V}_1 = \frac{1}{3} Q \omega_0 \frac{U}{2} + I_{DC1} \tag{4.43}$$

$$C\dot{V}_2 = -\frac{3\omega_0 U}{Q2} - \frac{\omega_0 U}{Q2} + \frac{2\omega_0}{Q} U + I_{DC2}$$

where I_{DC1}=-$QC\omega_0 U/6$ and I_{DC2}=0. By substituting I_{DC1} current source in Equation (4.41)

$$I_{C1} = \frac{Q}{3}\sqrt{I_0 I_2} + I_{bias1} \tag{4.44}$$

where I_{bias1} is $-QC\omega_0 \frac{U}{6} + \frac{Q}{3}\omega_0 C V_{TH}$. After this changing, the modified square root domain second order allpass filter is shown in Figure 4.33.

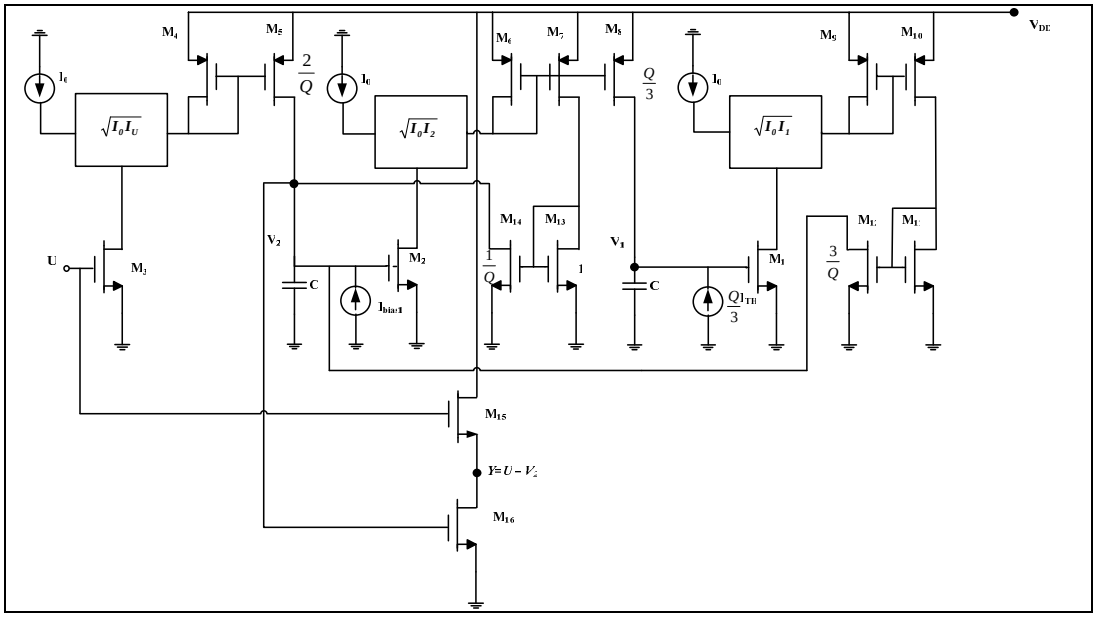

Figure 4. 33 Modified square root domain second order allpass filter

Table 4. 5 The parameters of the second order allpass filter

Parameter values	
Q	1
V_{DD}	2.5V
U (D.C. voltage)	1.4V
C	5pF
I_0	30µA
I_{bias1}	3.7µA
I_{TH}	14.835µA
Aspect ratio of transistor M_1 - M_3	14µm/7µm
Aspect ratios of transistors M_4, M_6 , M_7, M_9– M_{11}, and M_{13} - M_{16}	0.7µm/7µm
Aspect ratios of transistor M_5	0.7µm/14µm
Aspect ratios of transistor M_8	0.7µm/2.33µm
Aspect ratios of transistor M_{12}	0.7µm/21µm

The presented second order allpass filter was simulated by using TSMC 0.25µm CMOS Level 3 model parameters (Appendix) with values of parameters given in Table 4.5. In the circumstance, theoretical cut-off frequency is 1.18MHz while simulated is 1.18MHz. Gain and phase responses of the second order allpass filter are indicated in Figure 4.34 with theoretical response.

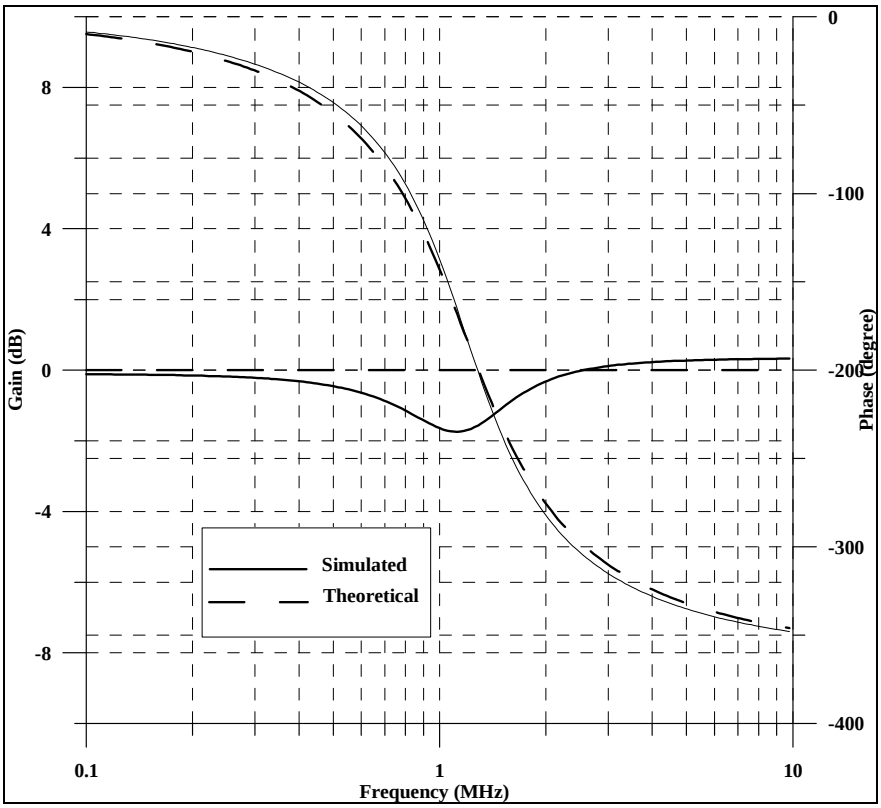

Figure 4. 34 Gain and phase responses of the second order allpass filter

The time response with 10mV sinusoidal input voltage at 1.18MHz that causes 428.9ns time delay at the output of the filter corresponding to 182.5˚ pahse difference. The time response and the dependence of the harmonic distorition on input signal amplitude of the filter are indicated in Figure 4.36 and 4.37 respectively. As such, input signal must be 200 mV or less to avoid output distortion. Quality factor of the filter can be adjusted with W/L parameters of the M_5, $M_{8,}$ M_{12}, and M_{14} transistors in the current mirrors and bias currents. Figure 4.38 shows the quality factor tuning of the second order allpass filter for Q.

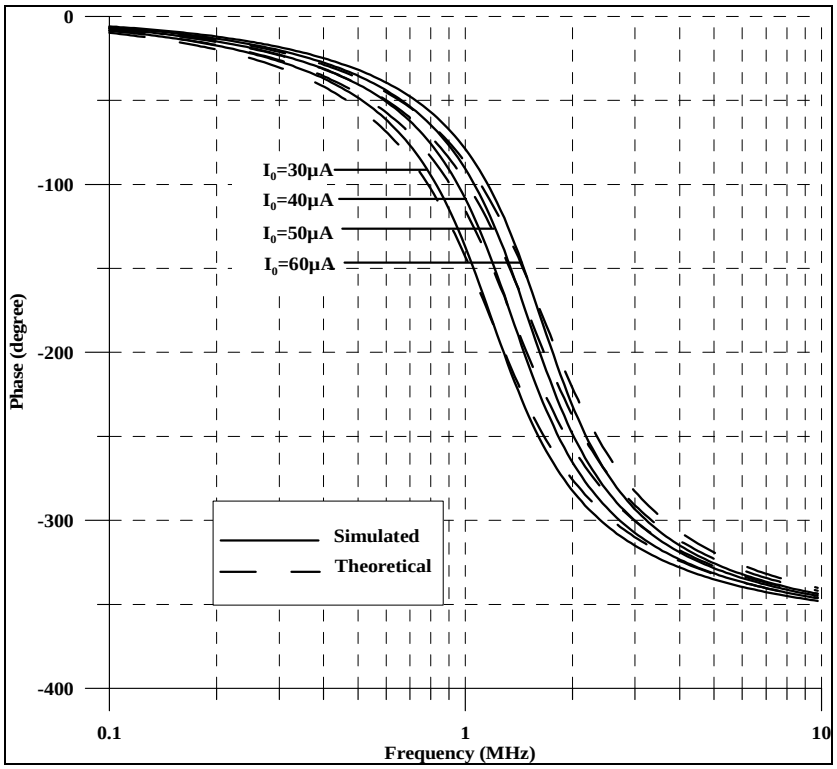

Figure 4. 35 Electronically tuneable phase response of the second order allpass filter I_0 is 30µA, 40µA, 50µA, and 60µA

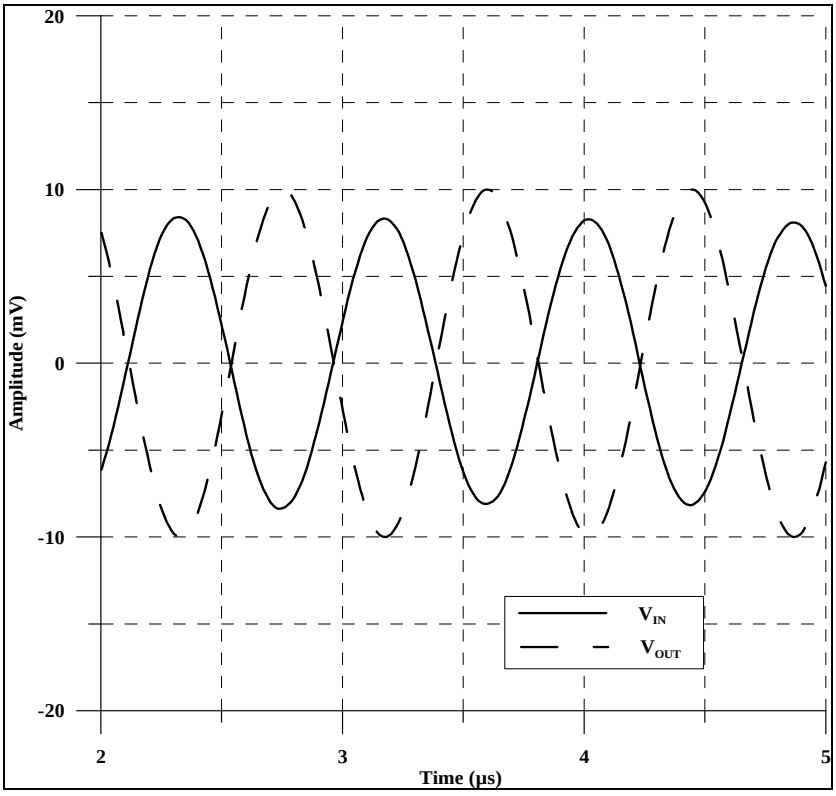

Figure 4. 36 The time response of the second order allpass filter

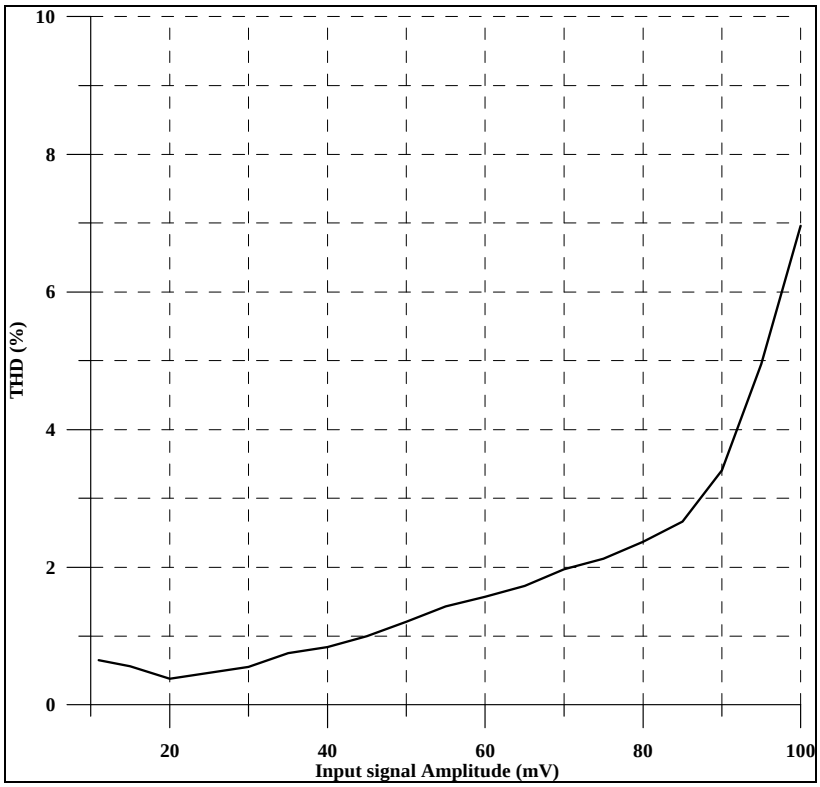

Figure 4. 37 THD versus input signal amplitude at 1.18MHz of allpass filter

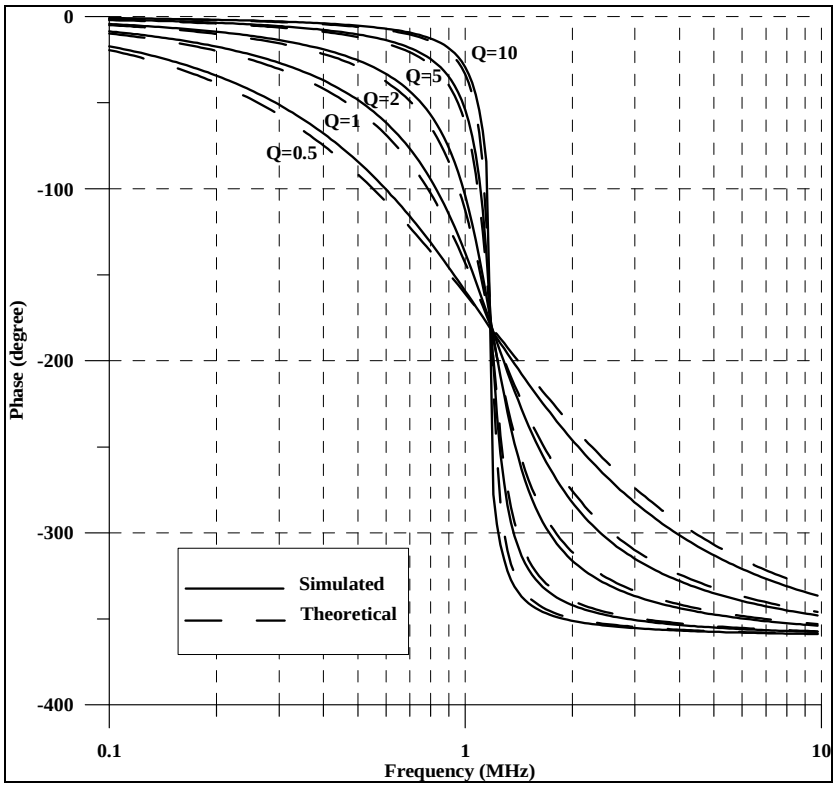

Figure 4. 38 The phase response of the second order allpass filter for Q is 0.5, 1,2,5,and 10

The performance of the second order allpass filter in terms of the sensitivity of MOS transistor parameter mismatch and tolerances of the capacitors has been evaluated by performing Monte Carlo simulations. For performing the Monte Carlo analysis, *W* and *L* dimensions of the all transistors in the filter have uniform distribution with 5% tolerances and the capacitor in the filter circuit have uniform deviation with 10% tolerances. The phase response of the second order allpass filter with Monte Carlo analysis for 100 runs is shown in Figure 4.39 when the cut off frequency is 1.18MHz. The phase degree was obtained between 154˚ and 201˚ during the analysis.

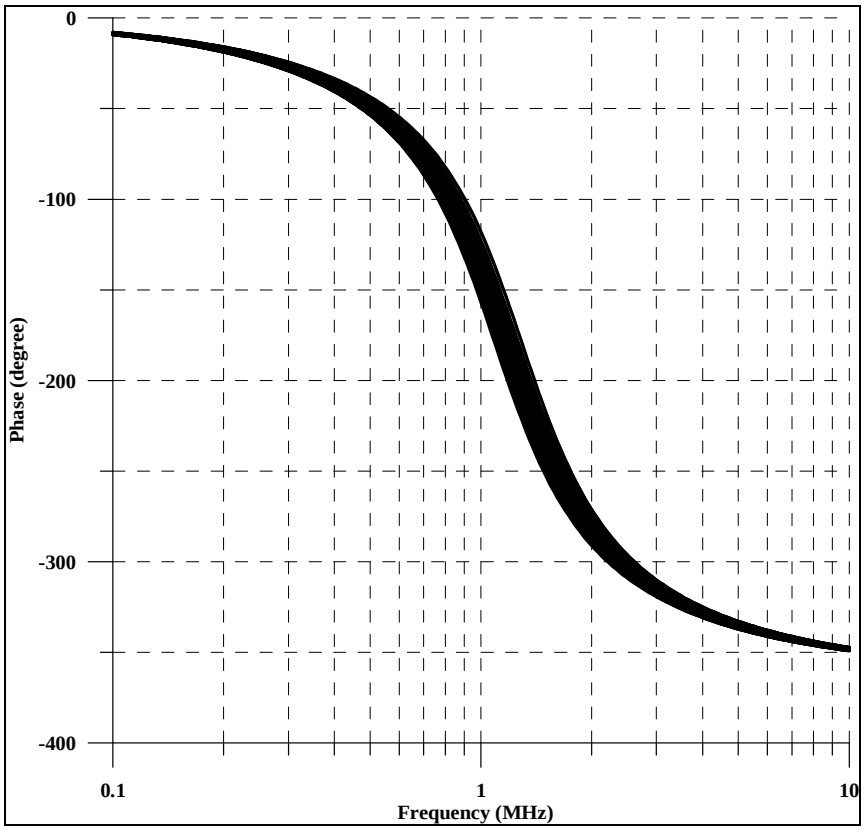

Figure 4. 39 Phase response of the second order allpass filter with Monte Carlo analysis

4.6 KHN Biquad Filter

KHN (Kerwin-Huelsman-Newcomb) biquad filter that provides lowpass, highpass, and bandpass filter outputs at a time has several advantages such as low passive and active sensitivities, low component spread and good stability behavior

(Kerwin, Huelsman, & Newcomb, 1967). In the literature, as a companding circuit, a KHN biquad filter was presented by Tola and others in 2009 and square root domain KHN biquad filter was proposed by Ölmez and Çam in 2009.

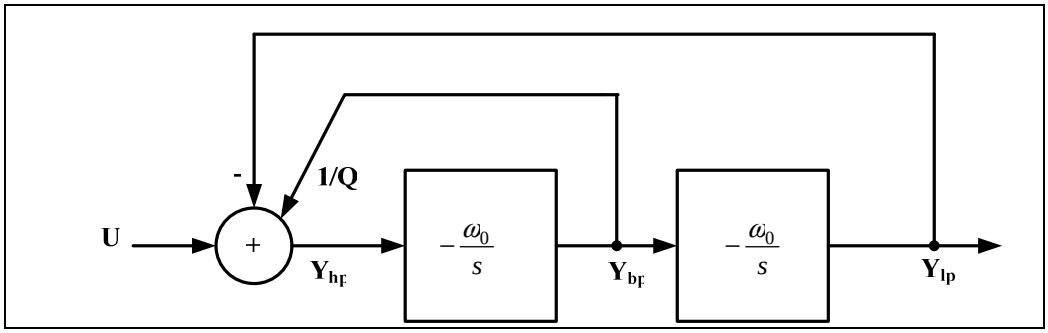

Figure 4. 40 Block diagram of KHN biquad filter

The block diagram of KHN biquad filter is shown in Figure 4.40 (Lopez & Vredad, 1997). To make compatible the block diagram to design in square root domain, it is modified as in Figure 4.41 (Ölmez & Çam, 2009).

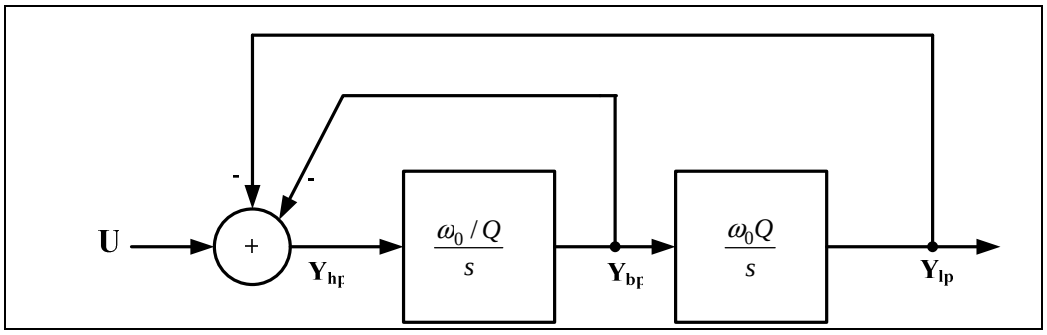

Figure 4. 41 Modified KHN biquad filter block diagram

The transfer functions of highpass, bandpass, and lowpass are obtained by using nodal analysis as;

$$H_{hp}(s) = \frac{s^2}{s^2 + \frac{\omega_0}{Q} s + \omega_0^2} \tag{4.45}$$

$$H_{bp}(s) = H_{hp}(s).\frac{\omega_0 / Q}{s} = \frac{(\omega_0 / Q)s}{s^2 + \frac{\omega_0}{Q} s + \omega_0^2} \tag{4.46}$$

$$H_{lp}(s) = H_{hp}(s).\frac{\omega_0^2}{s^2} = \frac{\omega_0^2}{s^2 + \frac{\omega_0}{Q}s + \omega_0^2} \tag{4.47}$$

In the block diagram, there are two lossless integrator blocks and a circuit that takes the differences between node voltages. By combining lossless integrators presented in Chapter 3 and a transconductor circuit that takes voltage differences in chapter 2, square root domain KHN biquad filter is obtained as indicated in Figure 4.42.

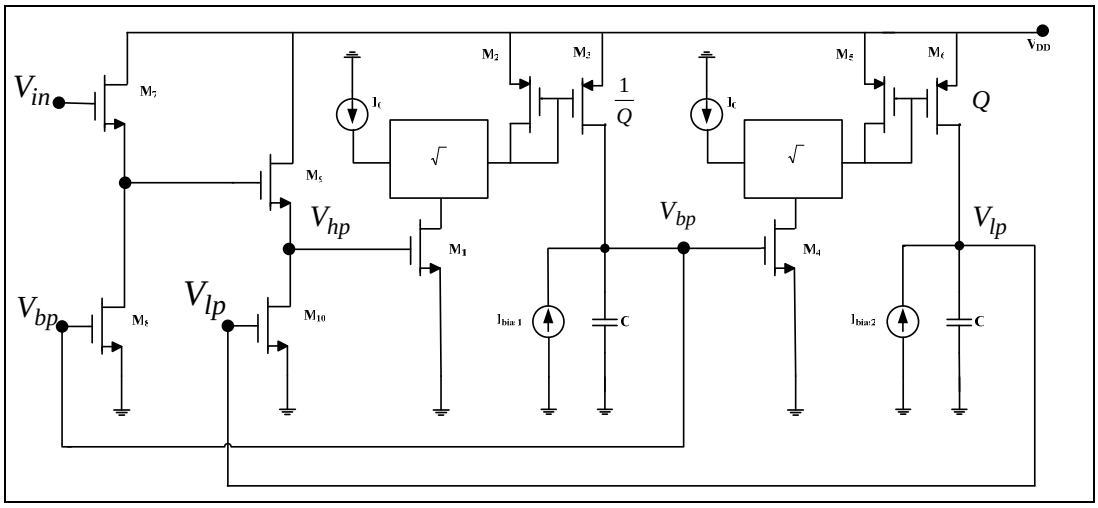

Figure 4. 42 The schematic of square root domain KHN biquad filter

In Figure 4.42, I_{bias1} and I_{bias2} currents are $\frac{1}{Q}C\omega_0 V_{TH} - \frac{C\omega_0 U}{Q}$ and $QC\omega_0 V_{TH} - QC\omega_0 U$, respectively. Simulations of KHN biquad filter and lossless integrator were performed in SPICE simulation program with TSMC 0.25µm CMOS Level 3 model parameters (Appendix) and values of parameters given in Table 4.6. Under these conditions the theoretical cut off frequency of the filter was 1.585 MHz, while the simulation result was 1.5495MHz.

Table 4. 6 The parameters of the KHN biquad filter

Parameter values	
Q	1
V_{DD}	2.5V
V_{IN} (D.C. voltage)	2.1V
C	7pF
I_0	50μA
I_{bias1}, I_{bias2}	22.5μA
Aspect ratio of transistor M_1, M_4	7μm/7μm
Aspect ratios of transistors M_2, M_3, and M_5– M_{10}	1μm/7μm

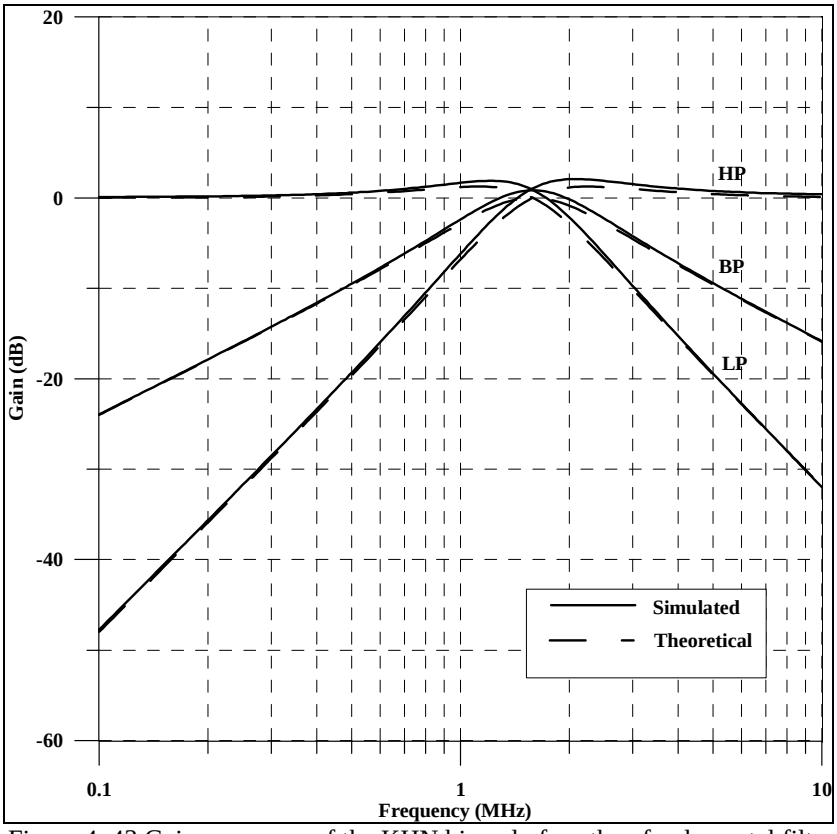

Figure 4. 43 Gain responses of the KHN biquad for the fundamental filter functions

Figure 4.44 shows the simulated and theoretical gain responses of the lowpass filter, while the bias current I_0 was changed from 20μA to 80μA. For different quality factor from 0.1 to 10, while the bias current was 30μA, bandpass filter

response is demonstrated in Figure 4.45. For performing the Monte Carlo analysis, W and L dimensions of the all transistors in the filter have uniform distribution with 10% tolerances and two capacitors in the filter circuit have uniform deviation with 10% tolerances. The gain response of the highpass filter with Monte Carlo analysis for 50 runs is shown in Figure 4.46 when the center frequency of filter was 1.737MHz at 60µA bias current. The center frequency was obtained between 1.614MHz and 1.85 MHz.

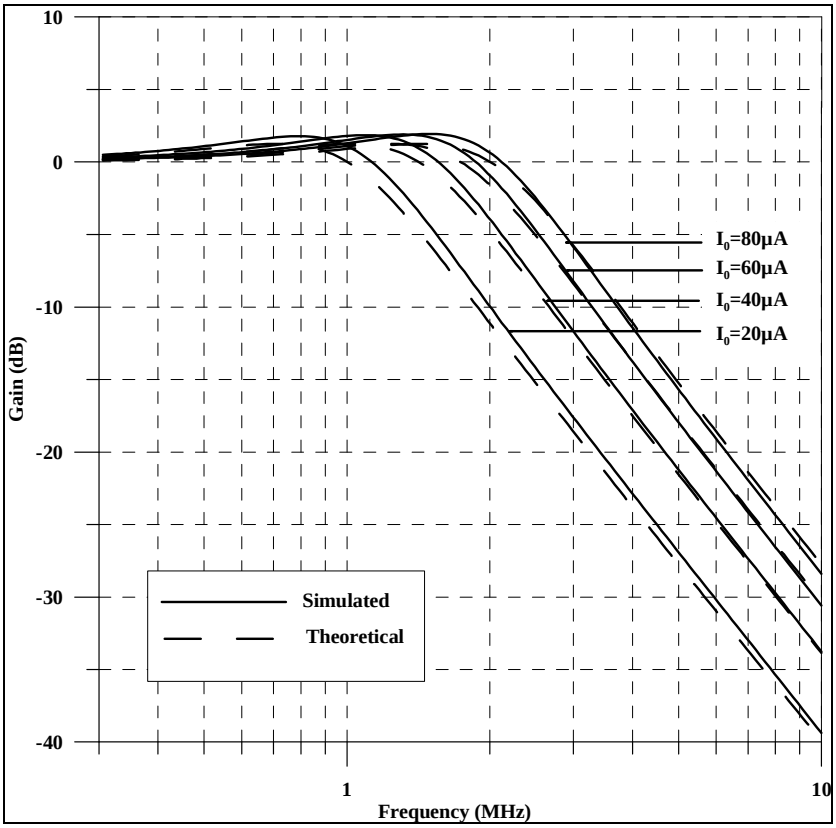

Figure 4. 44 Gain response of the lowpass filter, while is changed from 20µA to 80µA

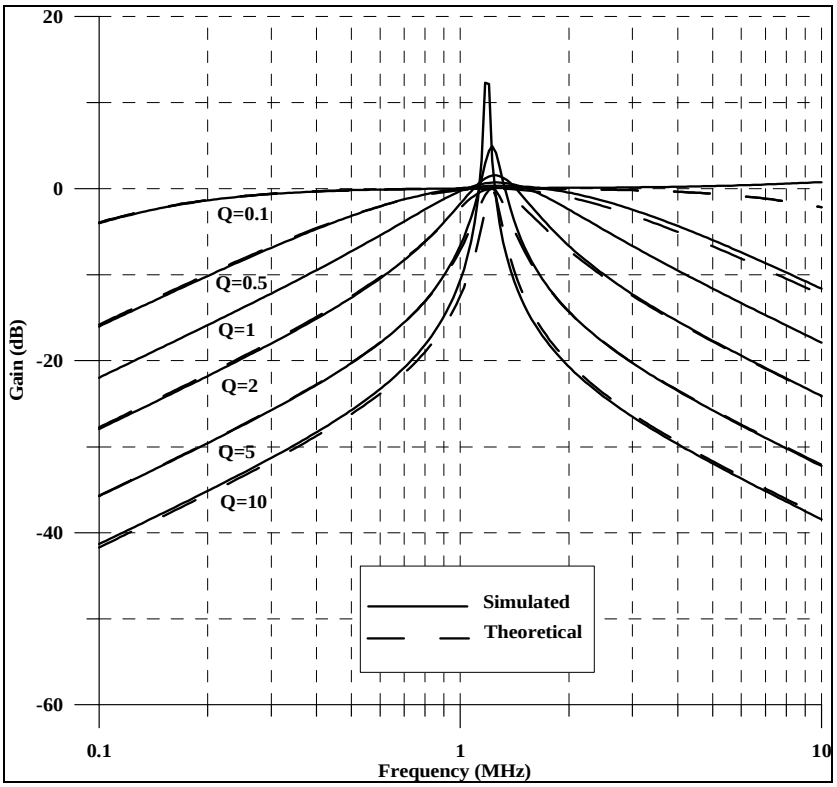

Figure 4. 45 The quality factor tuning for bandpass filter for Q is 0.1, 0.5, 1, 2, 5, and 10

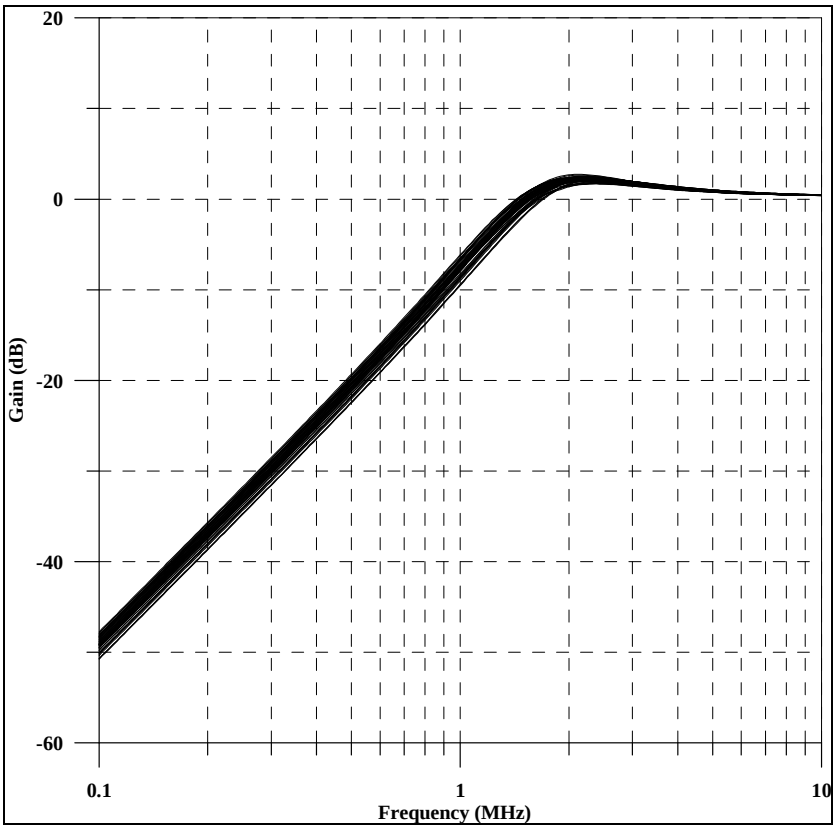

Figure 4. 46 Gain response of the highpass filter with Monte Carlo analysis

4.7 Tow-Thomas Biquad Filter

Tow-Thomas biquad that was introduced by Tow in 1969 and independently Thomas in 1971 provides lowpass and bandpass filter output. Square root domain Tow-Thomas biquad filter was firstly introduced by Ölmez and Çam in 2010. Tow-Thomas biquad filter consists of a lossless integrator, a lossy integrator, and a summation block as shown in Figure 4.47. This block diagram is modified as shown in Figure 4.48, to realize the biquad in square root domain.

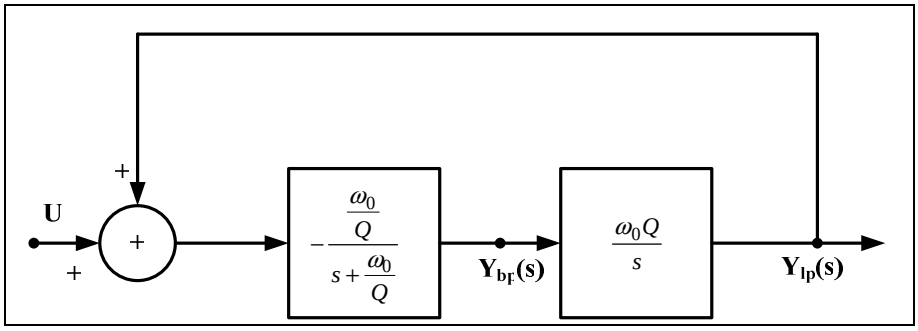

Figure 4. 47 Block diagram of Tow-Thomas biquad filter

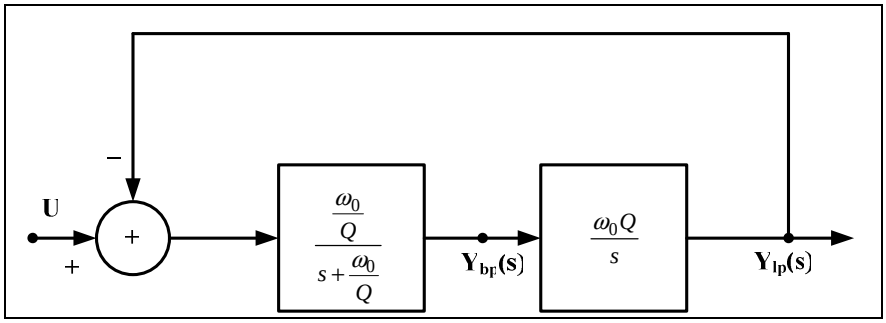

Figure 4. 48 Modified block diagram of Tow-Thomas biquad filter

The transfer functions of bandpass and lowpass are;

$$H_{bp}(s) = \frac{(\omega_0 / Q)s}{s^2 + \frac{\omega_0}{Q}s + \omega_0^2} \tag{4.48}$$

$$H_{lp}(s) = \frac{\omega_0^2}{s^2 + \frac{\omega_0}{Q}s + \omega_0^2} \tag{4.49}$$

Similarly to KHN biquad filter, by combining of a lossless integrator, a lossy integrator form Chapter 3, and a transconductor circuit that takes voltage difference form Chapter 2, Tow- Thomas biquad filter is obtained as shown in Figure 4.49.

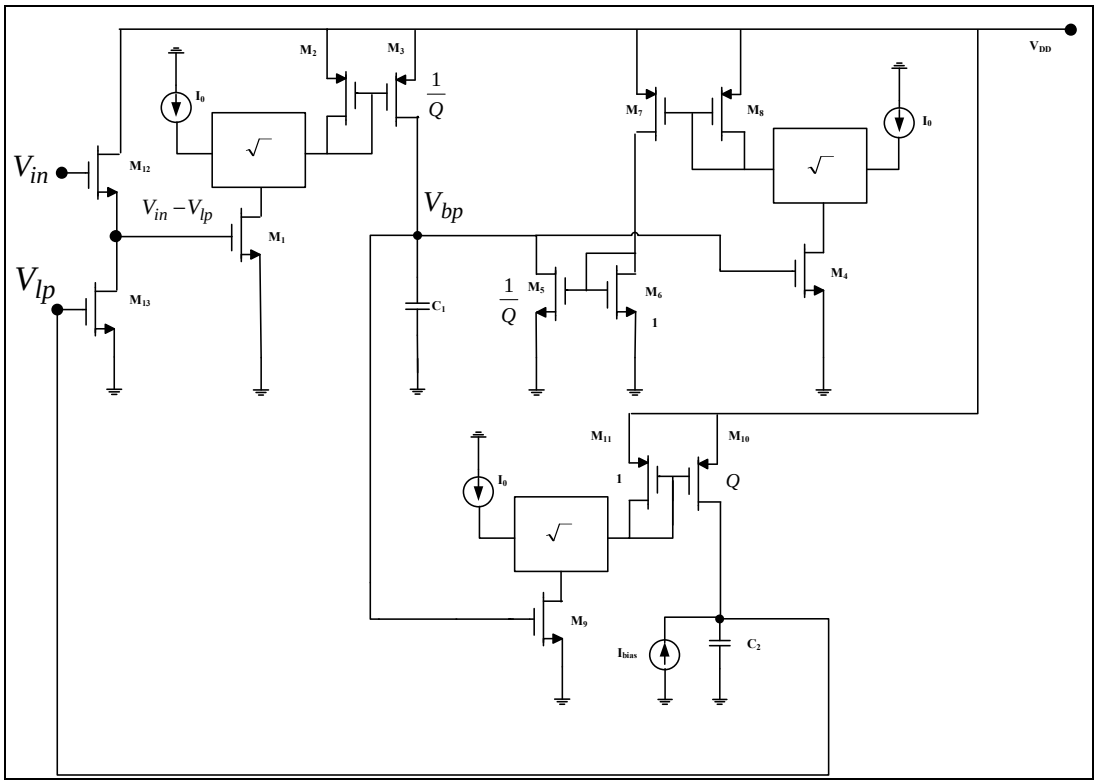

Figure 4. 49 Square root domain Tow-Thomas biquad filter

Table 4. 7 The parameters of the Tow-Thomas biquad filter

Parameter values	
Q	1
V_{DD}	2.5V
V_{IN} (D.C. voltage)	1.66V
C	15pF
I_0	100µA
I_{bias1}, I_{bias2}	22.5µA
Aspect ratio of transistors M_1 , M_4, and M_9	7µm/7µm
Aspect ratios of transistors M_2, M_3 , M_5– M_8, M_{10}, M_{11}	0.7µm/3.5µm
Aspect ratio of transistors M_{12} and M_{13}	0.7µm/7µm

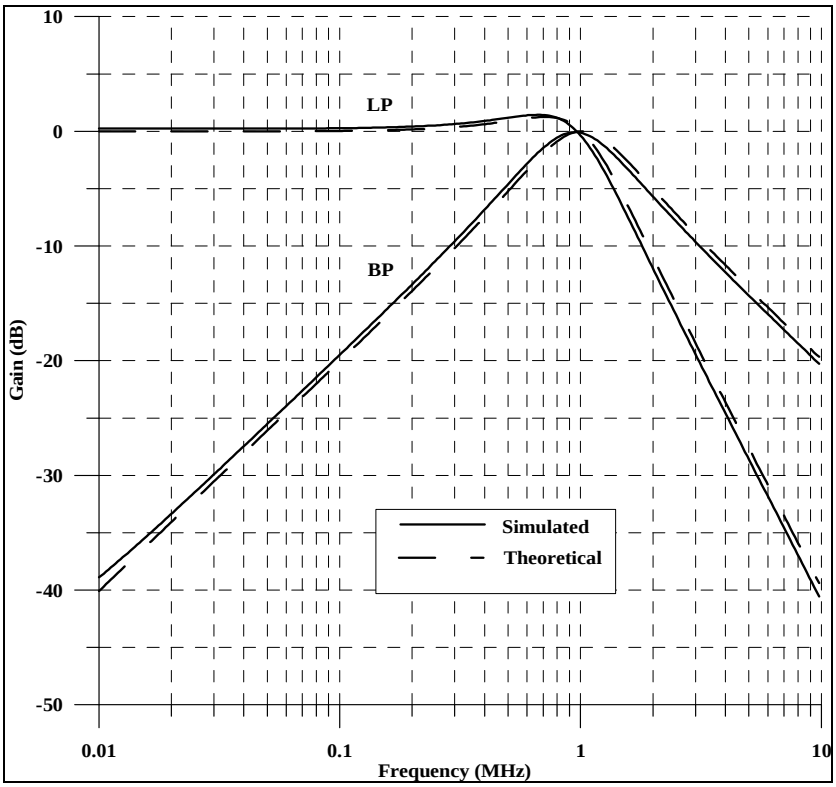

Figure 4. 50 Gain responses of the Tow-Thomas biquad for the fundamental filter functions

Simulations of the filter were performed in SPICE simulation program with TSMC 0.25µm CMOS model parameters and and values of parameters given in Table 4.7. Under these conditions the theoretical cut off frequency of the filter was 1.01 MHz, while the simulation result was 979.3 KHz.

Figure 4.51 shows the simulated and theoretical gain responses of the bandpass filter, while the bias current I_0 was changed from 40µA to 120µA. For different quality factor from 0.1 to 10, while the bias current was 60µA, bandpass filter response is demonstrated in Figure 4.45.

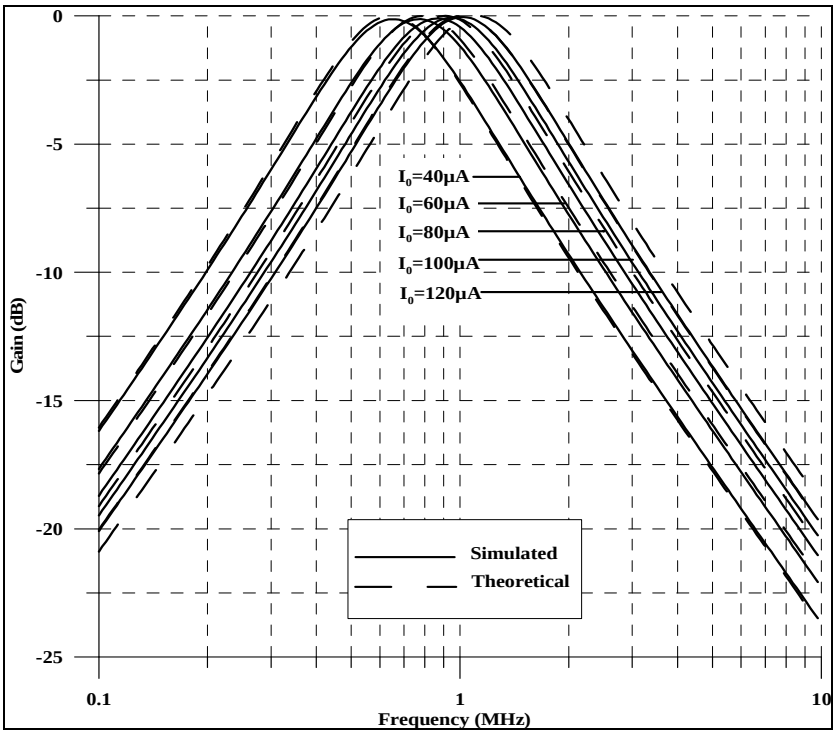

Figure 4. 51 Gain response of the bandpass filter, while I_0 was changed from 40µA to 120 µA.

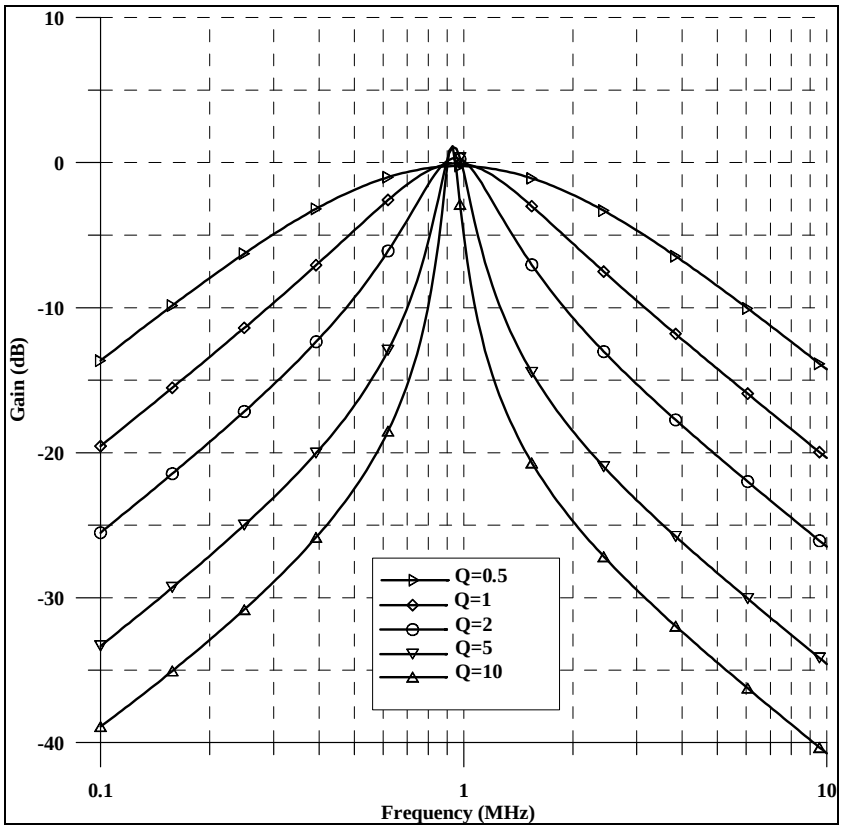

Figure 4. 52 The quality factor tuning for bandpass filter while the bias current is 60 µA.

CHAPTER FIVE
APPLICATION EXAMPLES OF THE PROPOSED SQUARE ROOT DOMAIN CIRCUITS

Filters are widely used in electronic system applications as; electronics, telecommunications, radar, consumer electronics, instrumentation systems to remove the frequencies in certain parts and to improve the magnitude, phase delay in some parts of the spectrum of a signal (Su, 2002) (Shenoi, 2006).In this chapter, 5th order Butterworth lowpass filter is proposed. This filter is appropriate to Bluetooth/Wi-Fi receivers. Also in this chapter, square root domain quadrature oscillator is proposed for the first time in the literature. Besides, a square root domain oscillator designed by using state space synthesis method is presented.

5.1 5th Order Butterworth Lowpass Filter For Bluetooth/Wi-Fi Receiver

Analog filters place in analog interface circuits in digital systems as it can be seen in many applications. One of them is Bluetooth/Wi-Fi (Wireless Fidelity) receiver. Literature survey shows that 5th order Butterworth filter is appropriate for Bluetooth/Wi-Fi receiver (Emira and others, 2004; Emira and others, 2006; Mohieldin and Sinenco, 2004).

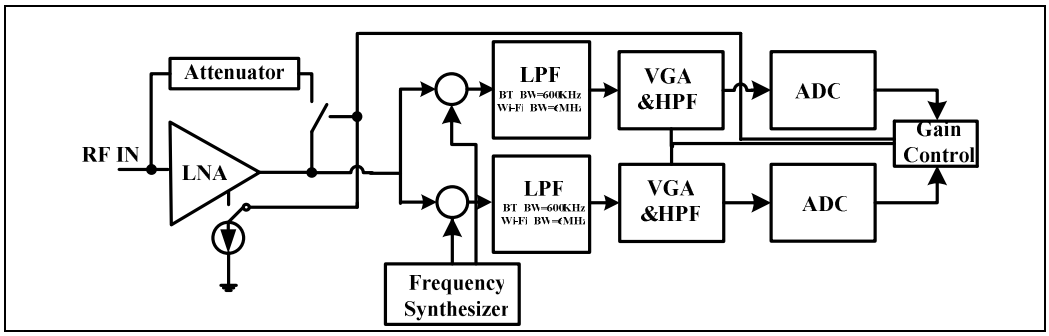

Figure 5. 1 Dual-mode Wi-Fi/BT receiver.

In square root domain, high order filters are designed by cascading first and second order ones (Yu, 2005). To design the 5th order Butterworth lowpass filter, its transfer function is decomposed to first an second order lowpass filters. The transfer function of normalized 5th order Butterworth lowpass filter is written as;

$$H(s) = \frac{1}{(s+1)(s^2+0.618s+1)(s^2+1.618s+1)} \tag{5.1}$$

According to Equation (5.1), the filter can be designed by cascading one first order lowpass filter and two second order lowpass filters. The transfer functions of each part are defined as;

$$H_{lp1}(s) = \frac{\omega_0}{s+\omega_0} \tag{5.2}$$

$$H_{lp2}(s) = \frac{0.618\omega_0^2}{s^2+0.618\omega_0 s+\omega_0^2} \tag{5.3}$$

$$H_{lp3}(s) = \frac{1.618\omega_0^2}{s^2+1.618\omega_0 s+\omega_0^2} \tag{5.4}$$

where ω_0 is cut-off frequency. Figure 5.2 shows square root domain 5th order Butterworth lowpass filter. The presented second order allpass filter was simulated by using TSMC 0.25µm CMOS mode parameters with values of parameters given in Table 5.1. Lowpass filter cut-off frequency is 6MHz and 600k.Hz for Wi-Fi, Bluetooth, respectively.

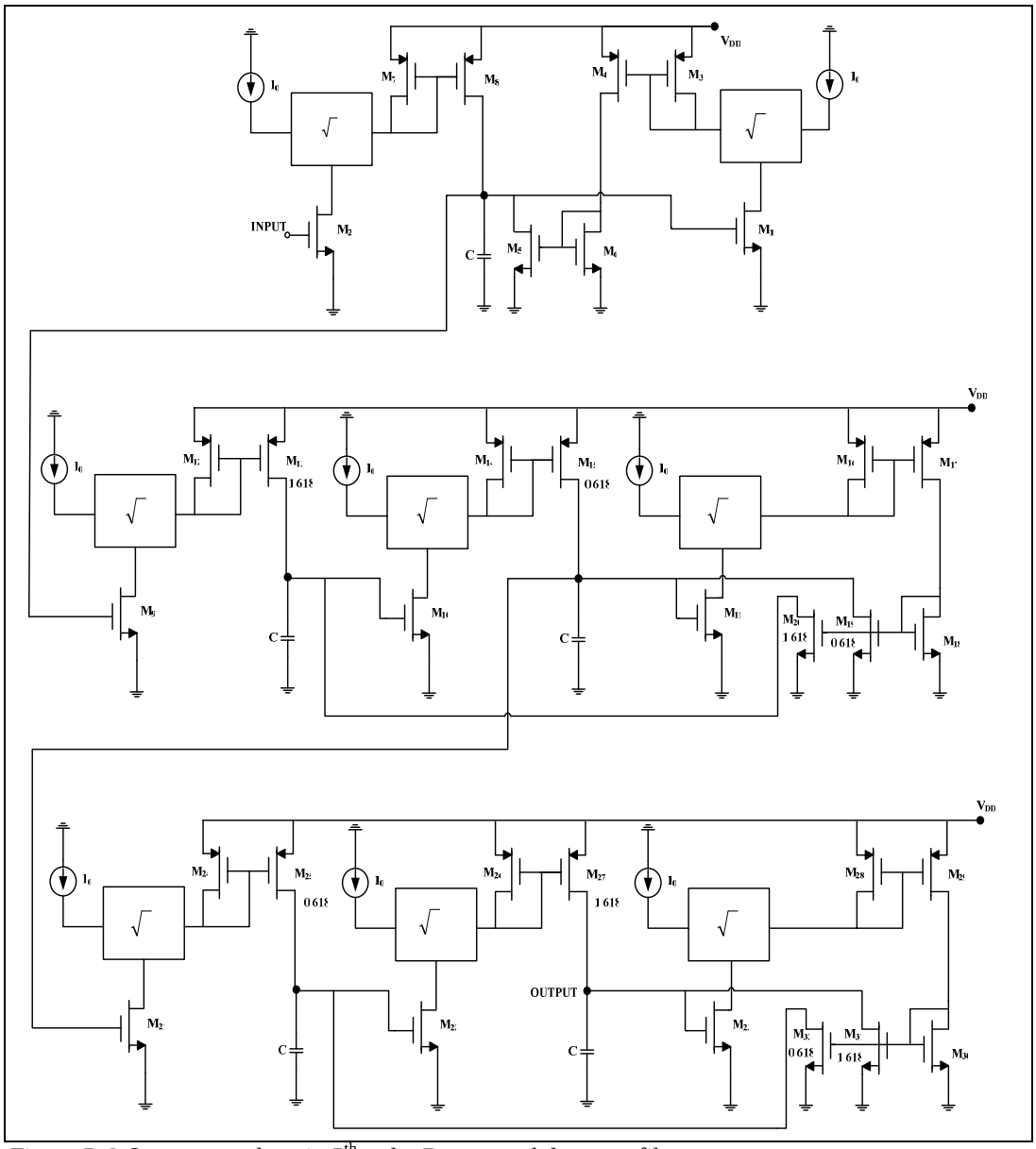

Figure 5. 2 Square root domain 5th order Butterworth lowpass filter

Gain responses of the filter in two mode are illustrated in Figure 5.2 and Figure 5.3 with the theoretical responses. To change the mode of the filter it is needed to change only bias current with same structure. Table 5.2 summarized the simulation results for both Wi-Fi and Bluetooth mode.

Table 5. 1 The parameters of the 5th order Butterworth lowpass filter

Parameter values	
V_{DD}	2.5V
U (D.C. voltage)	0.5V
C	1.5pF
I_0	32.194μA (for Wi-Fi) 0.32194 μA (for Bluetooth)
Aspect ratio of transistor M_1 - M_{12} , M_{16}, M_{17}, M_{21} - M_{23}	7μm/7μm
Aspect ratios of transistors M_{14},M_{18}	7μm/14μm
Aspect ratios of transistor M_{13}	7μm/11.326μm
Aspect ratios of transistors M_{15},M_{19}	7μm/8.652μm
Aspect ratios of transistors M_{20}	7μm/22.652μm
Aspect ratios of transistor M_{24}, M_{28}, M_{29}	0.7μm/7μm
Aspect ratios of transistors M_{25}, M_{32}	0.7μm/8.652μm
Aspect ratios of transistors M_{16}, M_{20}	0.7μm/14μm
Aspect ratios of transistors M_{27}, M_{30}	0.7μm/22.652μm

Table 5. 2 Simulation results of 5th order Butterworth lowpass filter

	Wi-Fi	Bluetooth
Power consumption	1.55mW	0.741mW
IM3	-51.55dBm	-29.66dBm
Dynamic Range	88.24dBm	59.1dBm
Output Noise	$4.18\text{x}10^{-14}\sqrt{V/Hz}$	$1.97\text{x}10^{-13}\sqrt{V/Hz}$

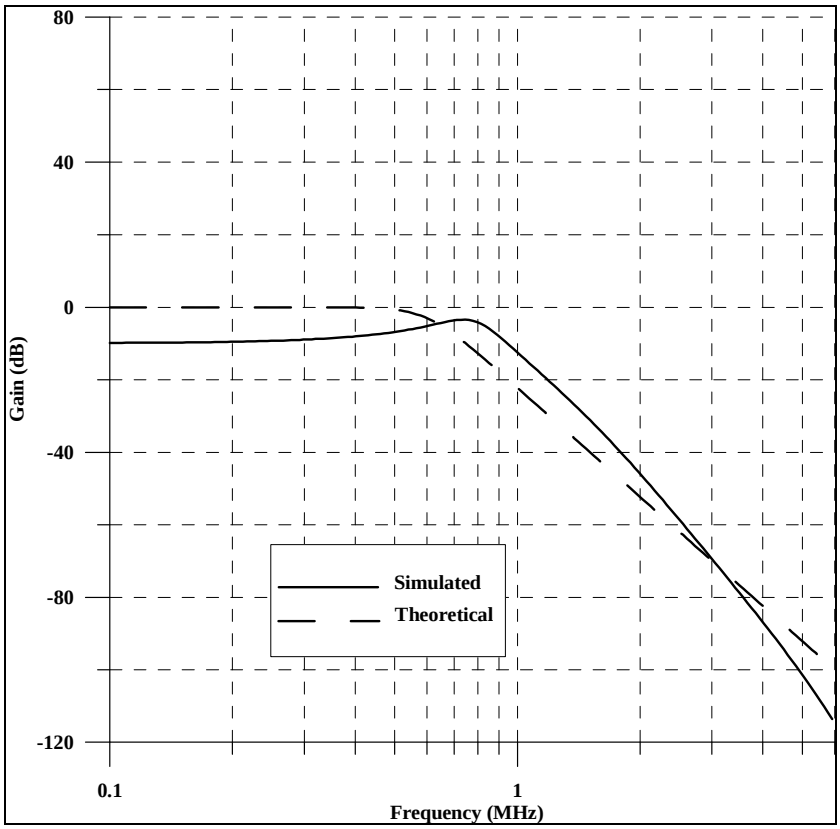

Figure 5. 3 Gain response of the 5th order Butterworth lowpass filter in Bluetooth mode

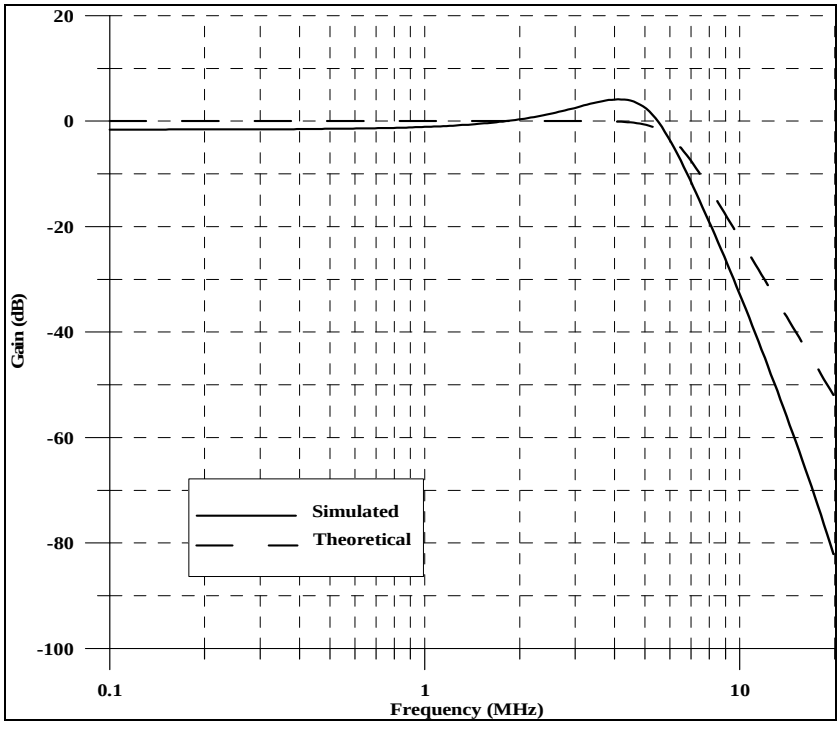

Figure 5. 4 Gain response of the 5th order Butterworth lowpass filter in Wi-Fi mode

5.2 Oscillators

5.2.1 A square root domain oscillator

Square root domain oscillators were presented by Thanachayanont and others in 1996, Mulder and others in 1998, Ragheb and Soliman in 2006. In this dissertation, a square root domain oscillator that was designed by using state space synthesis method and has different structure from others was presented. A simple oscillator transfer function can be written as follows;

$$H(s) = \frac{\omega_0^2}{s + (b-a)\omega_0 s + \omega_0^2} \tag{5.5}$$

where ω_0 is oscillation frequency, b and a are coefficients. This transfer function allows to oscillate in three cases that;

(1) when b=a; oscillation maintained,

(2) when b-a>0, oscillation dies out,

(3) when b-a<0, waveform blows up.

The state space representation obtained by using observable canonical form is expressed as

$$\dot{x}_1 = -\omega_0^2 x_2 + \omega_0^2 u \tag{5.6}$$

$$\dot{x}_2 = x_1 - (b-a)\omega_0 x_2$$

$$y = x_2$$

To realize the filter, state variable x_1 is multiplied with ω_0. So the final state equations are obtained;

$$\dot{x}_1 = -\omega_0 x_2 + \omega_0 u \tag{5.7}$$

$$\dot{x}_2 = \omega_0 x_1 - (b-a)\omega_0 x_2$$

$$y = x_2$$

If b is equal to a, oscillation is occurred. Under this condition second state equation is rearranged that;

$$\dot{x}_2 = \omega_0 x_1 \tag{5.8}$$

If the node voltage V_1 , V_2 and voltage signal U are assumed the state variables x_1,

x_2, and u, state and output equations in (5.7) and (5.8) are rewritten as

$$C\dot{V}_1 = -\omega_0 V_2 + \omega_0 U \tag{5.9}$$

$$C\dot{V}_2 = \omega_0 V_1$$

$$y = V_2$$

where C is a capacitor value seemed as multiplying factor. $C\dot{V}_1$ and $C\dot{V}_2$ are accepted a current flows through a grounded capacitor C whose voltage across its terminals in order given V_1 and V_2 and by assuming that U, V_2, and V_1 are gate-source voltages of MOS transistors operating in saturation region with their drain currents are defined as I_u, I_2, and I_1, respectively. So capacitor current equations in (5.9) are arranged as

$$I_{C1} = -C\omega_0\left(\sqrt{\frac{I_2}{\beta}} + V_{TH}\right) + C\omega_0\left(\sqrt{\frac{I_u}{\beta}} + V_{TH}\right) \tag{5.10}$$

$$I_{C2} = C\omega_0\left(\sqrt{\frac{I_1}{\beta}} + V_{TH}\right)$$

where $I_1=\beta(V_1-V_{TH})^2$, $I_2=\beta(V_2-V_{TH})^2$, $I_u=\beta(U-V_{TH})^2$, $I_{C1} = C\dot{V}_1$, and $I_{C2} = C\dot{V}_2$. Hence, the state equations in (5.10) are transformed into

$$I_{C1} = -\sqrt{I_0 I_2} + \sqrt{I_0 I_u} \tag{5.11}$$

$$I_{C2} = \sqrt{I_0 I_1} + I_{TH}$$

where the bias current $I_0 = (\omega_0{}^2 C^2)/\beta$ and threshold voltage compensation current $I_{TH}=\omega_0 C V_{TH}$. So, the square root domain oscillator circuit composed of three geometric mean circuits, current mirror circuits, and a D.C. current source is shown in Figure 5.4

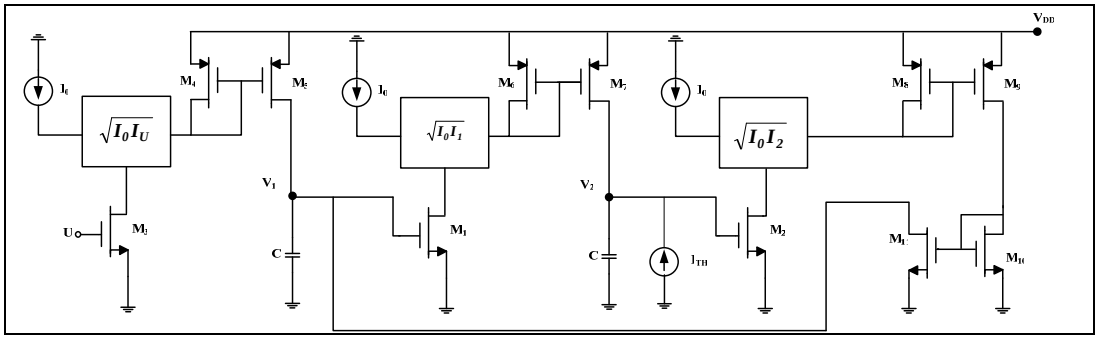

Figure 5. 5 Square root domain oscillator

It is known that D.C. operating point is very important to start to oscillate (Kundert, 1995). When it is considered that V_2 is equal to U and also V_1, state equations are rearranged that;

$$C\dot{V}_1 = -\omega_0 V_2 + \omega_0 U \tag{5.12}$$

$$C\dot{V}_2 = \omega_0 V_1$$

To provide the D.C. operating conditions, D.C. current sources are added to second state equation

$$C\dot{V}_2 = \omega_0 V_1 + I_{DC} \tag{5.13}$$

where I_{DC}=-$C\omega_0 U$. By substituting I_{DC} current source in the second state equation

$$I_{C2} = \sqrt{I_0 I_1} + I_{bias} \tag{5.14}$$

where I_{bias}=-$C\omega_0(U-V_{TH})$. By changing the I_{bias} current source value, the oscillation cases can be realized.

Simulations of oscillator were performed in SPICE simulation program with TSMC 0.25µm CMOS Level 3 model parameters (Appendix) and values of parameters given in table 5.3. Under these conditions the theoretical oscillation frequency of the filter was 193KHz, while the simulation result was 191KHz as shown in Figure 5.6.

Table 5. 3 The parameters of the oscillator

Parameter values	
V_{DD}	2.5V
C	50pF
I_0	20µA
I_{bias}	21.22µA
Aspect ratio of transistor M_1 - M_3	3.5µm/7µm
Aspect ratios of transistors M_4– M_{11}	0.7µm/7µm

When I_{bias} current source is 41µA and -20µA, the output waveforms are illustrated in Figure 5.7 and 5.8, respectively. Figure 5.7 shows that oscillator operates in unstable region and Figure 5.8 shows that oscilation dies out.

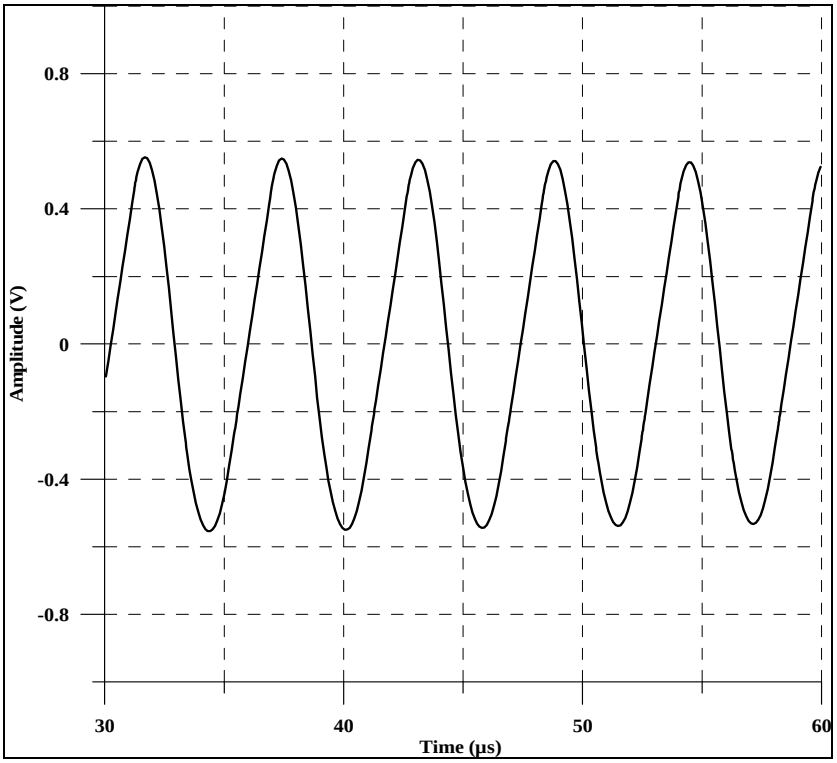

Figure 5. 6 Simulated output waveform of the oscillator

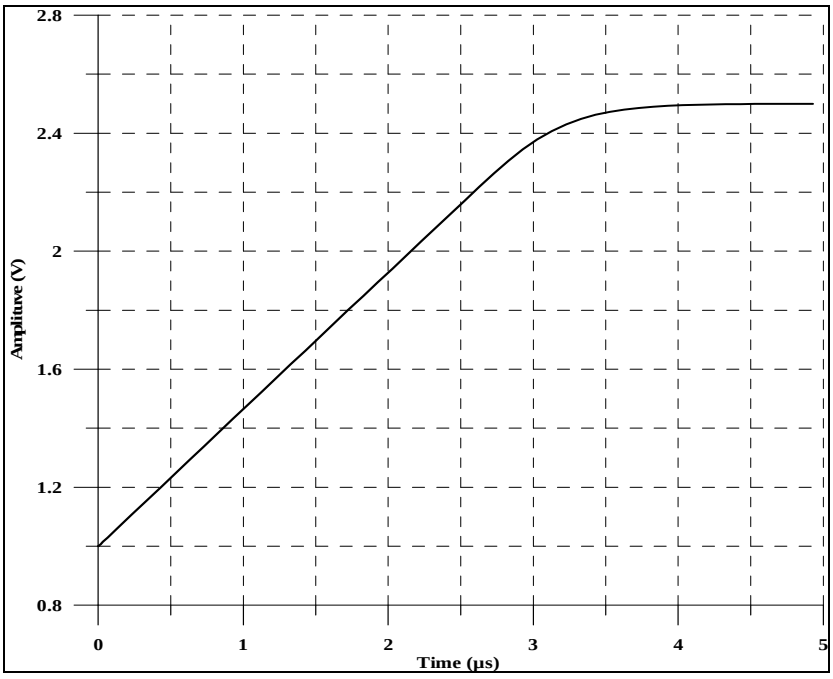

Figure 5. 7 Simulated output waveform of the oscillator under unstable condition

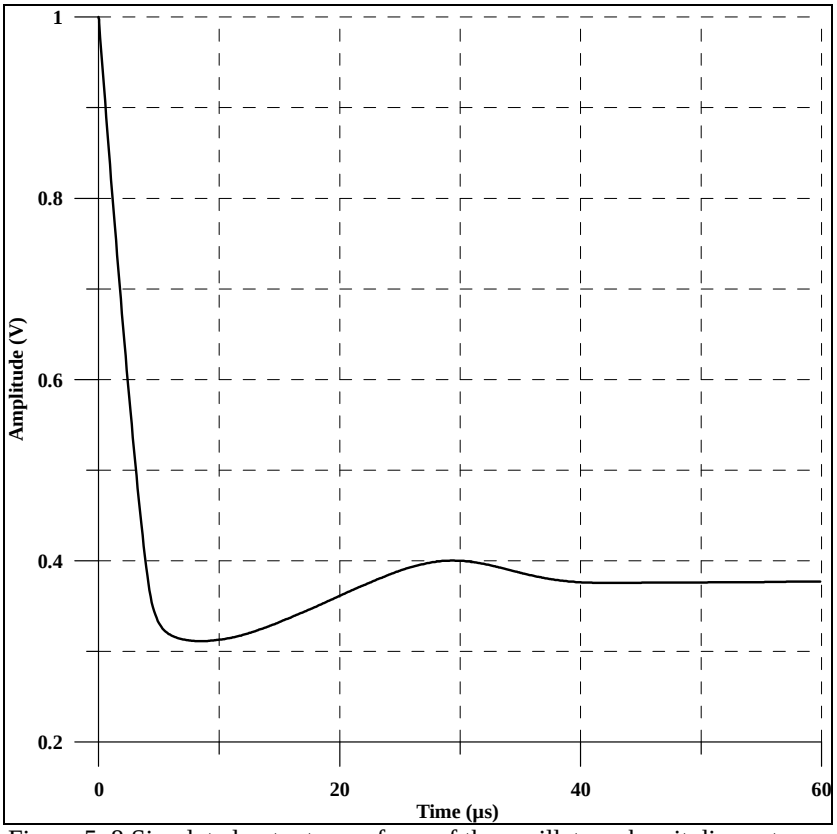

Figure 5. 8 Simulated output waveform of the oscillator when it dies out

5.2.2 Square root domain quadrature oscillator

Quadrature oscillator is obtained by combining first order allpass filter and a lossless integrator blocks as shown in Figure 5.9 (Kılınç & Çam, 2004)

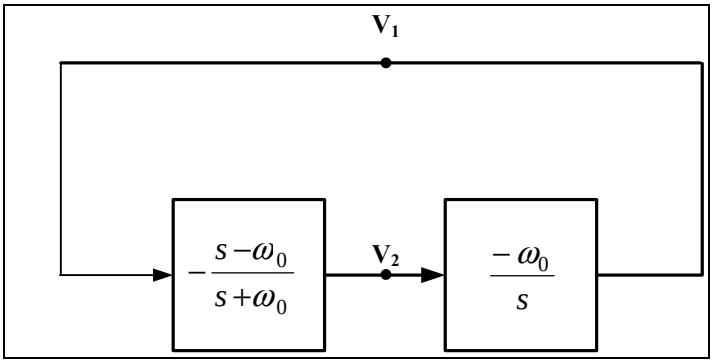

Figure 5. 9 Block diagram for quadrature oscillator

First order allpass and lossless integrator construction with adding a current mirror to obtain negative gain in Chapter 2 are used to be composed of the quadrature oscillator. The schematic of square root domain quadrature oscillator is illustrated in Figure 5.10.

Table 5. 4 The parameters of quadrature oscillator

Parameter values	
V_{DD}	2.5V
C	30pF
I_0	20μA
I_{TH}	18.94 μA
I_{bias}	14.2 μA
Aspect ratio of transistor M_1, M_2 and M_{11}	7μm/7μm
Aspect ratios of transistors M_3-M_5 , M_7-M_{10} , and M_{12}-M_{15}	0.7μm/7μm
Aspect ratios of transistor M_6	0.7μm /14μm

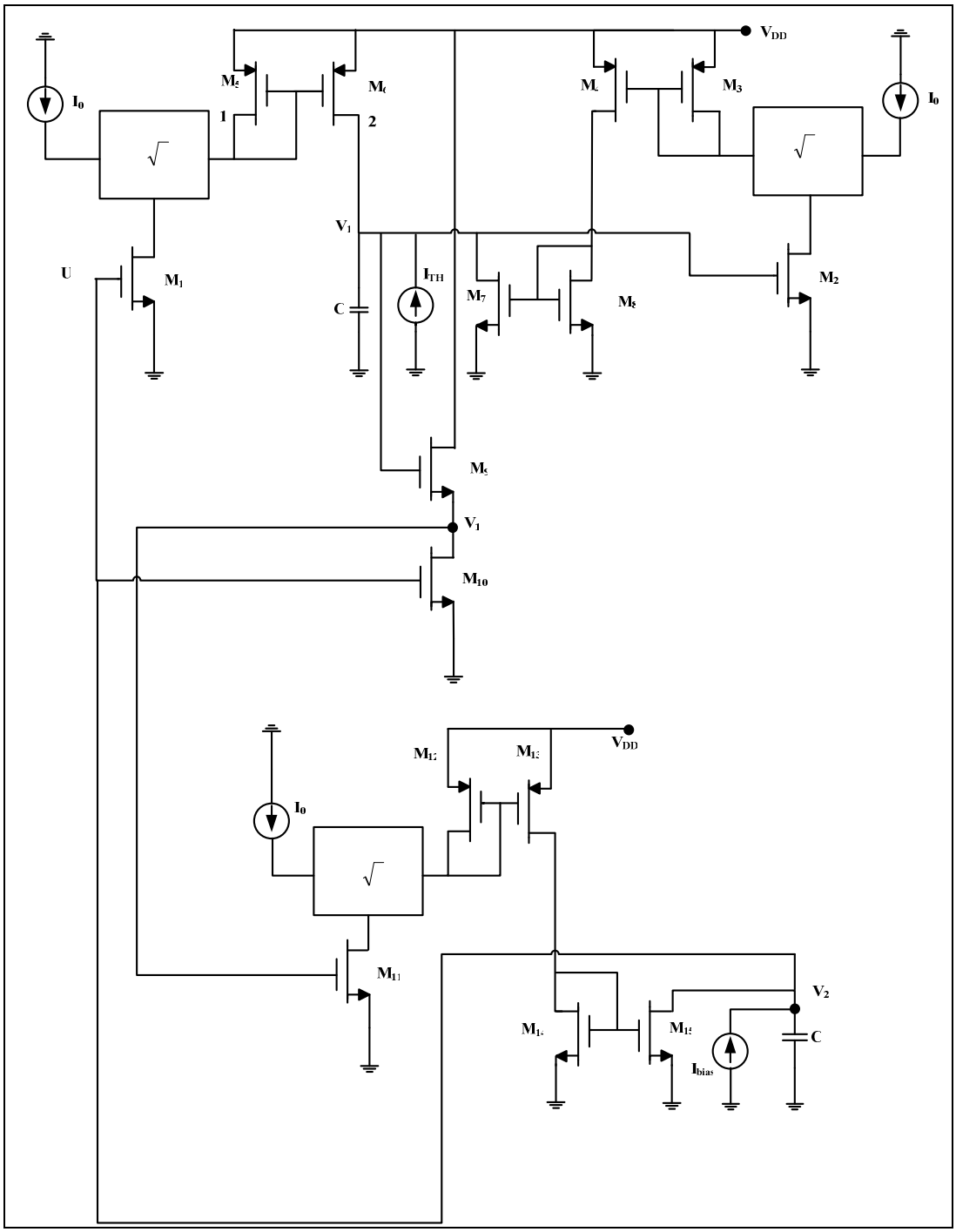

Figure 5. 10 Square root domain quadrature oscillator

By using TSMC 0.25μm CMOS Level 3 model parameters (Appendix), the quadrature was simulated with values of parameters given in table 5.4. Under these conditions, oscillation frequency is 234KHz while simulated is 243KHz.

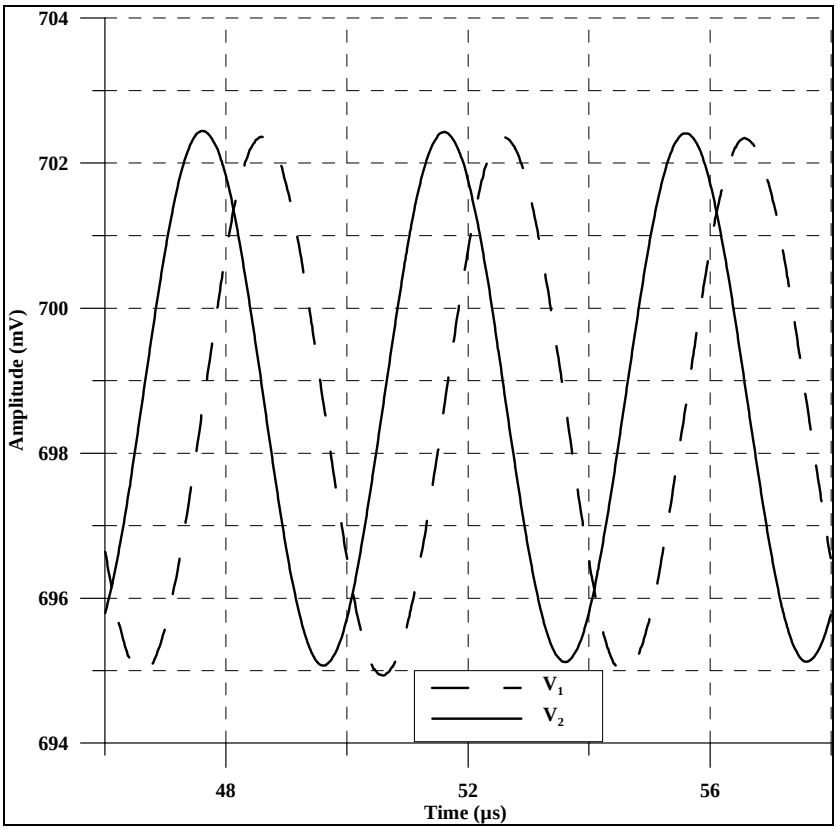

Figure 5. 11 Simulated waveforms of quadrature oscillator

CHAPTER SIX
CONCLUSION

6.1 Conclusion

In recent years, there is a growing research interest in the area of companding in the literature to being compatible with CMOS VLSI technology. In this dissertation study, novel square root domain filters and oscillators that is a subclass of companding circuits were proposed. All circuits are features of electronically tuneable by changing bias current and capacitors value. It is valid for all of them that consist of only capacitors and MOS transistors. Because of their structure, they have advantages as tunability due to applied bias current, high linearity, low-voltage-low power consumption, and large dynamic range. Also all square root domain circuits were designed by using state space synthesis method that is very powerful in companding circuit design.

In this thesis, lossless integrator, first order highpass, first order allpass, second order highpass, second order allpass, second order notch filter designed by using state space synthesis method in square root domain were proposed for the first time in the literature. By combining the proposed structures, KHN biquad, Tow-Thomas biquad filters were also proposed as novel. Besides the novel circuits, first order lowpass, second order lowpass, and second order bandpass filters were presented in different structures than the literatures'.

It is known that filters have wide usage area in electronic system applications. 5^{th} order Butterworth lowpass filter for Bluetooth/Wi-Fi receiver was designed by cascading first and second order lowpass filters. Additionally, a square root domain oscillator designed by using state space synthesis method was presented and quadrature oscillator created by cascading first order allpass filter and lossless integrator was proposed for the first time in the literature. All proposed circuits are electronically tuneable, suitable for low voltage/low power applications. The cut-off frequency of filters and oscillation frequency of oscillators can be adjustable by

changing external current sources. The quality factor of filter is also tunable. All simulations in the thesis were done by using PSpice simulation program. Due to consisting MOS transistors operating in saturation region and grounded capacitor; low power consumption, large dynamic range, and low THD value, the proposed circuits are compatible with CMOS VLSI technology.

6.2 Future Work

During the design procedures, MOS transistors are assumed to be ideal, second order effects like the body effect, mobility reduction, and channel length modulation are not noticed. In this dissertation, it is aimed to synthesis the structures, not optimization. So, the difference occurs between simulation and theoretical results as shown in simulation results. Designs can be considered with second order effects, operation of geometric mean circuit can be improved to obtain better results.

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APPENDIX

TSMC 0.25 µm CMOS Process Model Parameters

.MODEL CMOSN NMOS (LEVEL=3 TOX=5.7E-9 NSUB=1E17
+GAMMA=0.4317311 PHI=0.7 VTO=0.4238252 DELTA=0 UO=425.6466519
+ETA=0 THETA=0.1754054 KP=2.501048E-4 VMAX=8.287851E4
+KAPPA=0.1686779 RSH=4.062439E-3 NFS=1E12 TPG=1 XJ=3E-7
+LD=3.162278E-11 WD=1.232881E-8 CGDO=6.2E-10 CGSO=6.2E-10
+CGBO=1E-10 CJ=1.81211E-3 PB=0.5 MJ=0.3282553 CJSW=5.341337E-10
+MJSW=0.5)

.MODEL CMOSP PMOS (LEVEL=3 TOX=5.7E-9 NSUB=1E17
+GAMMA=0.6348369 PHI=0.7 VTO=-0.5536085 DELTA=0 UO=250 ETA=0
THETA=0.1573195 KP=5.194153E-5 VMAX=2.295325E5 KAPPA=0.7448494
+RSH=30.0776952 NFS=1E12 TPG=-1 XJ=2E-7 LD=9.968346E-13
+WD=5.475113E-9 CGDO=6.66E-10 CGSO=6.66E-10 CGBO=1E-10
+CJ=1.893569E-3 PB=0.9906013 MJ=0.4664287 CJSW=3.625544E-10
+MJSW=0.5)